Design Example Report

Title	*27 W USB PD 3.0 Power Supply with 3.3 V - 11 V PPS Output Using InnoSwitch™3-Pro INN3366C-H301 and VIA Labs VP302*
Specification	85 VAC – 265 VAC Input; 5 V / 3 A; 9 V / 3 A; or 3.3 V – 11 V PPS Output
Application	Mobile Phone Charger
Author	Applications Engineering Department
Document Number	DER-701
Date	June 28, 2019
Revision	1.1

Summary and Features

- InnoSwitch3-Pro - digitally controllable CV/CC QR flyback switcher IC with integrated high-voltage MOSFET, synchronous rectification and FluxLink™ feedback
  - I²C Interface enables low pin count USB PD Controller (8 pin)
  - Sophisticated telemetry and comprehensive protection features
- USB PD 3.0 with PPS using highly optimized, low pin count USB PD Controller VP302
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
- Meets DOE6 and CoC V5 2016 efficiency requirement (>1% efficiency margin)
- Micro stepping of voltages (20 mV) and CC thresholds (50 mA) in compliance with PPS protocol
- Output overvoltage and overcurrent protection
- Integrated thermal protection
- <30 mW no-load input power

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PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at https://www.power.com/company/intellectual-property-licensing/.

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing a 27 W USB PD power supply with 5 V / 3 A, 9 V / 3 A, or 3.3 V – 11 V Programmable Power Supply (PPS) output using InnoSwitch3-Pro INN3366C-H301 IC and VIA Labs VP302 USB PD controller. This design shows the high power density and efficiency that is possible due to the high level of integration of the InnoSwitch3-Pro controller providing exceptional performance.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data

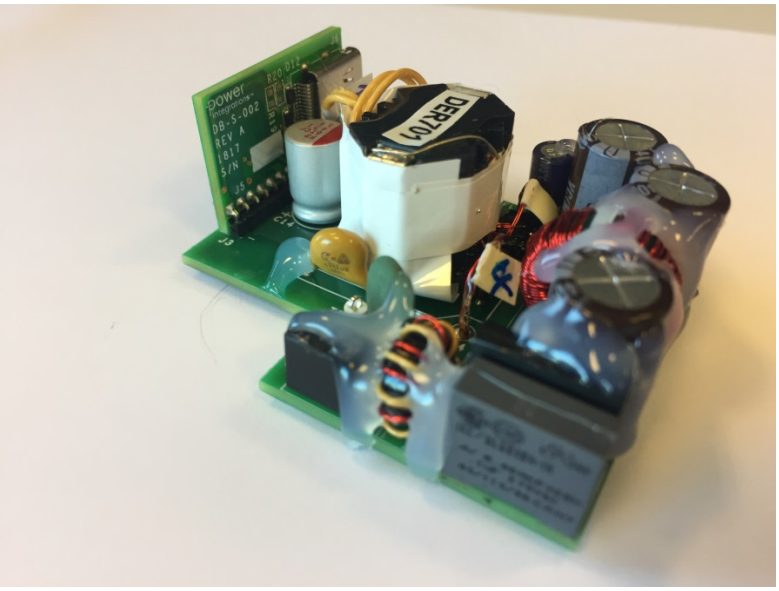

Figure 1 – Populated Circuit Board Photograph, Entire Assembly.

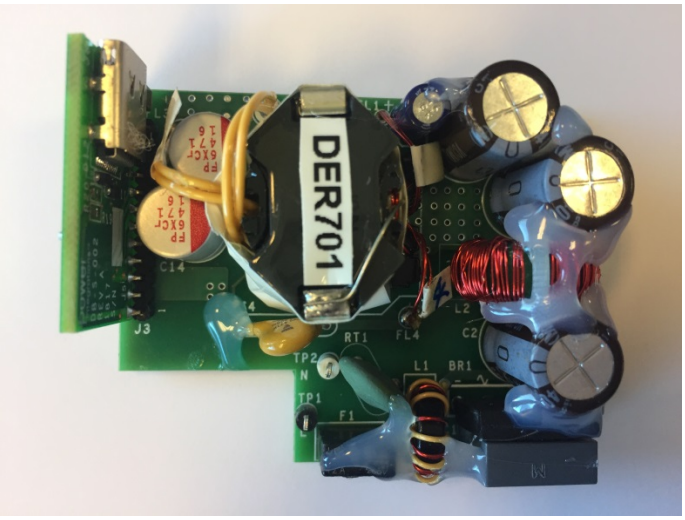

Figure 2 – Populated Circuit Board Photograph - Top.

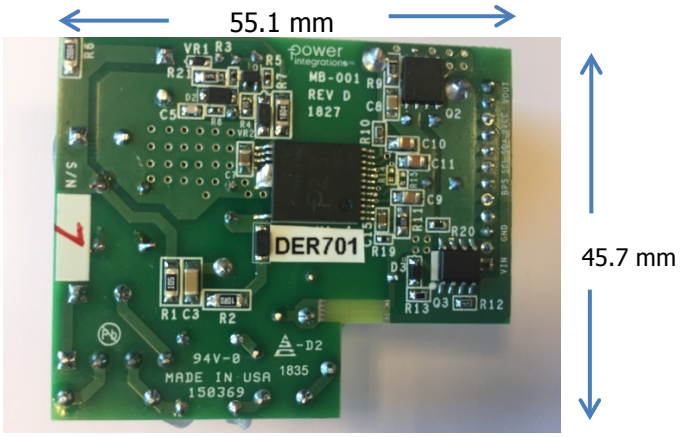

Figure 3 – Populated Circuit Board Photograph - Bottom.

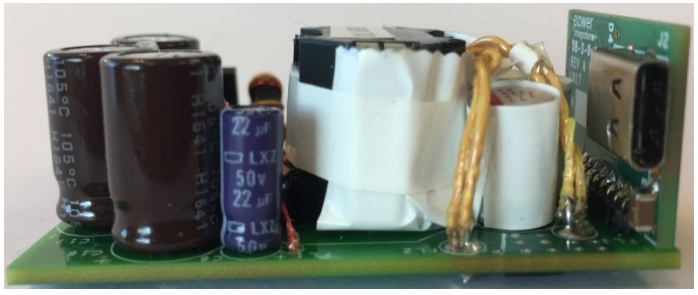

Figure 4 – Populated Circuit Board Photograph (Side View).

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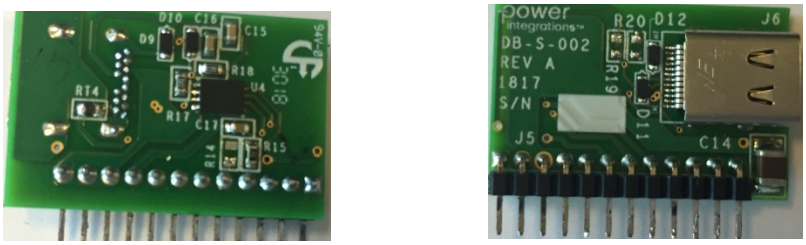

Figure 5 – Populated Circuit Board Photograph, Daughter Board. [Front and Rear].

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power			24.6		mW	Measured at 85 VAC.
5 V Setting						
Output Voltage	$V_{OUT(5\ V)}$		5.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(5\ V)}$			150	mV	Measured at End of 100 mΩ Cable. (20 MHz Bandwidth).
Output Current	$I_{OUT(5\ V)}$			3	A	±3%
Average Efficiency	$\eta_{(5\ V)}$		88.9		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(5\ V)}$			15	W	
9 V Setting						
Output Voltage	$V_{OUT(9\ V)}$		9.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(9\ V)}$			150	mV	Measured at End of 100 mΩ Cable. (20 MHz Bandwidth).
Output Current	$I_{OUT(9\ V)}$			3	A	±3%
Average Efficiency	$\eta_{(9\ V)}$		89.8		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(9\ V)}$			27	W	
3.3 V – 11 V PPS Setting						
Output Voltage	$V_{OUT(PPS)}$	3.3		11	V	±3%
Output Voltage Ripple	$V_{RIPPLE(PPS)}$			150	mV	Measured at the End of 100 mΩ Cable. (20 MHz Bandwidth).
Output Current	$I_{OUT(PPS)}$			3	A	±3%
PPS Voltage Step	$V_{STEP(PPS)}$		20		mV	PPS Output Voltage Step Size.
PPS Current Step	$I_{STEP(PPS)}$		50		mA	PPS Operating Current Step Size.
Average Efficiency (3.3 V)	$\eta_{(3.3\ V)}$		86.7		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Average Efficiency (11 V)	$\eta_{(11\ V)}$		89.8		%	
Continuous Output Power	$P_{OUT(PPS)}$			27	W	
Conducted EMI		Meets CISPR22B / EN55022B				
Ambient Temperature	T_{AMB}	0		40	ºC	Free Convection, Sea Level.

Note: To use this design for a charger/adapter, circuit board would need to be modified depending on shape and form factor of the housing. ESD and Line surge performance should be evaluated and layout adjusted to meet the target specification.

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3 Schematic [Part A - Mother Board]

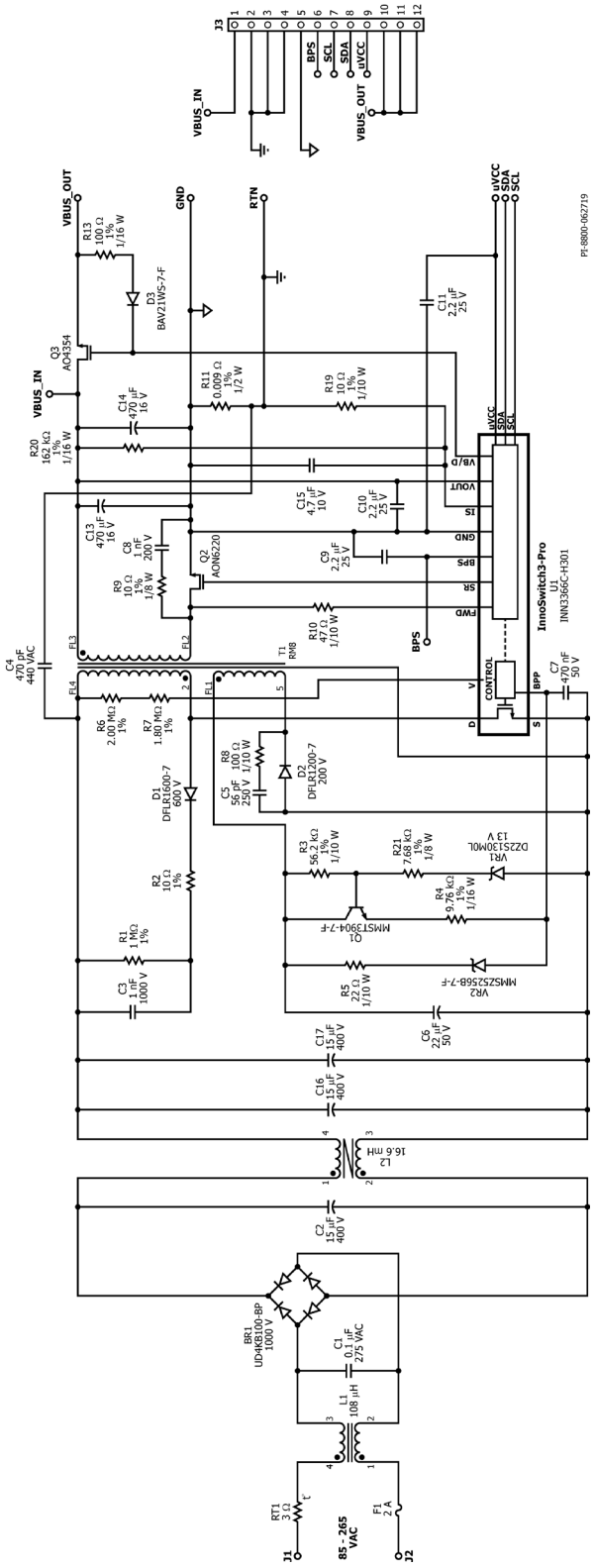

Figure 6 – Schematic of Mother Board.

4 Schematic [Part B - Daughter Board]

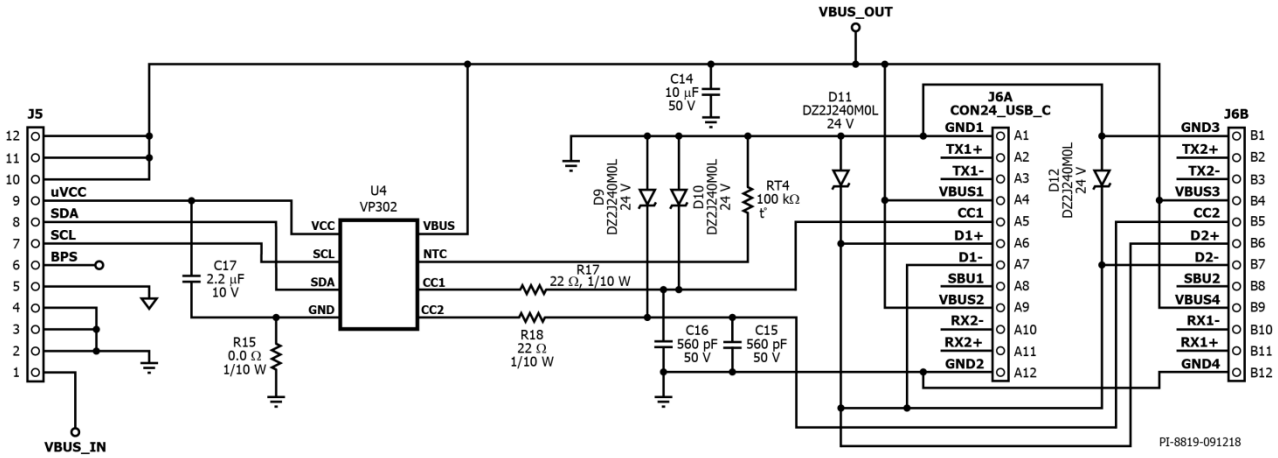

Figure 7 – Schematic of Daughter Board.

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5 Circuit Description

5.1 Mother Board Circuit Description

5.1.1 Input Rectifier and Filter

Fuse F1 isolates the circuit to provide protection from component failure, and the thermistor RT1 limits the inrush current when the unit is connected to the input AC supply. Capacitor C1 and common mode choke L1 provide differential and common mode noise filtering for EMI attenuation. Bridge rectifier BR1 rectifies the AC line voltage to have a full wave rectified DC, which is passed to a pi-filter consisting of C2, L2, and C16 and C17. This filter also provides differential and common mode noise filtering to further attenuate EMI.

5.1.2 InnoSwitch3-Pro IC Primary

One end of the transformer primary is connected to the rectified DC bus and the other end is connected to the drain terminal of the MOSFET inside the InnoSwitch3-Pro IC U1. Resistors R6 and R7 provide input voltage sensing for protection in case of AC input undervoltage or overvoltage.

A low-cost RCD clamp formed by diode D1, resistors R2, R1 and capacitor C3 limits the peak drain-source voltage of U1 at the instant the MOSFET inside U1 turns off. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor C7 when AC is first applied. During normal operation the primary side block is powered from an auxiliary winding on the transformer T1. The output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C6. Resistor R4 limits the current being supplied to the BPP pin of the InnoSwitch3-Pro IC U1. A linear regulator comprising resistor R3, R21, BJT Q1 and Zener diode VR1 ensures sufficient current flows through R4 such that the internal current source of U1 is not required to charge C7 during normal operation. The RC network comprising of resistor R8 and capacitor C5 offers damping of the high frequency ringing in the voltage across diode D2 to reduce radiated EMI.

Zener diode VR2 offers primary sensed output overvoltage protection. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at output of the converter, the auxiliary winding voltage increases and causes breakdown of VR2 which then causes excess current to flow into the BPP pin of InnoSwitch3-Pro IC U1. If the current flowing into the BPP pin increases above the I_{SD} threshold, the InnoSwitch3-Pro controller will latch off and prevent any further increase in output voltage. Resistor R5 limits the current injected to BPP pin.

5.1.3 InnoSwitch3-Pro IC Secondary

The secondary-side of the InnoSwitch3-Pro IC provides output voltage and current sensing and a gate drive to a MOSFET for synchronous rectification. The voltage across the transformer secondary winding is rectified by the secondary-side MOSFET (or SR FET) Q2 and filtered by capacitors C13 and C14. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via a RC snubber, R9 and C8.

The gate of Q2 is turned on by secondary-side controller inside IC U1, based on the secondary winding voltage sensed via resistor R10 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the SR FET is turned off just prior to the secondary-side commanding a new switching cycle from the primary. In discontinuous mode of operation, the SR FET is turned off when the magnitude of the voltage drop across the SR FET falls below a threshold of approximately $V_{SR(TH)}$. Secondary-side control of the primary-side power MOSFET avoids any possibility of cross conduction of the two MOSFETs and provides extremely reliable synchronous rectifier operation.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C9 connected to the BPS pin of InnoSwitch3-Pro IC U1 provides decoupling for the internal circuitry.

The output current is sensed by monitoring the voltage drop across resistor R11. Resistors R19 and R20 add an offset to the sensed output current to provide a positive slope to the CC characteristic. The resulting current measurement is filtered with decoupling capacitor C15 and monitored across the IS and SECONDARY GROUND pins. An internal current sense threshold which is configured via the I^2C interface up to approximately 32 mV is used to reduce losses. Once the threshold is exceeded, the InnoSwitch3-Pro IC U1 regulates the number of switch pulses to maintain a fixed output current.

During constant current (CC) operation, when the output voltage falls, the secondary side controller inside InnoSwitch3-Pro IC U1 will power itself from the secondary winding directly. During the on-time of the primary-side power MOSFET, the forward voltage that appears across the secondary winding is used to charge the SECONDARY BYPASS pin decoupling capacitor C9 via resistor R10 and an internal regulator. This allows output current regulation to be maintained down to the minimum UV threshold. Below this level the unit enters auto-restart until the output load is reduced. Capacitor C10 is needed between the VOUT pin and the SECONDARY GROUND pin for ESD protection of the VOUT pin.

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When the output current is below the CC threshold, the device operates in constant voltage mode. The output voltage is monitored by the VOUT pin of the InnoSwitch3-Pro IC. Similar with current regulation, the output voltage is also compared to an internal voltage threshold that is set via the I^2C interface and the controller inside IC U1 regulates the output voltage by controlling the number of switch pulses.

N-MOSFET Q3 functions as the bus switch which connects or disconnects the output of the flyback converter from the USB Type-C receptacle. Q3 is controlled by the VB/D pin on the InnoSwitch3-Pro IC. Resistors R13 and diode D3 are connected across the Source and Gate terminals of Q3 to provide a discharge path for the bus voltage across C14 on the daughter board when Q3 is turned off.

5.2 Daughter Board Circuit Description

5.2.1 USB Type-C and PD Interface

In this design, VP302 (U4) is the USB Power Delivery (USB PD) controller. It is powered by the InnoSwitch3-Pro IC through the µVCC pin. USB PD protocol is communicated over either CC1 or CC2 line depending on the orientation in which Type-C plug is connected.

VP302 communicates with InnoSwitch3-Pro IC through the I^2C interface using the SCL and SDA lines in which it sets the CV, CC, V_{kp}, OVA and UVA parameters. These parameters correspond to the output voltage, constant output current, constant output power voltage threshold, output overvoltage threshold, and output undervoltage threshold registers of the InnoSwitch3-Pro IC, respectively. The status of the InnoSwitch3-Pro IC is read by the VP302 IC from the telemetry registers also using the I^2C interface.

Capacitor C17 provides decoupling to VCC of the VP302 IC. Capacitors C15 and C16, resistors R17, R18, and TVS D9, D10, D11, and D12 provide protection from ESD to pins CC1, CC2, D1 and D2.

Thermistor RT4 is connected to the NTC pin of the VP302 IC to provide temperature detection of the USB Type-C receptacle. The VBUS pin of the VP302 IC is used to sense the output voltage at the USB Type-C receptacle, which is the voltage after the bus switch Q3. The VBUS pin is also used for discharging the capacitor C14 on the daughter board when the bus switch Q3 is opened.

Resistors R14 and R15 in the daughter board are place holders for connecting the ground of VP302 to the ground of the InnoSwitch3-Pro IC depending on the need. In order to get better eye diagram in the USB PD3.0 tests, R15 should be populated and R14 should not be populated.

6 PCB Layout

PCB copper thickness is 2.0 oz for both mother board and daughter board.

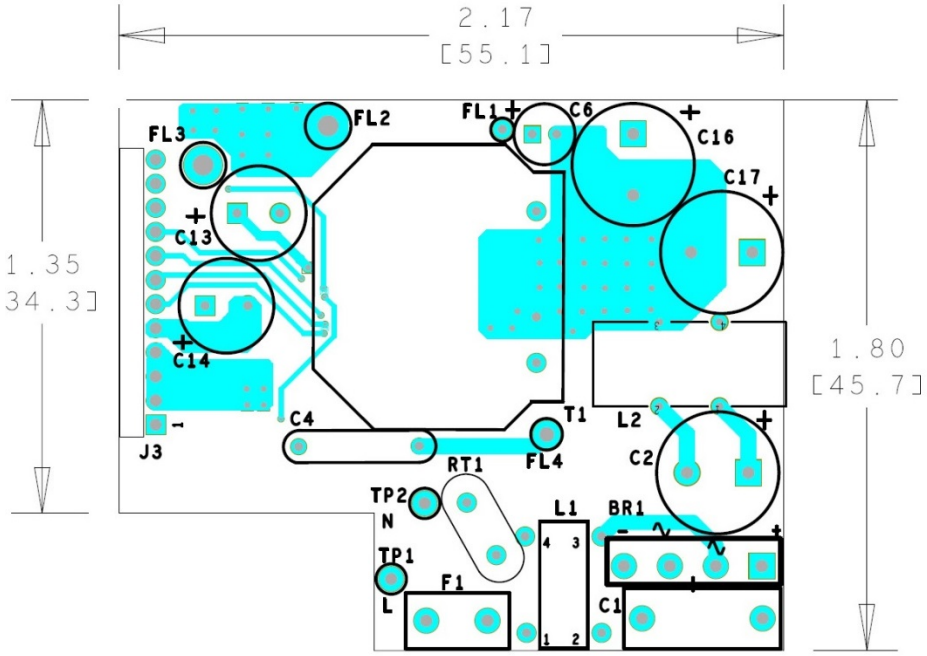

Figure 8 – Printed Circuit Layout, Mother Board, Top.

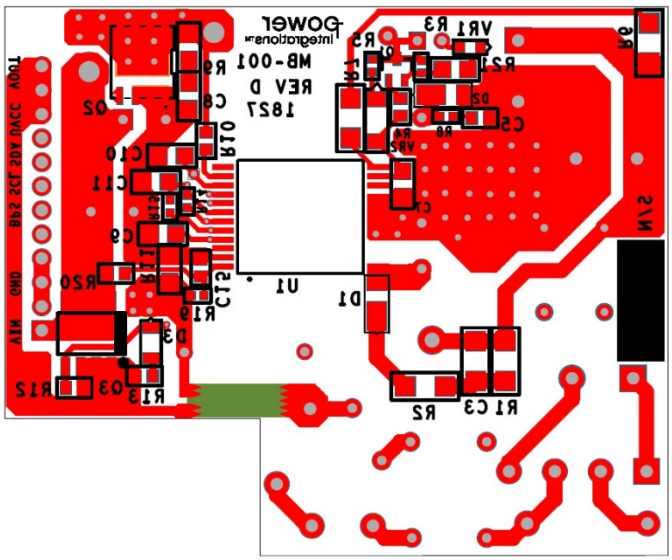

Figure 9 – Printed Circuit Layout, Mother Board, Bottom.

Note: Component references R12, R14, R15, and J3, although present in the layout, are not to be populated when used with a daughter board.

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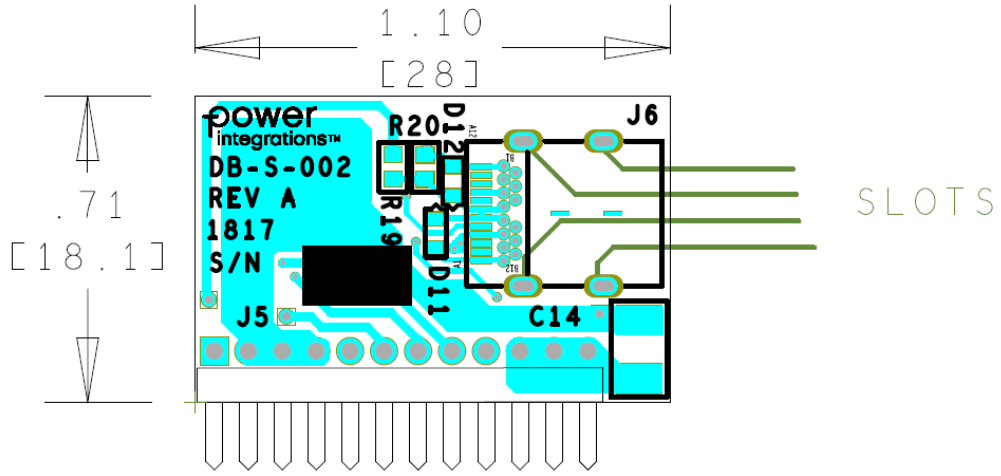

Figure 10 – Printed Circuit Layout, Daughter board, Top.

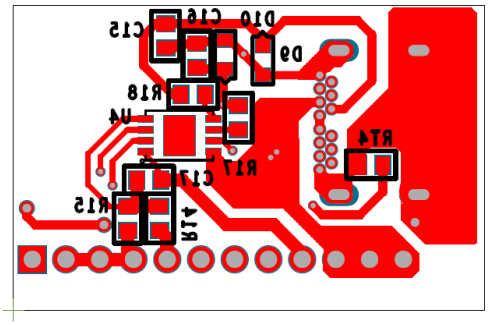

Figure 11 – Printed Circuit Layout, Daughter Board, Bottom.

Note: Component reference R14, R19, and R20, although present in the layout, are not to be populated.

7 Bill of Materials

7.1 Mother Board

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	Bridge Rectifier, 1000 V, 4 A, 4-ESIP, D3K, -55°C ~ 150°C (TJ), Vf = 1 V @ 7.5 A	UD4KB100-BP	Micro Commercial
2	1	C1	0.1 μF, 20% , 275 VAC, 560 VDC, X2, -40°C ~ 110°C, 5 mm W x 13 mm L x 11.1 mm H	R46KF310000P1M	KEMET
3	3	C2 C16 C17	15 μF, 400 V, Electrolytic, (10 x 16)	UVC2G150MPD	Nichicon
4	1	C3	1 nF, 1000 V, Ceramic, X7R, 1206	CC1206KKX7RCBB102	Yageo
5	1	C4	470 pF, ±10%, 440VAC, (X1, Y2) rated, Ceramic Capacitor, Y5S, Radial, Disc, -40°C ~ 125°C	VY2471K29Y5SS63V7	Vishay
6	1	C5	56 pF, 250 V, Ceramic, NP0, 0603	GQM1875C2E560JB12D	Murata
7	1	C6	22 μF, 50 V, Electrolytic, (5 x 11)	UPW1H220MDD	Nichicon
8	1	C7	470 nF, 50 V, Ceramic, X7R, 0805	GRM21BR71H474KA88L	Murata
9	1	C8	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
10	3	C9 C10 C11	2.2 μF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
11	2	C13 C14	470 μF, 16 V,Al Organic Polymer, 12 mOhm, (8 x 11.5)	RNE1C471MDN1	Nichicon
12	1	C15	4.7 μF, 10 V, Ceramic, X5R, 0603	C1608X5R1A475M/0.50	TDK
13	1	D1	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes, Inc.
14	1	D2	200 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1200-7	Diodes, Inc.
15	1	D3	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
16	1	F1	2 A, 250 V, Slow, Long Time Lag, RST	RST 2	Belfuse
17	1	L1	Toroidal Common Mode Choke, 108 μH, custom	32-00369-00	Power Integrations
18	1	L2	Toroidal Common Mode Choke, 16.6 mH, custom	32-00368-00	Power Integrations
19	1	Q1	NPN, Small Signal BJT, 40 V, 0.2 A, SOT-323	MMST3904-7-F	Diodes, Inc.
20	1	Q2	MOSFET, N-CH, 100V, 48A (Tc), 113.5 W (Tc), DFN5X6, 8-DFN (5x6)	AON6220	Alpha & Omega Semi.
21	1	Q3	MOSFET, N-CH, 30 V, 23 A (Ta), 3.1 W (Ta), 3.7 mΩ (@ 20 A, 10 V), 8SOIC	AO4354	Alpha & Omega Semi.
22	1	R1	RES, 1 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ105V	Panasonic
23	1	R2	RES, 10 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF10R0V	Panasonic
24	1	R3	RES, 56.2 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF5622X	Panasonic
25	1	R4	RES, 9.76 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF9761V	Panasonic
26	1	R5	RES, 22 Ω, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ220X	Panasonic
27	1	R6	RES, 2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
28	1	R7	RES, 1.80 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1804V	Panasonic
29	1	R8	RES, 100 Ω, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ101X	Panasonic
30	1	R9	RES, 10 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF10R0V	Panasonic
31	1	R10	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
32	1	R11	RES, 0.009 Ω, 0.5 W, 1%, 0805	CRF0805-FZ-R009ELF	Bourns
33	1	R13	RES, 100 Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1000V	Panasonic
34	1	R19	RES, 10 Ω, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF10R0X	Panasonic
35	1	R20	RES, 162 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1623V	Panasonic
36	1	R21	RES, 7.68 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF7681V	Panasonic
37	1	RT1	NTC Thermistor, 3 Ω, 5 A	SCK10035LSY	Thinking Electronics
38	1	T1	Flyback Transformer, 570 μH, RM8, PC95 material, custom Bobbin, RM8, Vertical, 12 pins	 P-803	Power Integrations Pin Shine
39	1	TP1	Test Point, BLK, Mini THRU-HOLE MOUNT	5001	Keystone

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40	1	TP2	Test Point, WHT, Mini THRU-HOLE MOUNT	5002	Keystone
41	1	U1	InnoSwitch3-Pro, InSOP24D	INN3366C-H301	Power Integrations
42	1	VR1	13 V, 5%, 150 mW, SSMINI-2	DZ2S130M0L	Panasonic
43	1	VR2	DIODE ZENER 30 V 500 mW SOD123	MMSZ5256B-7-F	Diodes, Inc.

7.2 Daughter Board

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	C14	10 μF, 35 V, Ceramic, X7R, 1210	CL32B106KLJNNNE	Samsung
2	2	C15 C16	560 pF, 50 V, Ceramic, X7R, 0603, 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	CL10B561KB8NNNC	Samsung
3	1	C17	2.2 μF, 10 V, Ceramic, X5R, 0603	GRM188R61A225KE34D	Murata
4	4	D9 D10 D11 D12	DIODE, ZENER, 24 V, 200 mW, SMINI2	DZ2J240M0L	Panasonic
5	1	J5	15 Position (1 x 15) header, 2 mm pitch, Right Angle	NRPN151PARN-RC	Sullins Connector
6	1	J6	USB - C USB 3.1 (USB 3.1 Gen 2, Superspeed+) Receptacle Connector 24 Pos SMT, RA, TH	632723300011	Wurth
7	1	R15	RES, 0 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEY0R00V	Panasonic
8	2	R17 R18	RES, 22 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ220V	Panasonic
9	1	RT4	NTC Thermistor, 100 kΩ, 3%, 0603	NCP18WF104E03RB	Murata
10	1	U4	USB Type-C Power Delivery Controller for SMPS	VP302	VIA Labs

8 Transformer Specification

8.1 Electrical Diagram

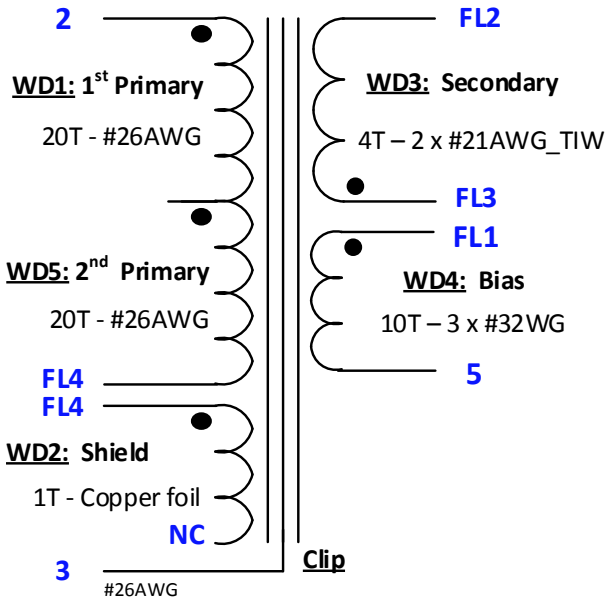

Figure 12 – Transformer Electrical Diagram.

8.2 Electrical Specifications

Electrical Strength	60 seconds, 60 Hz, from pins 2, 5, FL1, FL4 to FL2-FL3.	3000 VAC
Primary Inductance	Pin 2 - FL4, all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	570 µH, ±7%
Resonant Frequency	Pin 2 - FL4, all other windings open.	2000 kHz (Min.)
Primary Leakage Inductance	Pin 2 - FL4, with FL2 - FL3 shorted, measured at 100 kHz, 0.4 V_{RMS}.	8.0 µH (Max.)

8.3 Material List

Item	Description
[1]	Core: RM8, TDK-PC45; or Equivalent. Gapped ALG: 356nH/T².
[2]	Bobbin: RM8-V-12(6/6), in-line, PI#: 25-00041-00; or Equivalent. See Figure 14 to Modify the Bobbin.
[3]	Clip: RM8, Allstar Magnetic, CLI/P-RM8/I; or Equivalent.
[4]	Magnet Wire: #26 AWG, Double Coated.
[5]	Magnet Wire: #32 AWG, Double Coated.
[6]	Magnet Wire: #21 AWG, Triple Insulated Wire.
[7]	Tape: Polyester Film, 3M, 1 mil Thick, 9.3 mm Wide.
[8]	Tape: Polyester Film, 3M, 1 mil Thick, 33.0 mm x 54.0 mm
[9]	Copper Foil: Copper Tape; 8.6 mm width x 38.0 mm Length x 1 mil Thick, Soldered with Magnetic Wire #26 AWG at one End.
[10]	Varnish: Dolph BC 359; or Equivalent.

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8.4 Transformer Build Diagram

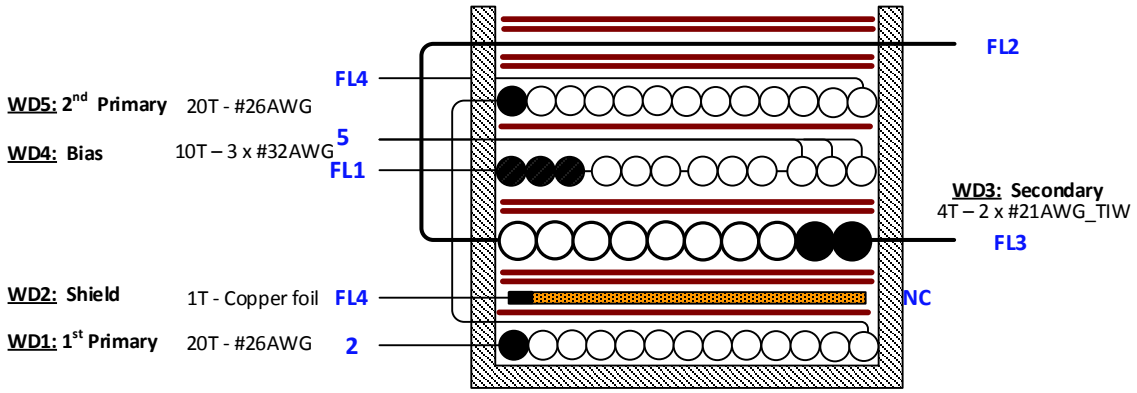

Figure 13 – Transformer Build Diagram.

8.5 Transformer Construction

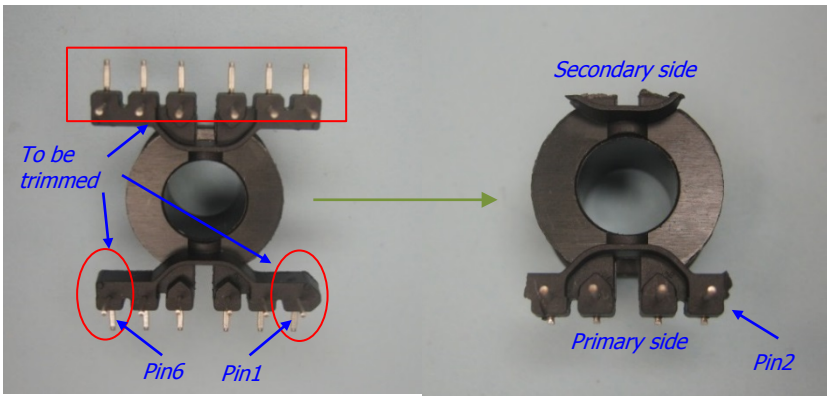

Figure 14 – Modify the Bobbin.

Winding Preparation	Trim secondary flange of bobbin Item [2] to match top flange. Trim off the portions at pin 1 and pin 6 of primary flange. Cut off all side pins on primary flange, (see Figure 14). Position this bobbin on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.
WD1 1st Primary	Start at pin 2, wind 20 turns of wire Item [4] in 1 layer, with tight tension, from left to right. At the last turn bring the wire back to the left and leave 3ft of wire for 2nd half primary winding – WD5.
Insulation	1 layer of tape Item [7].
WD2 Shield	Use copper Item [9], start as FL4 with the wire which is soldered to the copper foil, wind 1 turn overlapped but not shorted.
Insulation	2 layers of tape Item [7].
WD3 Secondary	Use 2 wires Item [6], leave ~30 mm floating, and mark as FL3. Start from the right slot on the secondary side of the bobbin, wind 4 turns with tight tension in 1 layer. At the last turn, exit the wires at the left slot on the secondary side of the bobbin and leave ~ 40mm as FL2.

Insulation	2 layers of tape Item [7].
WD4 Bias	Use 3 wires Item [5], leave ~ 20 mm marked as FL1, wind 10 turns in 1 layer, from left to right, spread the wires evenly across the bobbin. At the last turn bring the wires back to the left and finish at pin 5.
Insulation	1 layer of tape Item [7].
WD5 2nd Primary	Use wire floating from WD1 - 1st Primary; continue winding 20 turns from left to right. At the last turn, bring the wire back to left, leave ~20 mm floating, and mark as FL4.
Insulation	Apply 2 layers of tape Item [7], bring wires floating FL2 from WD3 - Secondary to the right, and apply another 2 layers of tape Item [7] (total of 4 layers) to secure all windings.
Gap and Ground Core	Gap core halves to 570 μH, secure with clips Item [3] with GND pins on bottom and cut short. Solder Item [4] to the top of one clip then and connect the other end of the wire to pin 3, which is connected to primary ground in the PCB.
Finish	Place 2 layers of tape Item [8] at bottom core of transformer and wrap. Ensure that the tape covers the core and bobbin on the secondary side, then wrap another 2 turns of tape Item [7] around the body of transformer. Varnish with Item [10].

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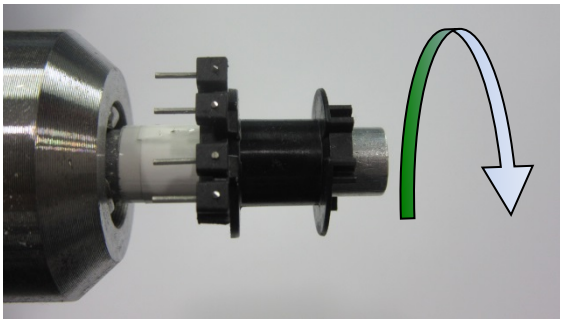
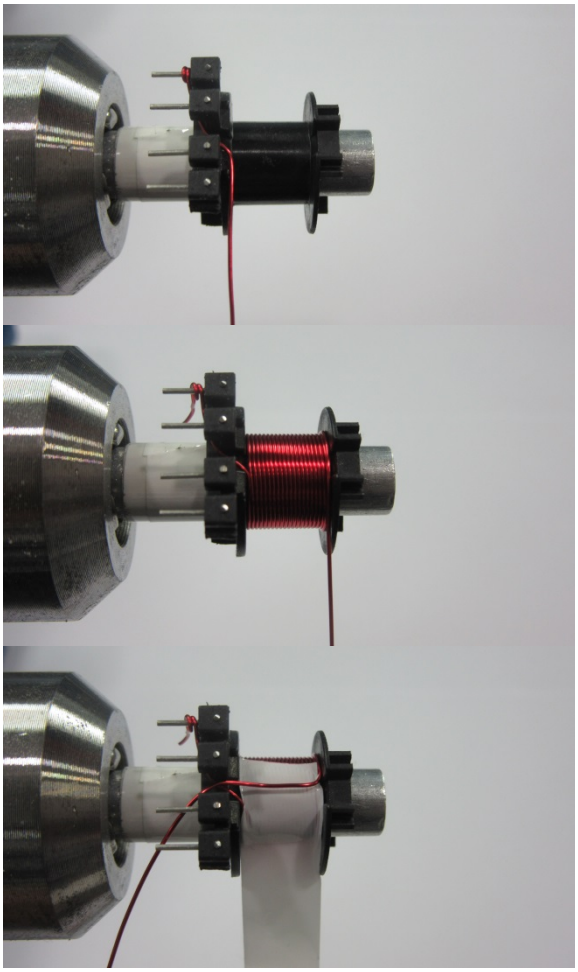
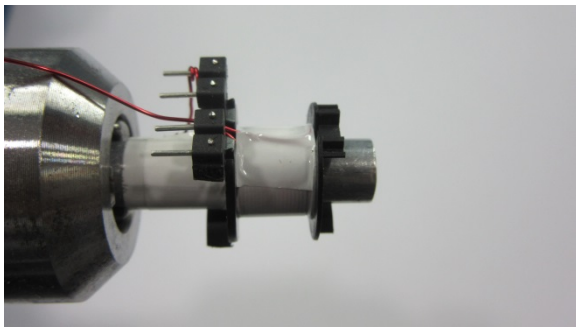
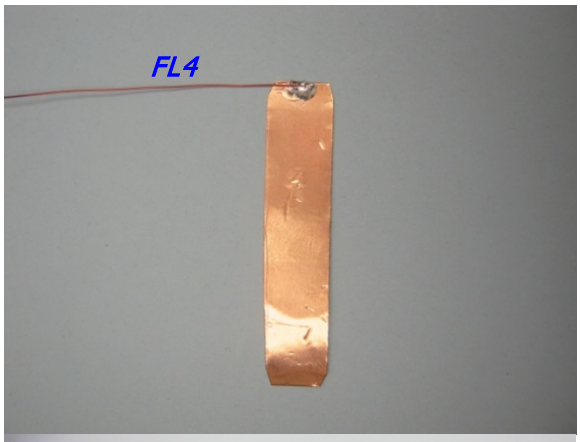
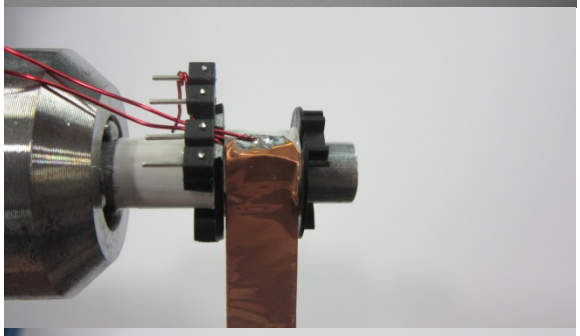
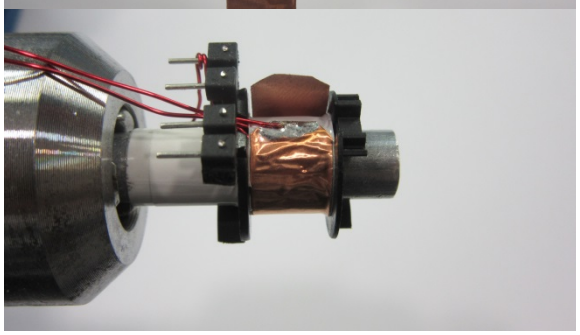
8.6 Winding Illustrations

Winding Preparation		Position the modified bobbin (Figure 14) on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.
WD1 **1st Primary**		Start at pin 2, wind 20 turns of wire Item [4] in 1 layer, with tight tension, from left to right. At the last turn bring the wire back to the left and leave 3ft of wire for 2nd half primary winding – WD5.

Insulation		1 layer of tape Item [7].
WD2 **Shield**	  	Prepare copper foil Item [9], start as FL4 with the wire which is soldered to the copper foil, wind 1 turn overlapped but not shorted.

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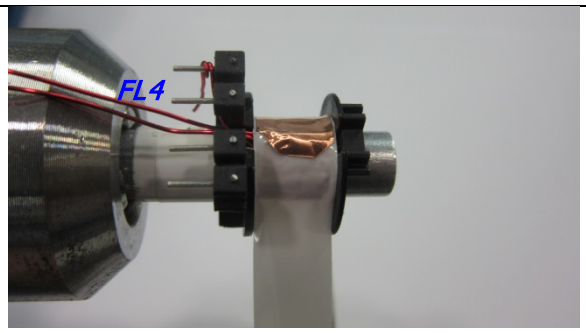
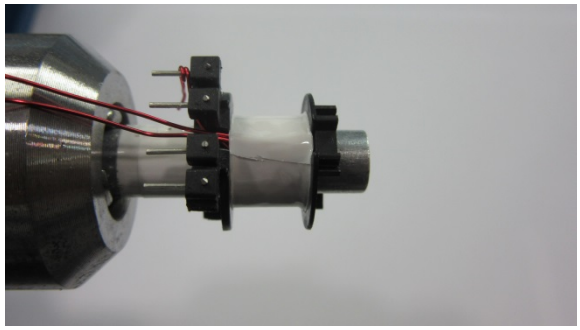
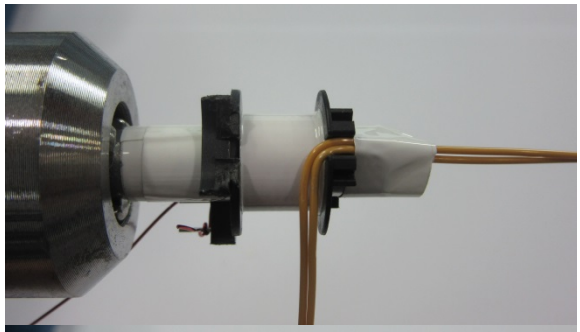
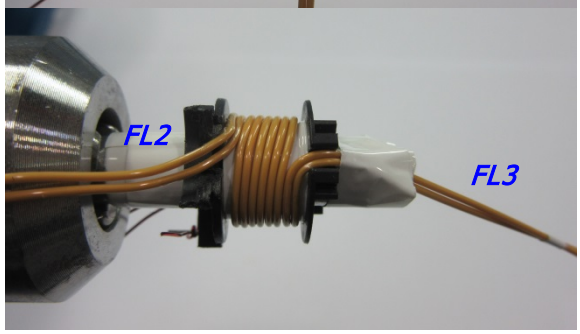
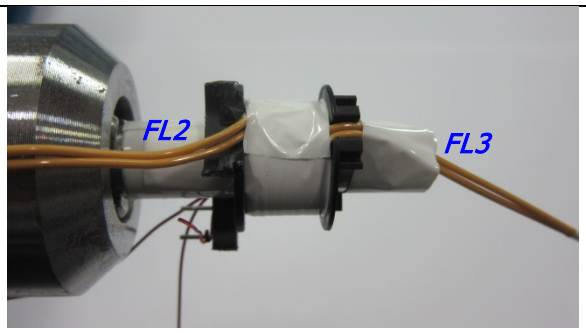
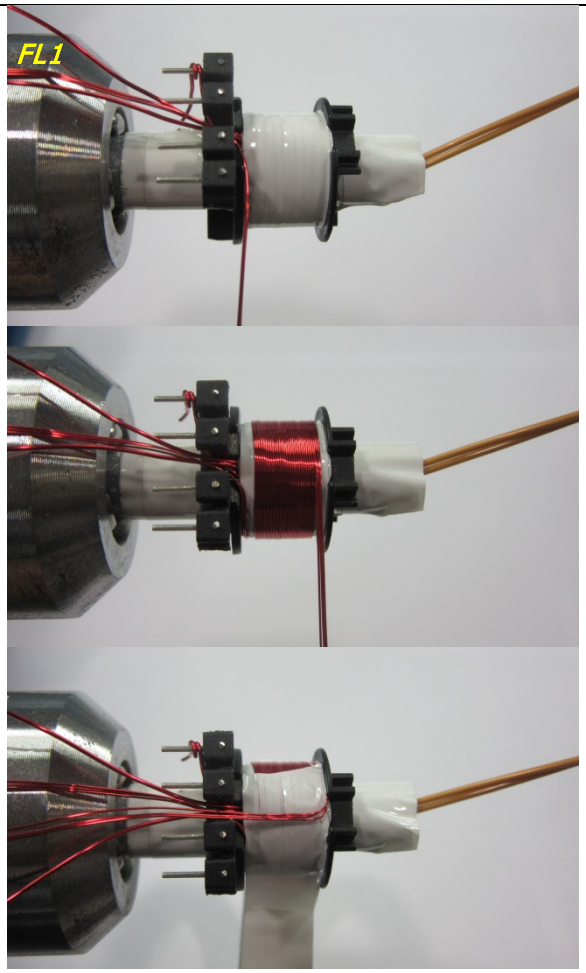
		
Insulation		2 layers of tape Item [7].
WD3 **Secondary**	 	Use 2 wires Item [6], leave ~30 mm floating, and mark as FL3. Start from the right slot on the secondary side of the bobbin, wind 4 turns with tight tension in 1 layer. At the last turn, exit the wires at the left slot on the secondary side of the bobbin and leave ~ 40mm as FL2.

Insulation		2 layers of tape Item [7].
WD4 **Bias**		Use 3 wires Item [5], leave ~20 mm marked as FL1, wind 10 turns in 1 layer, from left to right, spread the wires evenly across the bobbin. At the last turn bring the wires back to the left and finish at pin 5.

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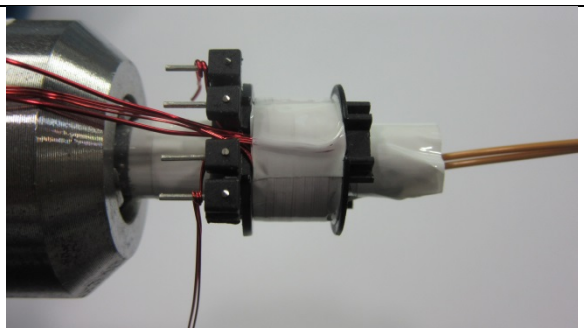
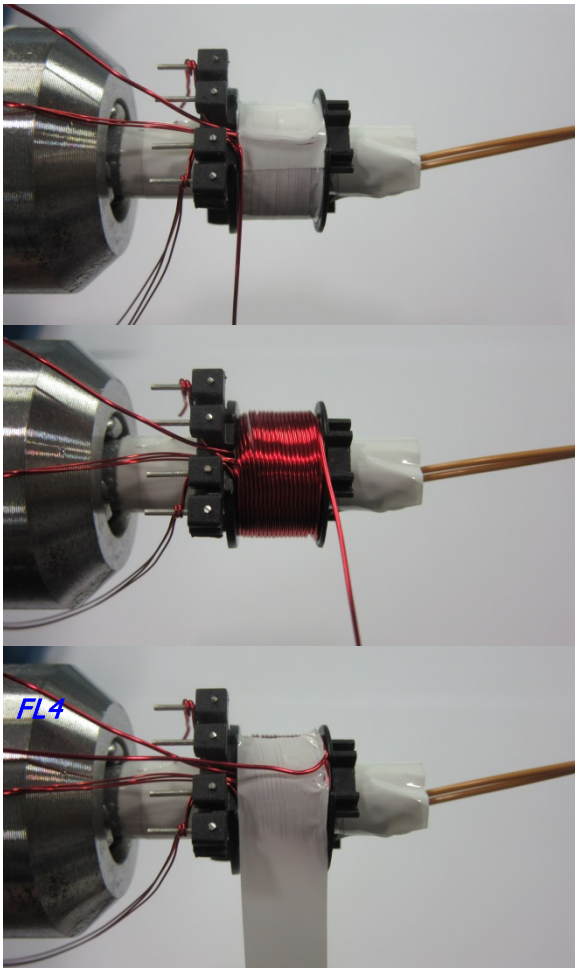
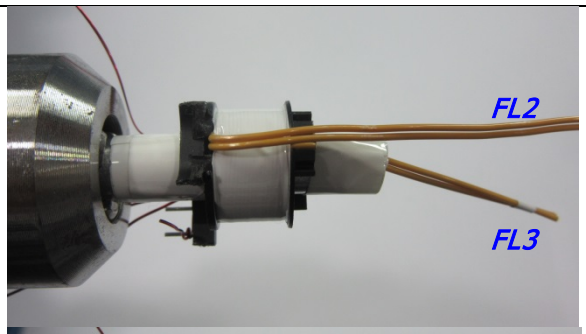
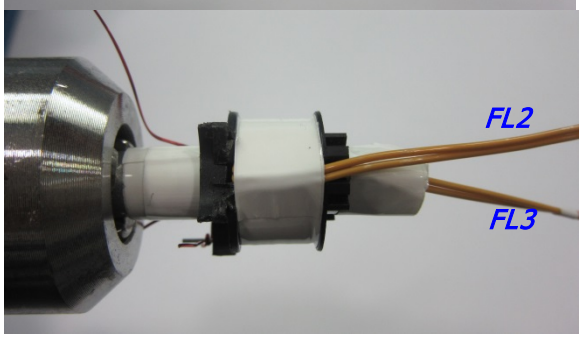
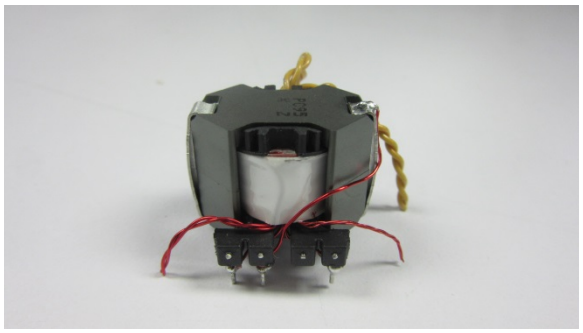
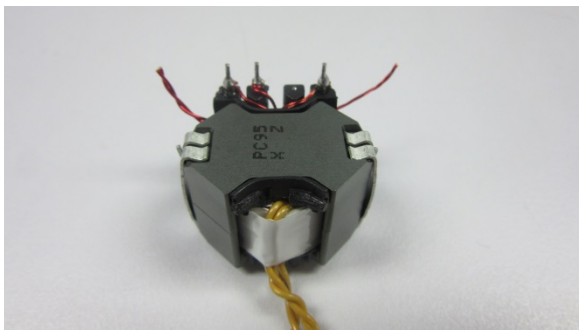
Insulation		1 layer of tape Item [7].
WD5 **2nd Primary**		Use wire floating from WD1-1st Primary; continue winding 20 turns from left to right. At the last turn, bring the wire back to left, leave ~20 mm floating, and mark as FL4.

Insulation	 	Apply 2 layers of tape Item [7], bring wires floating FL2 from WD3-Secondary to the right and apply another 2 layers of tape Item [7] (total of 4 layers) to secure all windings.
Gap and Ground Core		Gap core halves to 570 µH, secure with clips Item [3] with GND pins on bottom and cut short. Solder Item [4] to the top of one clip then and connect the other end of the wire to pin 3, which is connected to primary ground in the PCB.
Finish		Place 2 layers of tape Item [8] at bottom core of transformer and wrap. Ensure that the tape covers the core and bobbin on the secondary-side, then wrap another 2 turns of tape Item [7] around the body of transformer. Varnish with Item [10].

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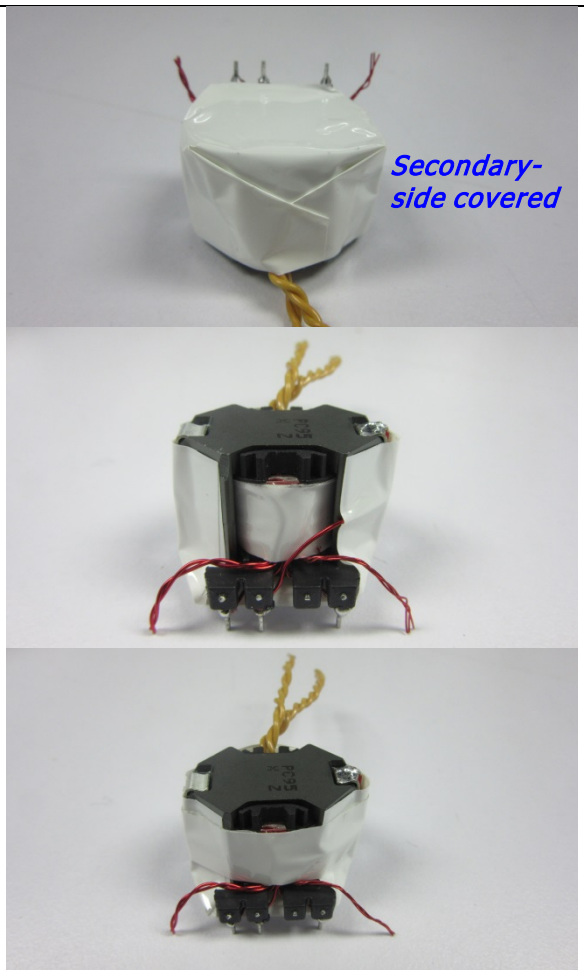
Secondary-
side covered

9 Common Mode Choke Specifications

9.1 108 μH Common Mode Choke (L1)

9.1.1 Electrical Diagram

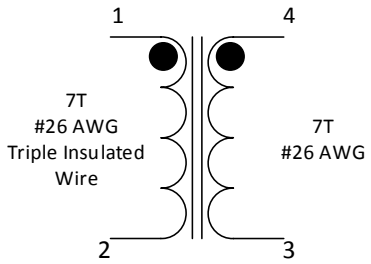

Figure 15 – Inductor Electrical Diagram.

9.1.2 Electrical Specifications

Inductance	Pins 1-2 measured at 100kHz, 0.4 RMS.	108 μH ±20%
Leakage Inductance	Pins 1-2, with 3-4 shorted.	0.5 μH ±10%

9.1.3 Material List

Item	Description
[1]	Toroid: Ferrite Inductor Toroid. 415" OD; Mfg Part Number: 35T0375-10H. Dim: 9.53 mm, O.D. x 4.75 mm, I.D. x 3.18 mm L.
[2]	Magnet Wire: #26 AWG, Double Coated.
[3]	Magnet Wire: #26 AWG, Triple Insulated Wire.

9.1.4 Winding Illustration

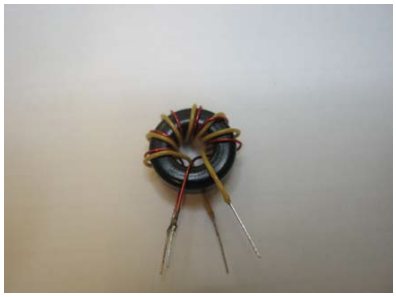

Figure 16 – 108 μH CMC L1 Front View.

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9.2 16.6 mH Common Mode Choke (L2)

9.2.1 Electrical Diagram

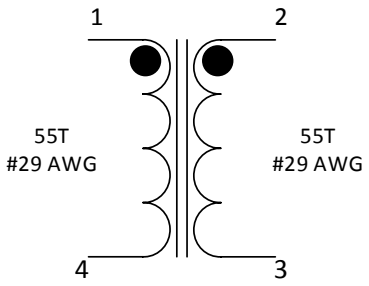

Figure 17 – Inductor Electrical Diagram.

9.2.2 Electrical Specifications

Inductance	Pins 1-4 and pins 2-3 measured at 100 kHz, 0.4 RMS.	16.6 mH ± 25%
Core effective Inductance Index		5500 nH/N^2
Leakage Inductance	Pins 1-4, with 2-3 shorted.	80 µH ± 10%

9.2.3 Materials List

Item	Description
[1]	Toroid: Ferrite Inductor Toroid T14 x 8 x 5.5, PI#: 32-00286-00.
[2]	Divider: Cable tie, Panduit - Fish Paper, Insulating Cotton Rag, 0.010” Thick, PI #: 66-00042-00.
[3]	Magnet Wire: #29 AWG Heavy Nyleze.
[4]	Epoxy: Devon, 5 mins Epoxy; or equivalent.

9.2.4 Winding Instructions

- Place 2 pieces of cable tie item [2] on to toroid item [1] to divide 2 equal sections.
- Use 4 ft of wire item [3], start as 1, wind 55 turns in 2 layers in one toroid half, and end as 4.
- Do the same for another half of the toroid. Start as 2 and end as 3.
- Pull up 2 notches of cable ties to be in line with toroid body (to save space), and apply Epoxy item [4] where leads floating.

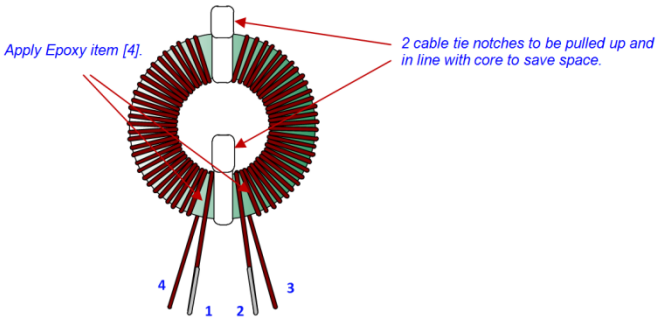

Figure 18 – 16.6 mH CMC L2 Front View.

10 Transformer Design Spreadsheet

1	ACDC_InnoSwitch3-Pro_Flyback_042018; Rev.1.0; Copyright Power Integrations 2018	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-Pro Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	VAC_MIN	85		85	V	Minimum AC line voltage
4	VAC_MAX			265	V	Maximum AC input voltage
5	VAC_RANGE			UNIVERSAL		AC line voltage range
6	FLINE			60	Hz	AC line voltage frequency
7	CAP_INPUT	45.0		45.0	uF	Input capacitance
9	**SETPOINT 1**					
10	VOUT1	11.00		11.00	V	Output voltage 1, should be the highest output voltage required
11	IOUT1	2.450		2.450	A	Output current 1
12	POUT1			26.95	W	Output power 1
13	EFFICIENCY1	0.89		0.89		Converter efficiency for output 1
14	Z_FACTOR1	0.50		0.50		Z-factor for output 1
16	**SETPOINT 2**					
17	VOUT2	9.00		9.00	V	Output voltage 2
18	IOUT2	3.000		3.000	A	Output current 2
19	POUT2			27.00	W	Output power 2
20	EFFICIENCY2	0.89		0.89		Converter efficiency for output 2
21	Z_FACTOR2	0.50		0.50		Z-factor for output 2
23	**SETPOINT 3**					
24	VOUT3	5.00		5.00	V	Output voltage 3
25	IOUT3	3.000		3.000	A	Output current 3
26	POUT3			15.00	W	Output power 3
27	EFFICIENCY3	0.89		0.89		Converter efficiency for output 3
28	Z_FACTOR3	0.50		0.50		Z-factor for output 3
30	**SETPOINT 4**					
31	VOUT4	3.00		3.00	V	Output voltage 4
32	IOUT4	3.000		3.000	A	Output current 4
33	POUT4			9.00	W	Output power 4
34	EFFICIENCY4	0.85		0.85		Converter efficiency for output 4
35	Z_FACTOR4	0.50		0.50		Z-factor for output 4
37	**SETPOINT 5**					
38	VOUT5			0.00	V	Output voltage 5
39	IOUT5			0.000	A	Output current 5
40	POUT5			0.00	W	Output power 5
41	EFFICIENCY5			0.00		Converter efficiency for output 5
42	Z_FACTOR5			0.00		Z-factor for output 5
44	**SETPOINT 6**					
45	VOUT6			0.00	V	Output voltage 6
46	IOUT6			0.000	A	Output current 6
47	POUT6			0.00	W	Output power 6
48	EFFICIENCY6			0.00		Converter efficiency for output 6
49	Z_FACTOR6			0.00		Z-factor for output 6
51	**SETPOINT 7**					
52	VOUT7			0.00	V	Output voltage 7
53	IOUT7			0.000	A	Output current 7
54	POUT7			0.00	W	Output power 7
55	EFFICIENCY7			0.00		Converter efficiency for output 7
56	Z_FACTOR7			0.00		Z-factor for output 7
58	**SETPOINT 8**					
59	VOUT8			0.00	V	Output voltage 8
60	IOUT8			0.000	A	Output current 8
61	POUT8			0.00	W	Output power 8
62	EFFICIENCY8			0.00		Converter efficiency for output 8
63	Z_FACTOR8			0.00		Z-factor for output 8

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65	**SETPOINT 9**					
66	VOUT9			0.00	V	Output voltage 9
67	IOUT9			0.000	A	Output current 9
68	POUT9			0.00	W	Output power 9
69	EFFICIENCY9			0.00		Converter efficiency for output 9
70	Z_FACTOR9			0.00		Z-factor for output 9
72	VOLTAGE_CDC	0.000		0.000	V	Cable drop compensation desired at full current
76	**PRIMARY CONTROLLER SELECTION**					
77	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
78	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
79	VDRAIN_BREAKDOWN	650		650	V	Device breakdown voltage
80	DEVICE_GENERIC	INN33X6		INN33X6		Device selection
81	DEVICE_CODE			INN3366C		Device code
82	PDEVICE_MAX			27	W	Device maximum power capability
83	RDSON_25DEG			1.50	Ω	Primary MOSFET on-time resistance at 25°C
84	RDSON_100DEG			2.32	Ω	Primary MOSFET on-time resistance at 100°C
85	ILIMIT_MIN			1.162	A	Primary MOSFET minimum current limit
86	ILIMIT_TYP			1.250	A	Primary MOSFET typical current limit
87	ILIMIT_MAX			1.338	A	Primary MOSFET maximum current limit
88	VDRAIN_ON_MOSFET			0.85	V	Primary MOSFET on-time voltage drop
89	VDRAIN_OFF_MOSFET			553.31	V	Peak drain voltage on the primary MOSFET during turn-off
93	**WORST CASE ELECTRICAL PARAMETERS**					
94	FSWITCHING_MAX	85736		85736	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
95	VOR	110.0		110.0	V	Voltage reflected to the primary winding (corresponding to setpoint 1) when the primary MOSFET turns off
96	VMIN			79.20	V	Valley of the rectified minimum input AC voltage at full load
97	KP			0.789		Measure of continuous/discontinuous mode of operation
98	MODE_OPERATION			CCM		Mode of operation
99	DUTYCYCLE			0.584		Primary MOSFET duty cycle
100	TIME_ON			9.76	us	Primary MOSFET on-time
101	TIME_OFF			4.98	us	Primary MOSFET off-time
102	LPRIMARY_MIN			531.4	uH	Minimum primary magnetizing inductance
103	LPRIMARY_TYP			571.4	uH	Typical primary magnetizing inductance
104	LPRIMARY_TOL	7.0		7.0	%	Primary magnetizing inductance tolerance
105	LPRIMARY_MAX			611.4	uH	Maximum primary magnetizing inductance
107	**PRIMARY CURRENT**					
108	IAVG_PRIMARY			0.366	A	Primary MOSFET average current
109	IPEAK_PRIMARY			1.275	A	Primary MOSFET peak current
110	IPEDESTAL_PRIMARY			0.238	A	Primary MOSFET current pedestal
111	IRIPPLE_PRIMARY			1.274	A	Primary MOSFET ripple current
112	IRMS_PRIMARY			0.559	A	Primary MOSFET RMS current
114	**SECONDARY CURRENT**					
115	IPEAK_SECONDARY			12.747	A	Secondary MOSFET peak current
116	IPEDESTAL_SECONDARY			2.384	A	Secondary MOSFET pedestal current
117	IRMS_SECONDARY			5.210	A	Secondary MOSFET RMS current
118	IRIPPLE_CAP_OUT			4.260	A	Output capacitor ripple current
122	**TRANSFORMER CONSTRUCTION PARAMETERS**					

123	**CORE SELECTION**					
124	CORE	RM8	Info	RM8		The transformer windings may not fit: pick a bigger core or bobbin and refer to the Transformer Parameters tab for fit calculations
125	CORE NAME			PC95RM08Z		Core code
126	AE			64.0	mm^2	Core cross sectional area
127	LE			38.0	mm	Core magnetic path length
128	AL			5290	nH	Ungapped core effective inductance per turns squared
129	VE			2430	mm^3	Core volume
130	BOBBIN NAME			B-RM08-V		Bobbin name
131	AW			30.0	mm^2	Bobbin window area
132	BW			8.80	mm	Bobbin width
133	MARGIN			0.0	mm	Bobbin safety margin
135	**PRIMARY WINDING**					
136	NPRIMARY			40		Primary winding number of turns
137	BPEAK			3271	Gauss	Peak flux density
138	BMAX			2994	Gauss	Maximum flux density
139	BAC			1495	Gauss	AC flux density (0.5 x Peak to Peak)
140	ALG			357	nH/N^2	Typical gapped core effective inductance per turns squared
141	LG			0.210	mm	Core gap length
142	LAYERS_PRIMARY	2		2		Primary winding number of layers
143	AWG_PRIMARY			27		Primary wire gauge
144	OD_PRIMARY_INSULATED			0.418	mm	Primary wire insulated outer diameter
145	OD_PRIMARY_BARE			0.361	mm	Primary wire bare outer diameter
146	CMA_PRIMARY			360.5	Cmils/A	Primary winding wire CMA
148	**SECONDARY WINDING**					
149	NSECONDARY	4		4		Secondary winding number of turns
150	AWG_SECONDARY			19		Secondary wire gauge
151	OD_SECONDARY_INSULATED			1.217	mm	Secondary wire insulated outer diameter
152	OD_SECONDARY_BARE			0.912	mm	Secondary wire bare outer diameter
153	CMA_SECONDARY			247.2	Cmils/A	Secondary winding wire CMA
155	**BIAS WINDING**					
156	NBIAS			10		Bias winding number of turns
160	**PRIMARY COMPONENTS SELECTION**					
161	**LINE UNDERVOLTAGE**					
162	BROWN-IN REQURED	76.00		76.00	V	Required line brown-in threshold
163	RLS			3.82	MΩ	Connect two 1.91 MOhm resistors to the V-pin for the required UV/OV threshold
164	BROWN-IN ACTUAL			76.58	V	Actual brown-in threshold using standard resistors
165	BROWN-OUT ACTUAL			69.26	V	Actual brown-out threshold using standard resistors
167	**LINE OVERVOLTAGE**					
168	OVERVOLTAGE_LINE		Warning	319.20	V	The device voltage stress will be higher than 90% of the breakdown voltage when overvoltage is triggered
170	**BIAS WINDING**					
171	VBIAS	7.00	Info	7.00	V	The rectified bias voltage maybe too low to supply the BP pin: Increase the rectified bias voltage to a value higher than 9V
172	VF_BIAS			0.70	V	Bias winding diode forward drop
173	VREVERSE_BIASDIODE			100.33	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
174	CBIAS			22	uF	Bias winding rectification capacitor
175	CBPP			0.47	uF	BPP pin capacitor
179	**SECONDARY COMPONENTS SELECTION**					

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180	**RECTIFIER**					
181	VDRAIN_OFF_SRFET			48.33	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
182	SRFET	Auto		AOD2816		Secondary rectifier (Logic MOSFET)
183	VBREAKDOWN_SRFET			80	V	Secondary rectifier breakdown voltage
184	RDSON_SRFET			29.0	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
188	**VARIABLE OUTPUTS ANALYSIS**					
189	**TOLERANCE CORNER**					
190	CORNER_VAC			85	V	Input AC RMS voltage corner to be evaluated
191	CORNER_ILIMIT	TYP		1.250	A	Current limit corner to be evaluated
192	CORNER_LPRIMARY	TYP		571.4	uH	Primary inductance corner to be evaluated
194	**SETPOINT SELECTION**					
195	SETPOINT	1		1		Select the setpoint which needs to be evaluated
196	FSWITCHING			69826.7	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
197	VOR			110.0	V	Voltage reflected to the primary winding when the primary MOSFET turns off
198	VMIN			79.28	V	Valley of the minimum input AC voltage
199	KP			0.957		Measure of continuous/discontinuous mode of operation
200	MODE_OPERATION			CCM		Mode of operation
201	DUTYCYCLE			0.584		Primary MOSFET duty cycle
202	TIME_ON			8.36	us	Primary controller's maximum on-time
203	TIME_OFF			5.96	us	Primary controller's minimum off-time
205	**PRIMARY CURRENT**					
206	IAVG_PRIMARY			0.365	A	Primary MOSFET average current
207	IPEAK_PRIMARY			1.199	A	Primary MOSFET peak current
208	IPEDESTAL_PRIMARY			0.051	A	Primary MOSFET current pedestal
209	IRIPPLE_PRIMARY			1.148	A	Primary MOSFET ripple current
210	IRMS_PRIMARY			0.540	A	Primary MOSFET RMS current
212	**SECONDARY CURRENT**					
213	IPEAK_SECONDARY			11.987	A	Secondary MOSFET peak current
214	IPEDESTAL_SECONDARY			0.512	A	Secondary MOSFET pedestal current
215	IRMS_SECONDARY			4.564	A	Secondary MOSFET RMS current
216	IRIPPLE_CAP_OUT			3.850	A	Output capacitor ripple current
218	**MAGNETIC FLUX DENSITY**					
219	BPEAK			2856	Gauss	Peak flux density
220	BMAX			2676	Gauss	Maximum flux density
221	BAC			1281	Gauss	AC flux density (0.5 x Peak to Peak)

Note: Although the spreadsheet shows a warning indicating that device voltage stress likely exceeding 90% of the device rating, this voltage will still be safely below the specified voltage breakdown rating of the device and is acceptable since line OV is an abnormal operating condition and hence not expected to be a continuous operating condition.

11 Performance Data

Note 1: Output voltages measured at PCB end.
2: Measurements taken at room temperature.

11.1 Efficiency vs. Load

11.1.1 Output: 3.3 V / 3 A

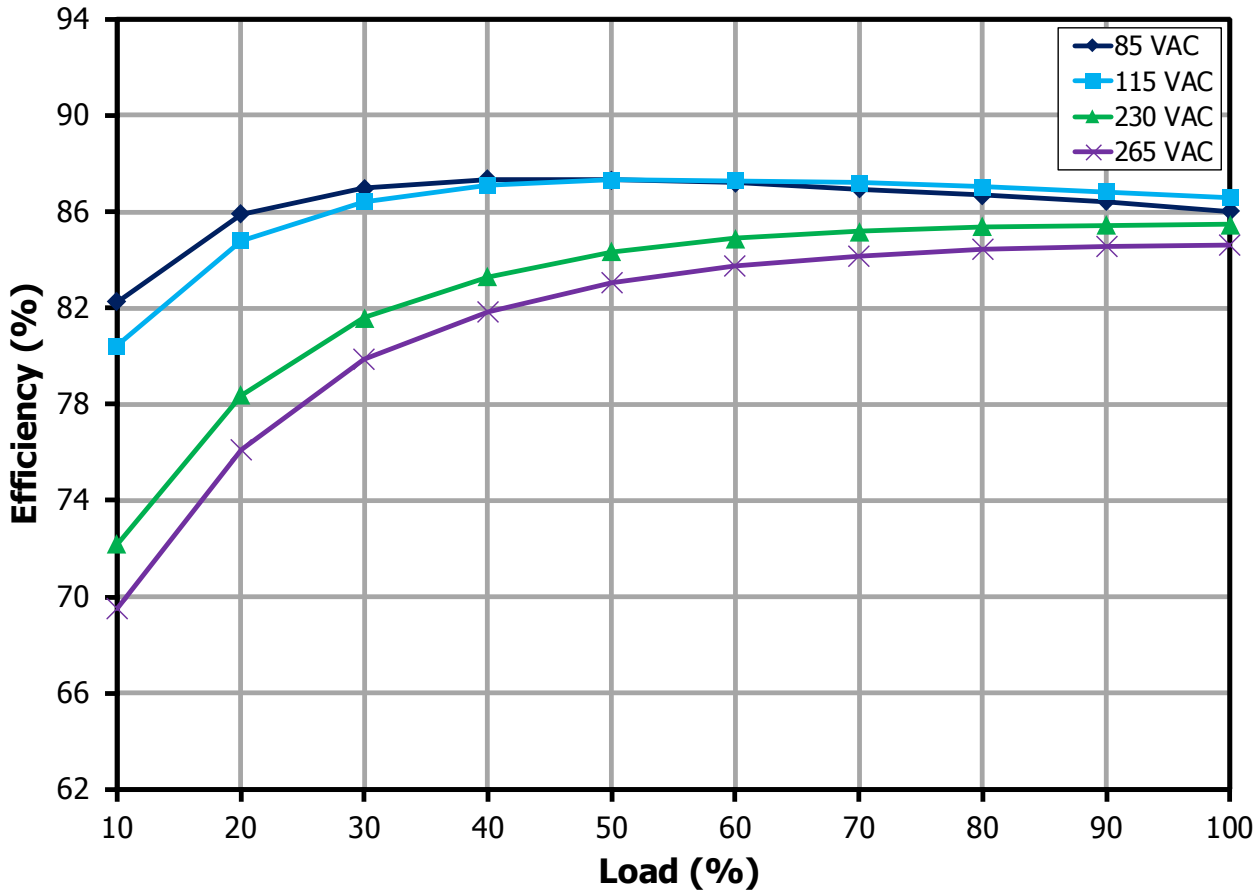

Figure 15 – 3.3 V Output Efficiency vs. Load.

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11.1.2 Output: 5 V / 3 A

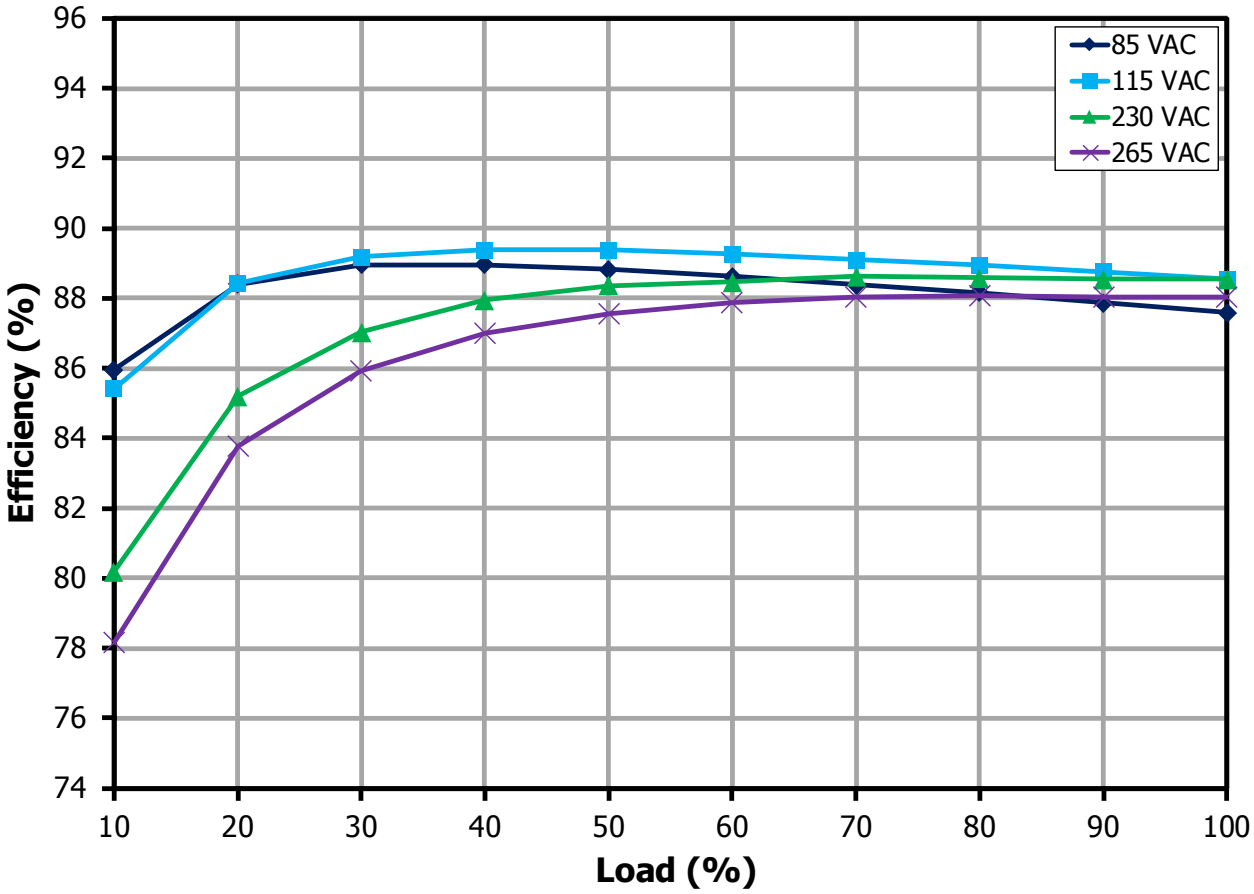

Figure 16 – 5 V Output Efficiency vs. Load.

11.1.3 Output: 9 V / 3 A

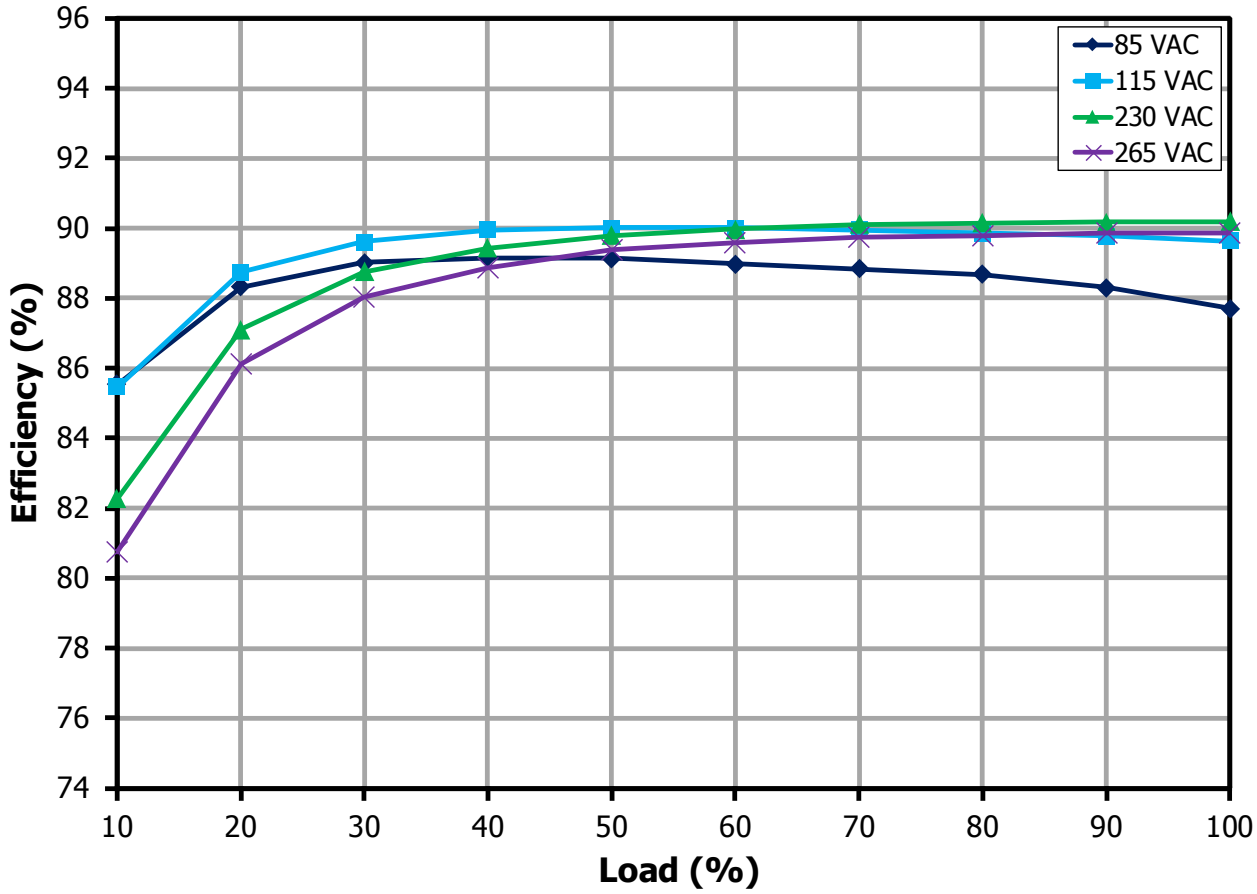

Figure 17 – 9 V Output Efficiency vs. Load.

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11.1.4 Output: 11 V / 2.45 A

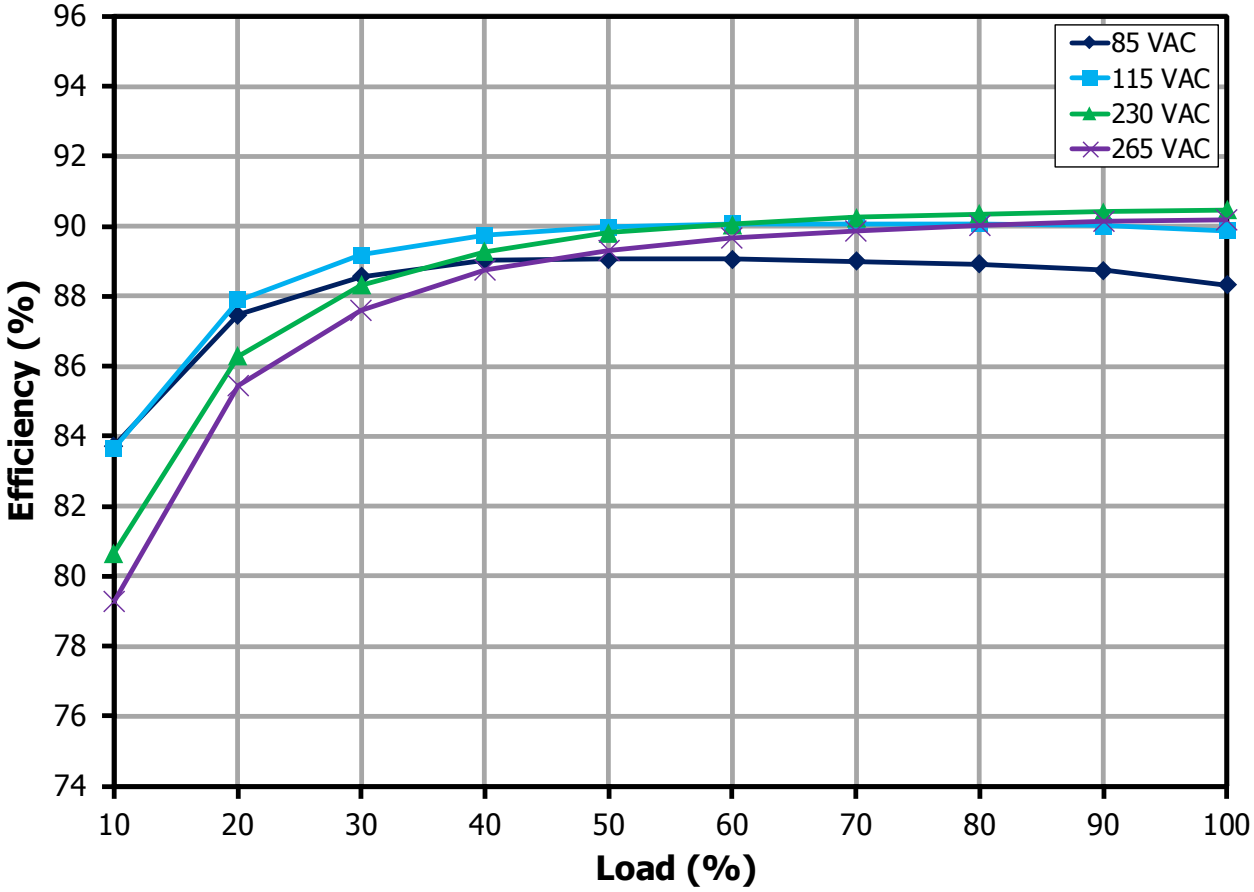

Figure 18 – 11 V Output Efficiency vs. Load.

11.2 Efficiency vs. Line

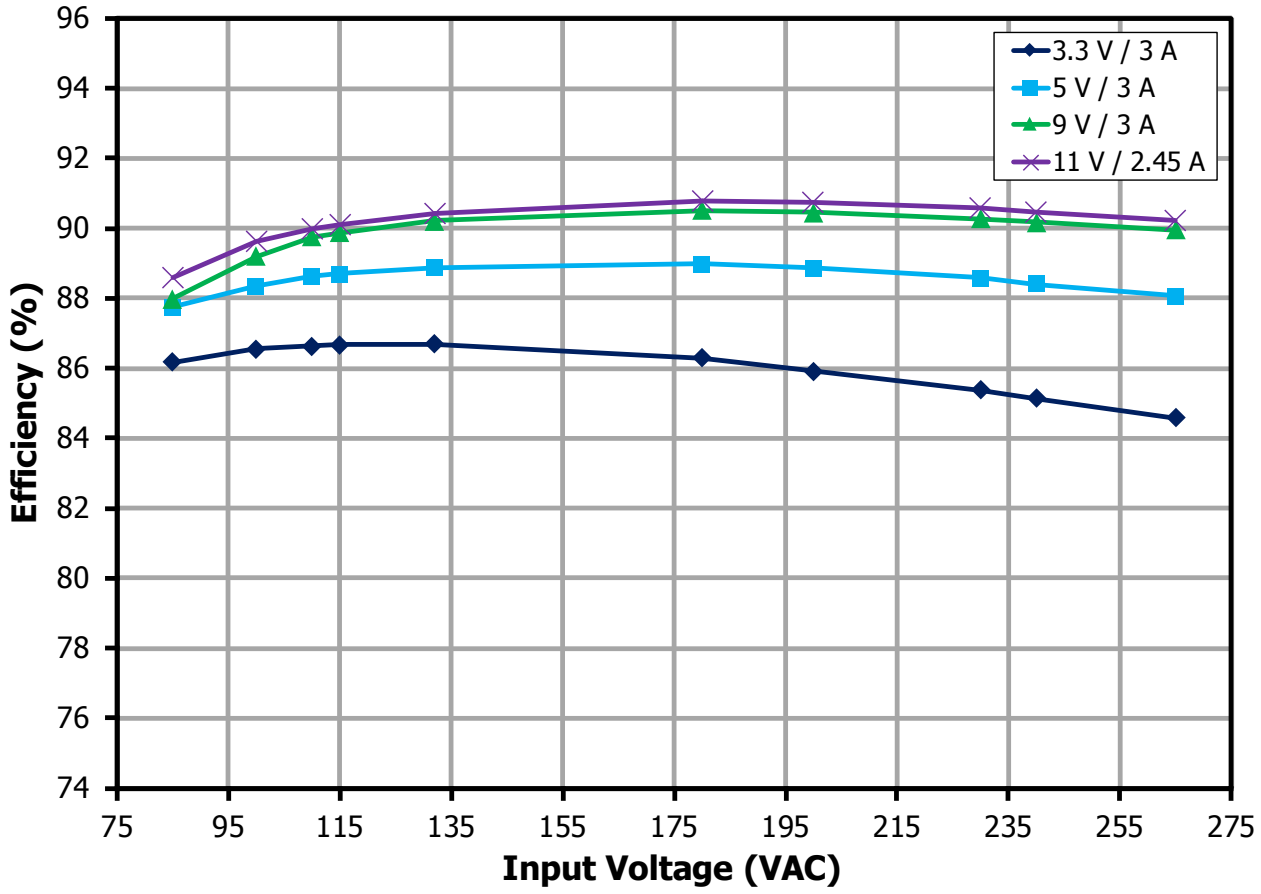

Figure 19 – Efficiency vs. Line.

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11.3 Load Regulation

11.3.1 Output: 3.3 V / 3 A

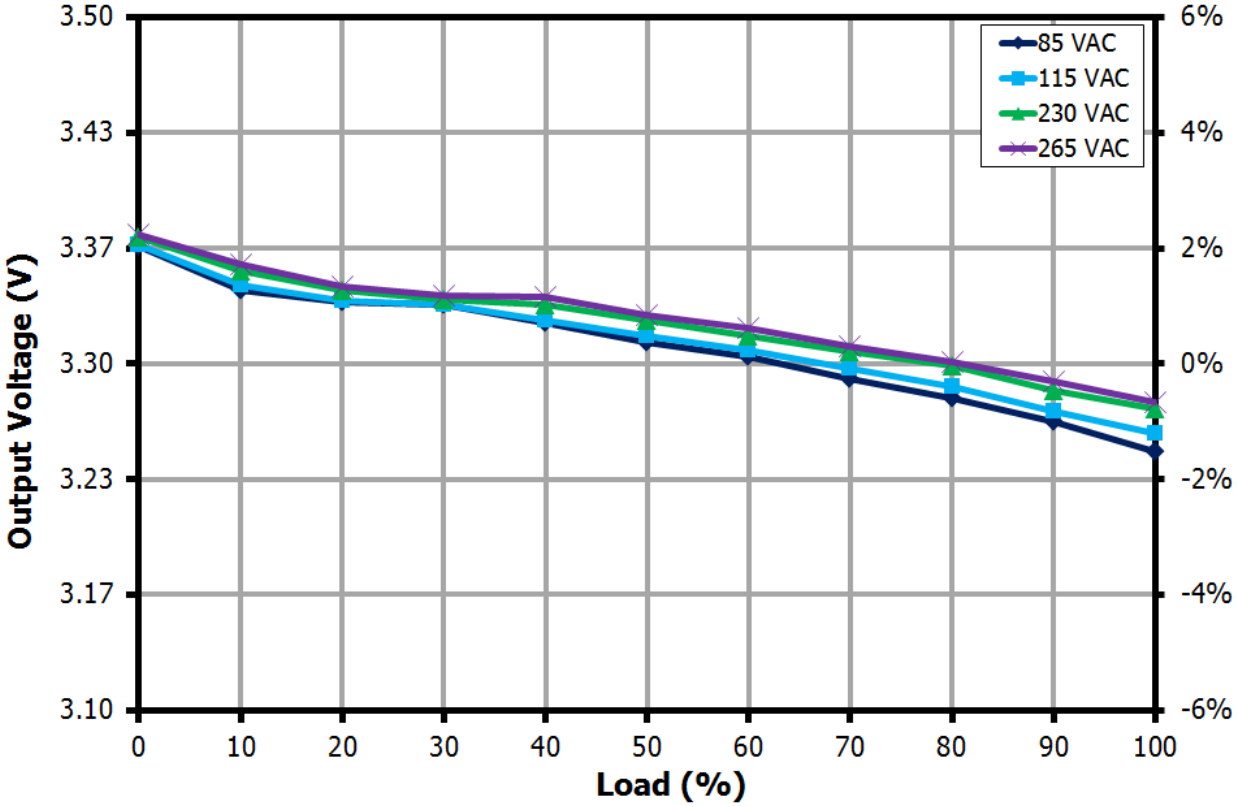

Figure 20 – 3.3 V Output Regulation vs. Percent Load.

11.3.2 Output: 5 V / 3 A

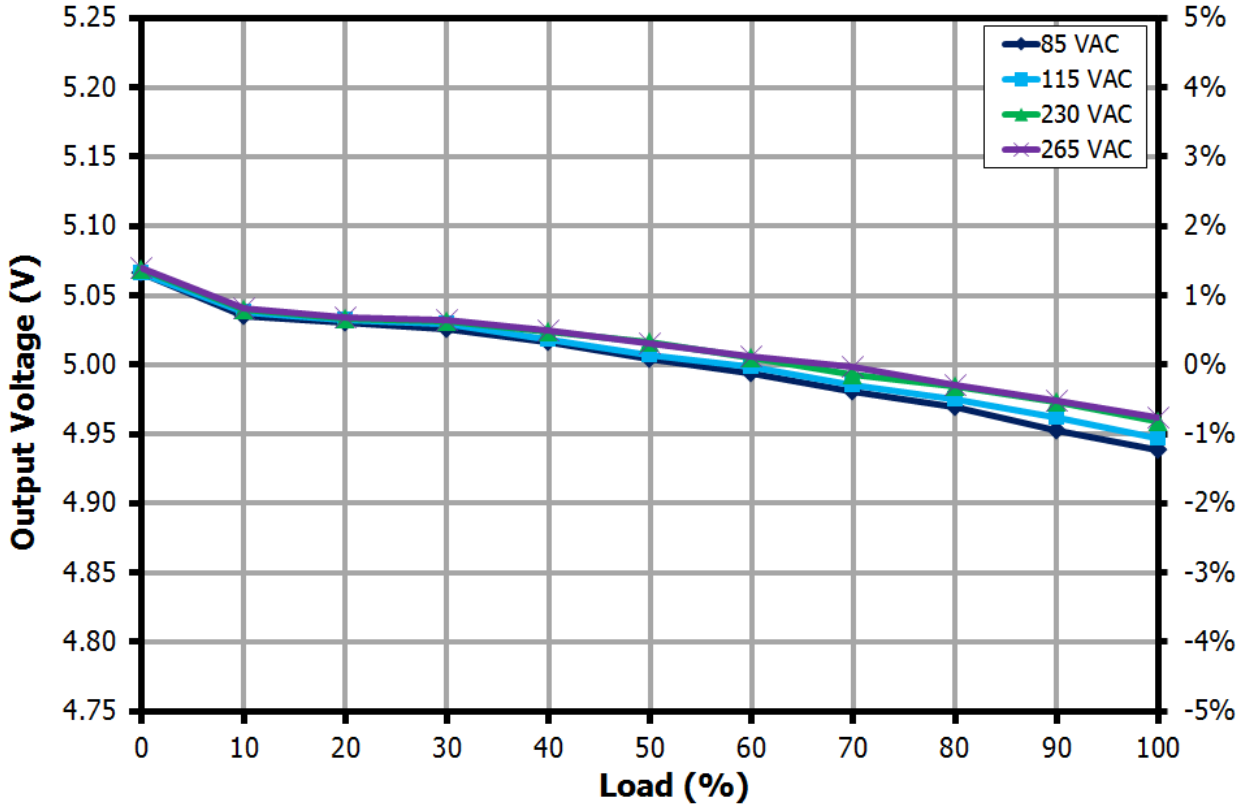

Figure 21 – 5 V Output Regulation vs. Percent Load.

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11.3.3 Output: 9 V / 3 A

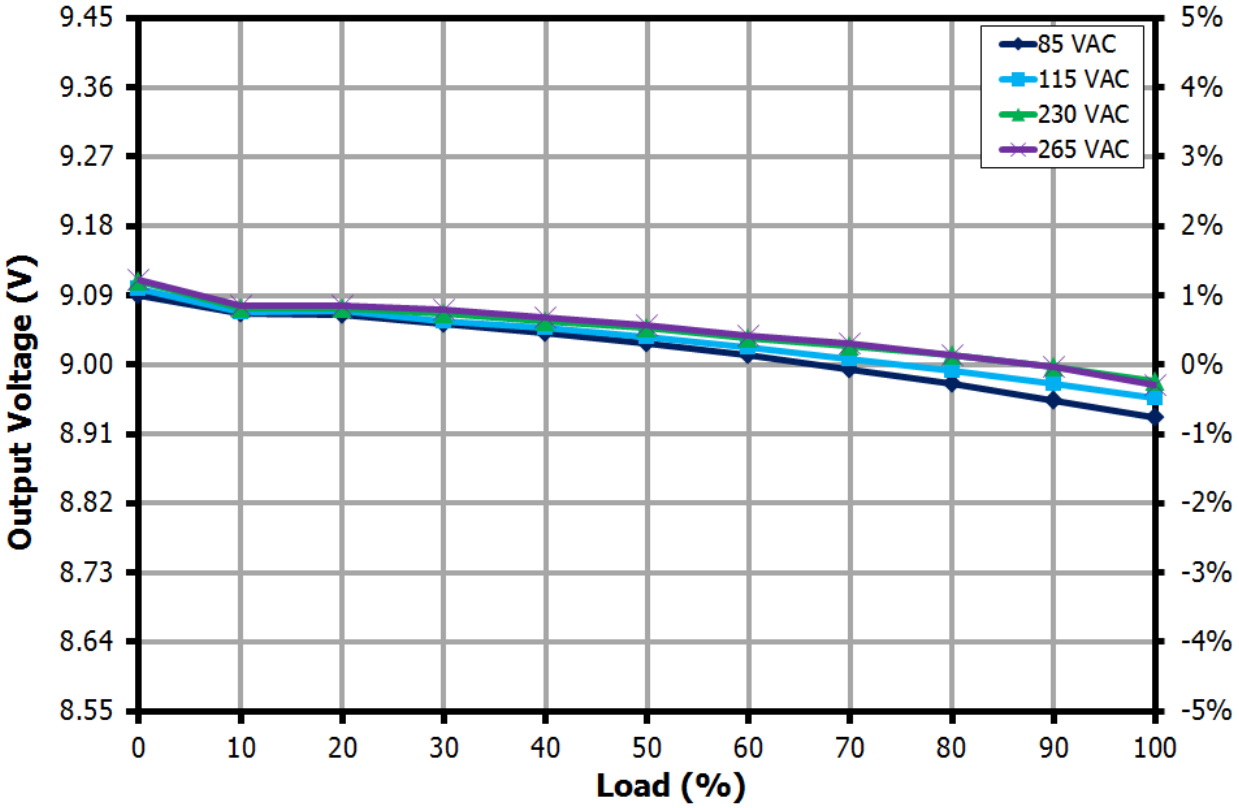

Figure 22 – 9 V Output Regulation vs. Percent Load.

11.3.4 Output: 11 V / 2.45 A

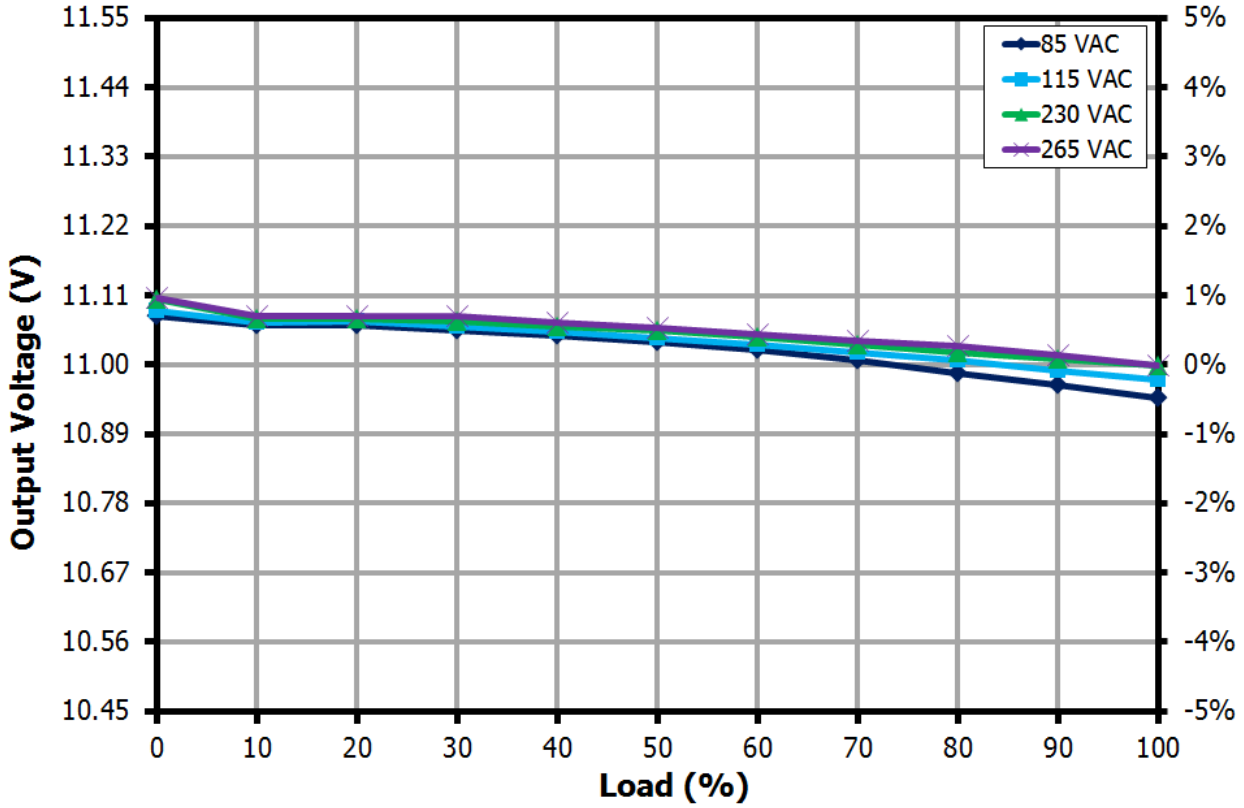

Figure 23 – 11 V Output Regulation vs. Percent Load.

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11.4 Line Regulation

11.4.1 Output: 3.3 V / 3 A

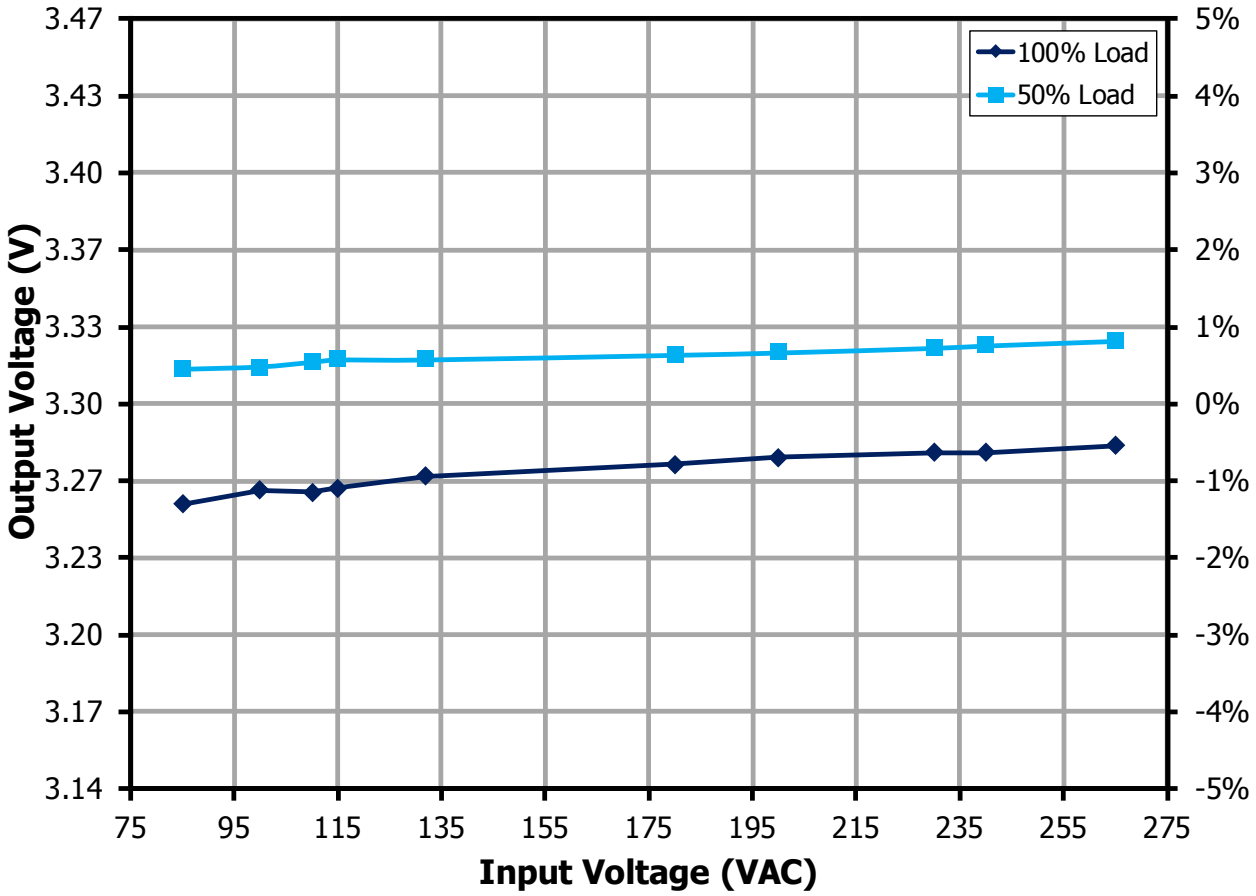

Figure 24 – 3.3 V Output Regulation vs. Input Line Voltage at 50% and 100% Load.

11.4.2 Output: 5 V / 3 A

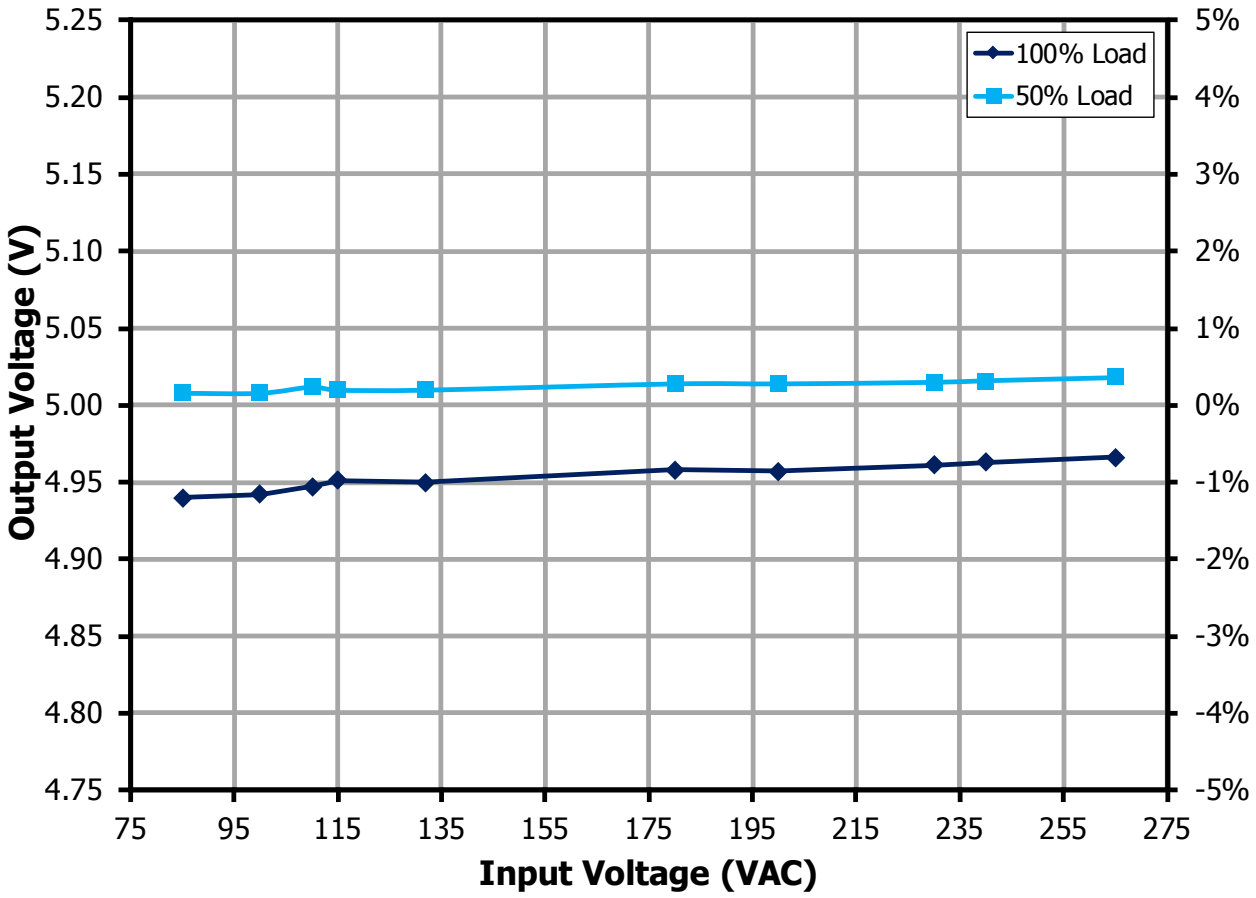

Figure 25 – 5 V Output Regulation vs. Input Line Voltage at 50% and 100% Load.

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11.4.3 Output: 9 V / 3 A

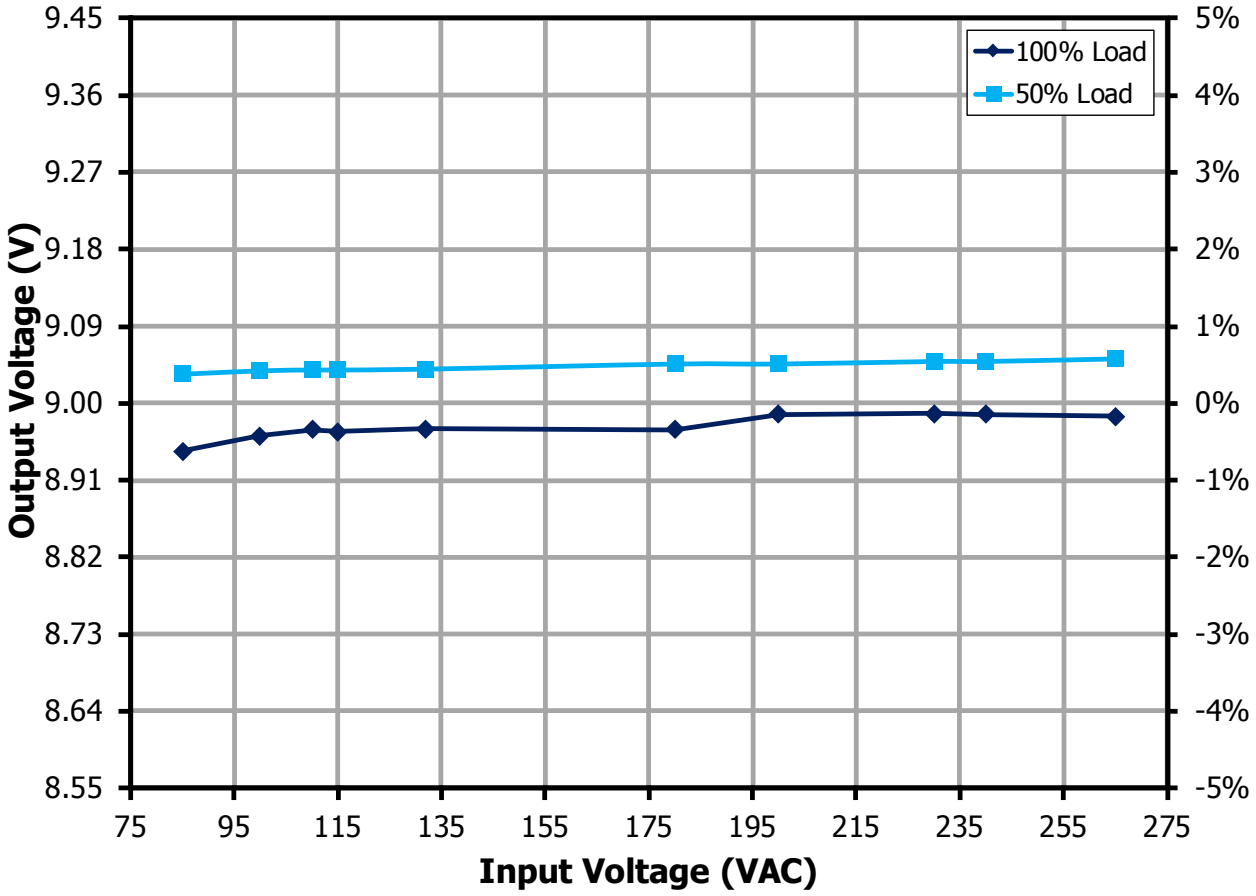

Figure 26 – 9 V Output Regulation vs. Input Line Voltage at 50% and 100% Load.

11.4.4 Output: 11 V / 2.45 A

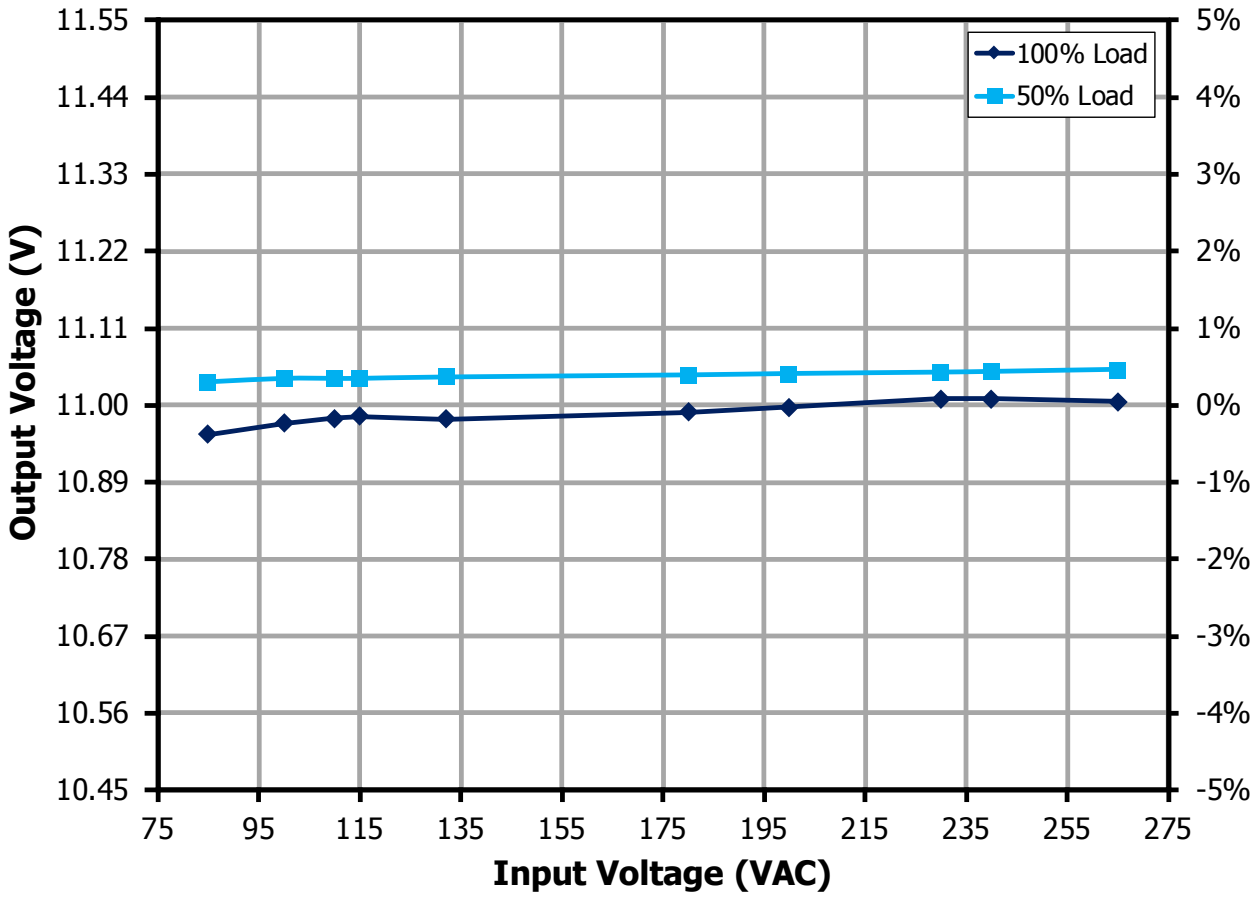

Figure 27 – 11 V Output Regulation vs. Input Line Voltage at 50% and 100% Load.

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11.5 No-Load Input Power at 5 V Output

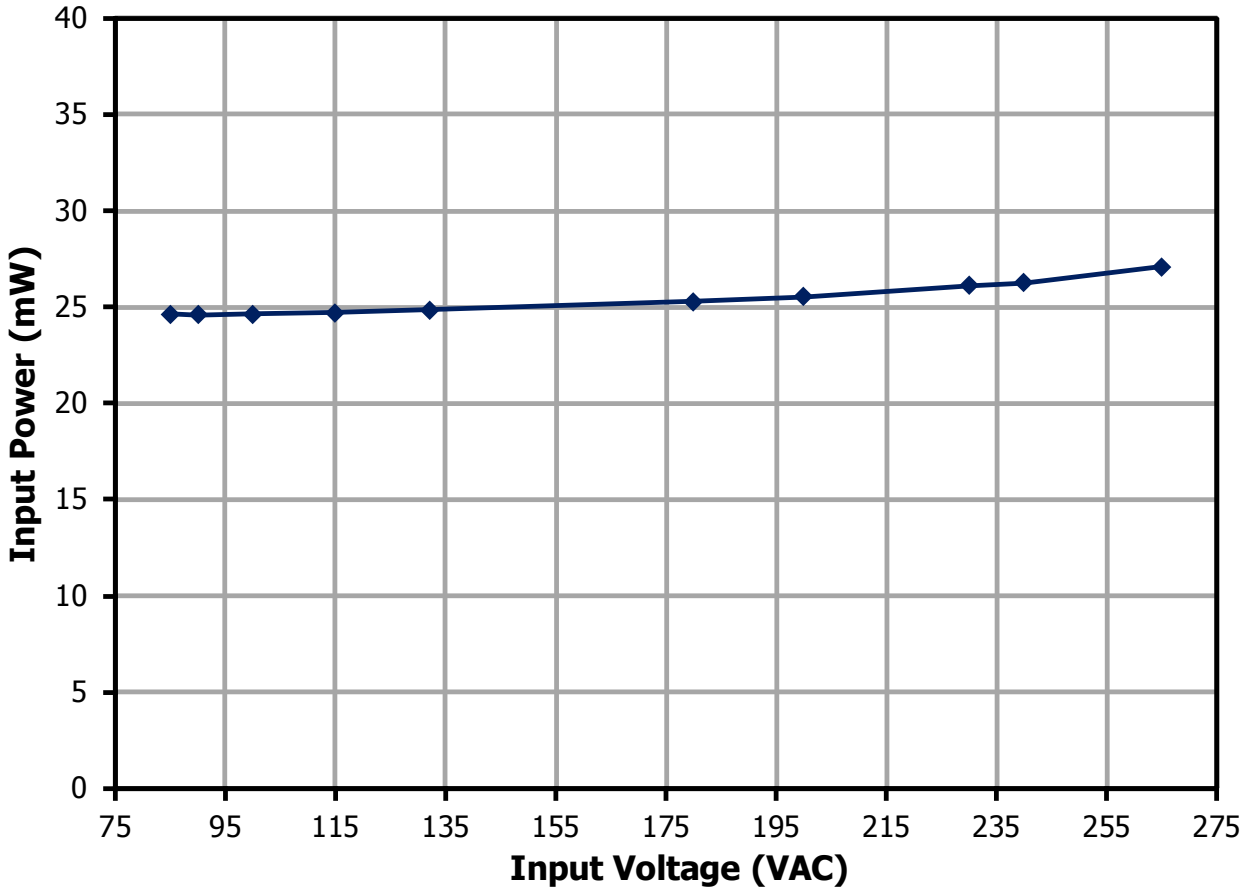

Figure 28 – No-Load Input Power vs. Input Line Voltage.

11.6 Average and 10% Load Efficiency

11.6.1 Efficiency Requirements

		Test	Average	Average	10% Load
		Effective	2016	Jan-16	Jan-16
Output Voltage (V)	Model (V)	Power (W)	New EISA2007 (%)	CoC v5 Tier 2 (%)	CoC v5 Tier 2 (%)
3.3	<6	9.9	78.6	78.9	69.7
5	<6	15	81.4	81.8	72.5
9	>6	27	86.6	87.3	77.3
11	>6	27	86.6	87.3	77.3

11.6.2 Average and 10% Load Efficiency (On the Board)

11.6.2.1 Output: 3.3 V / 3 A

Input (VAC)	Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)
115	100	9.78	86.64	**86.76**	78.63	78.93
	75	7.41	87.17			
	50	4.97	87.34			
	25	2.50	85.88			
	10	1.00	**80.40**			69.66
230	100	9.83	85.44	**83.87**	78.63	78.93
	75	7.43	85.28			
	50	4.99	84.37			
	25	2.50	80.40			
	10	1.00	**72.23**			69.66

11.6.2.2 Output: 5 V / 3 A

Input (VAC)	Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)
115	100	14.84	88.60	**88.99**	81.39	81.84
	75	11.20	89.05			
	50	7.51	89.40			
	25	3.77	88.89			
	10	1.51	**85.39**			72.48
230	100	14.87	88.48	**87.93**	81.39	81.84
	75	11.22	88.56			
	50	7.52	88.36			
	25	3.77	86.31			
	10	1.51	**80.18**			72.48

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11.6.2.3 Output: 9 V / 3 A

Input (VAC)	Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)
115	100	26.82	89.78	**89.82**	86.62	87.30
	75	20.19	89.99			
	50	13.52	90.10			
	25	6.78	89.38			
	10	2.706	**85.34**			77.30
230	100	26.853	90.29	**89.68**	86.62	87.30
	75	20.210	90.26			
	50	13.524	89.98			
	25	6.779	88.20			
	10	2.709	**82.34**			77.30

11.6.2.4 Output: 11 V / 2.45 A

Input (VAC)	Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)
115	100	26.82	90.13	**89.83**	86.61	87.29
	75	20.16	90.23			
	50	13.48	90.12			
	25	6.75	88.82			
	10	2.70	**83.40**			77.29
230	100	26.85	90.63	**89.66**	86.61	87.29
	75	20.18	90.49			
	50	13.48	89.88			
	25	6.75	87.62			
	10	2.70	**80.48**			77.288

11.7 CV/CC Operation

Note: Positive slope in CC region is per the guidelines of USB PD 3.0 PPS specification.

11.7.1 Output: 5 V / 3 A

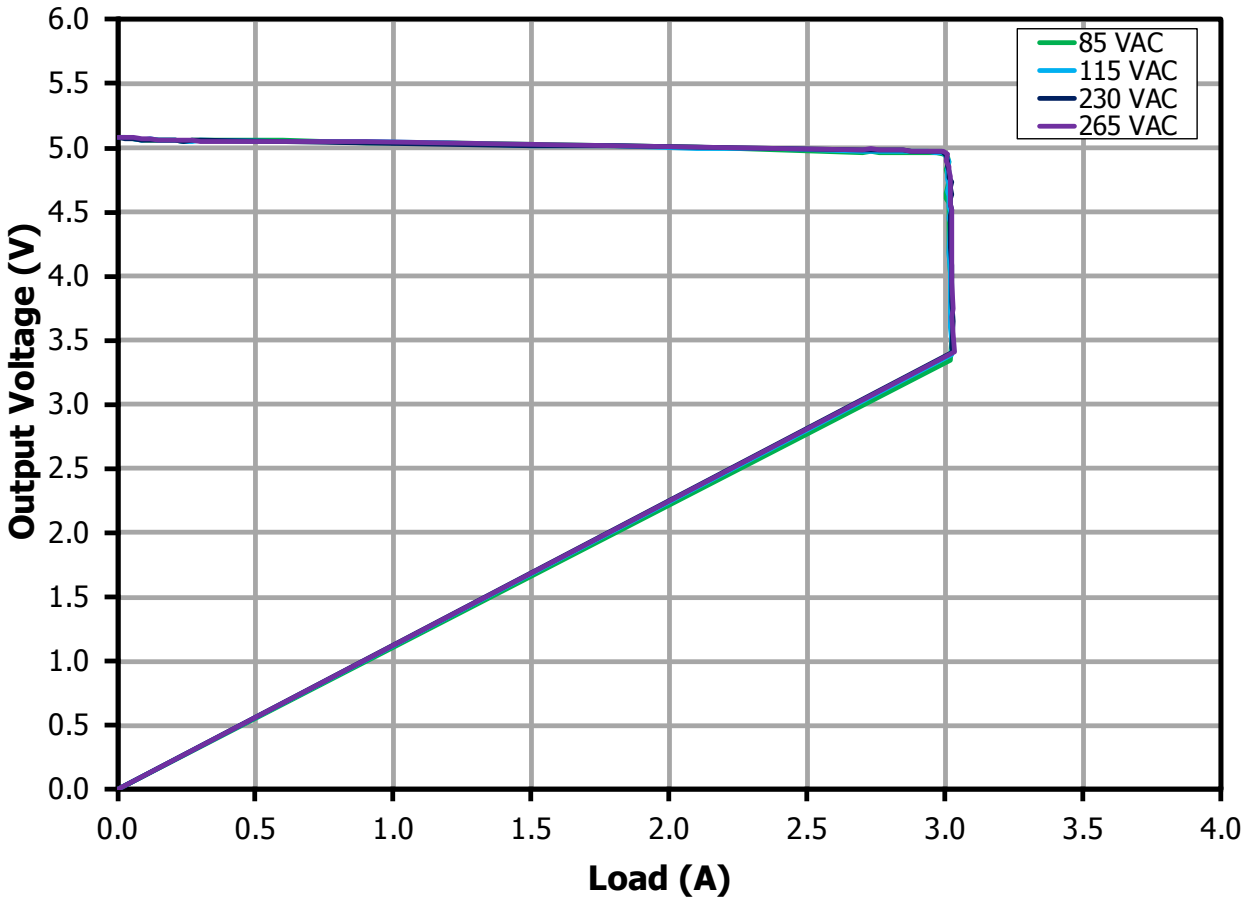

Figure 29 – Output Voltage vs. Output Current, Room Temperature.

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11.7.2 Output: 9 V / 3 A

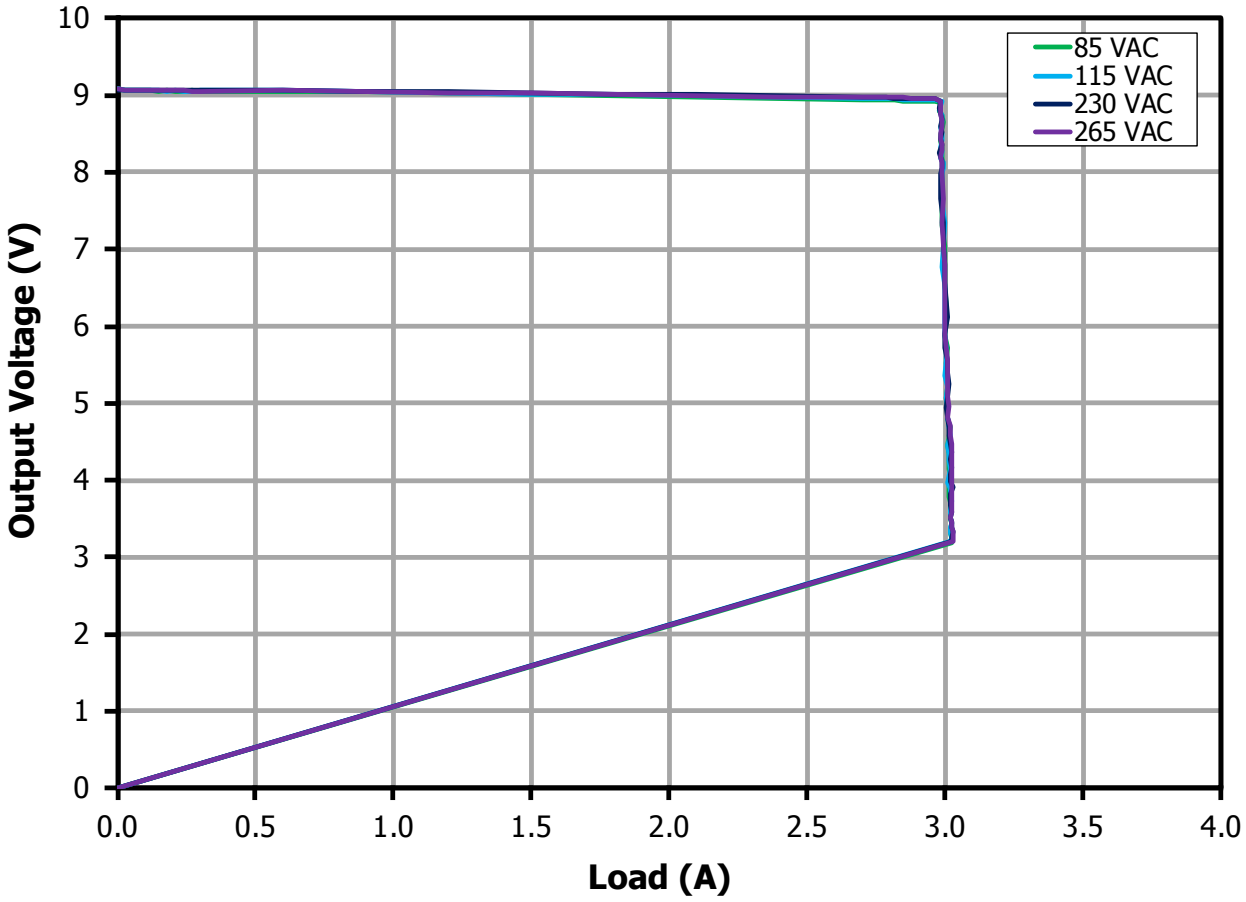

Figure 30 – Output Voltage vs. Output Current, Room Temperature.

11.7.3 Output: 11 V / 2.45 A

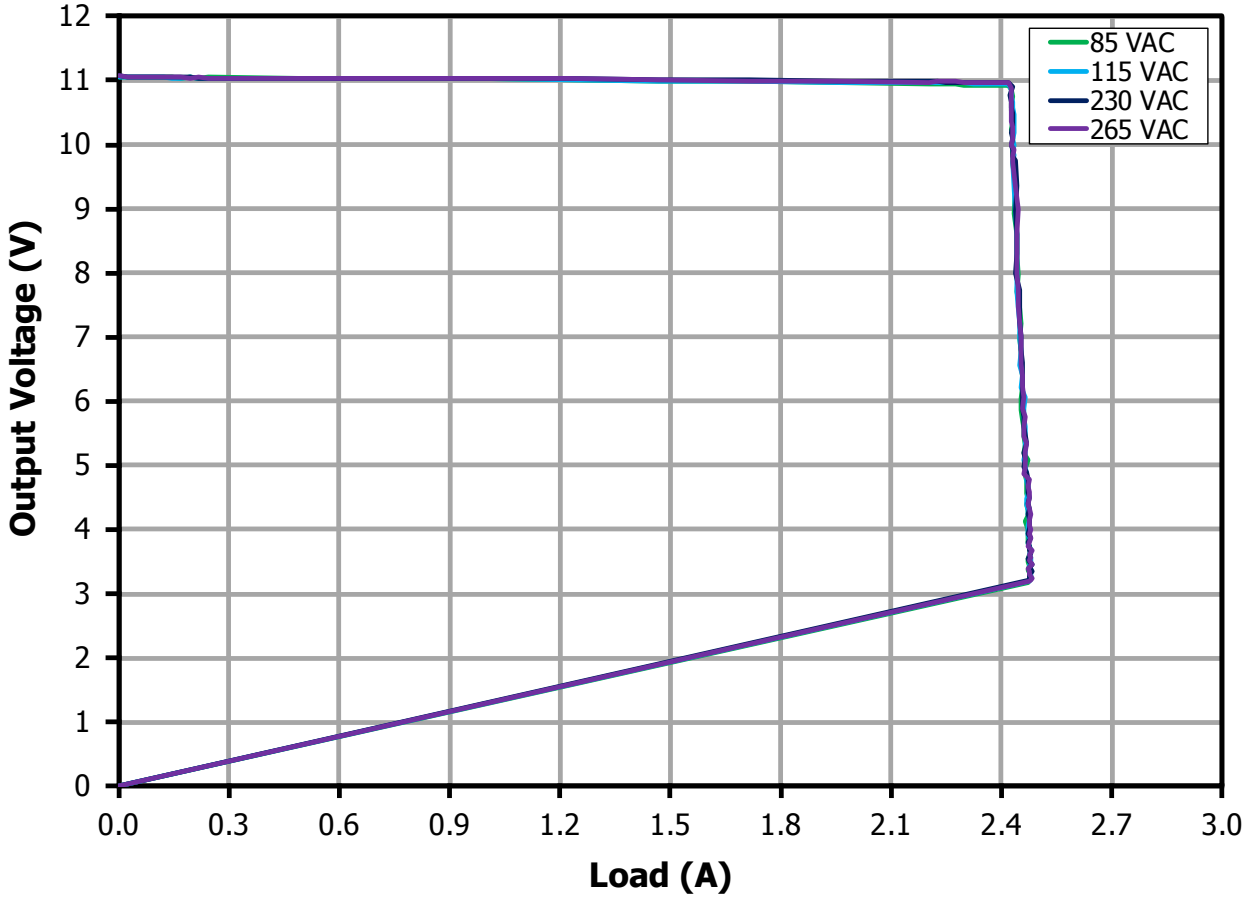

Figure 31 – Output Voltage vs. Output Current, Room Temperature.

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12 Thermal Performance in Open Case

Note: For plastic enclosed adapters, this design requires use of a metallic heat spreader and suitable thermally conductive insulator to ensure sufficiently low temperature of the InnoSwitch3-Pro IC and transformer. The performance data below is for open case operation and does not use the heat spreader for cooling.

12.1 85 VAC Input 5 V / 3 A

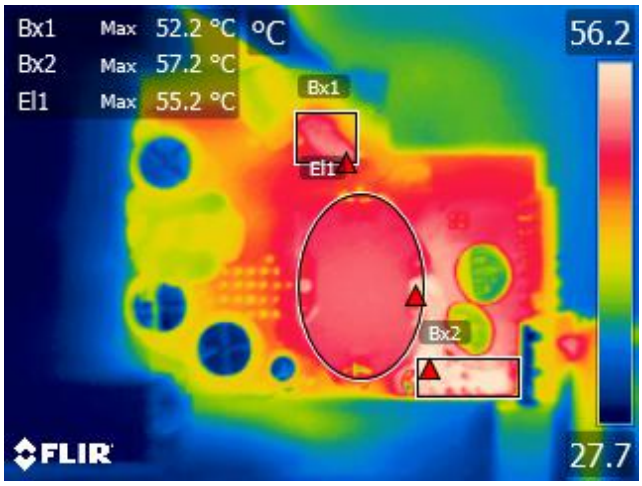

Figure 32 – Top Side Thermal Image.
Bx1: Thermistor RT1 = 55.2 ºC.
Bx2: SR FET, PCB = 57.2 ºC.
El1: Transformer = 55.2 ºC.

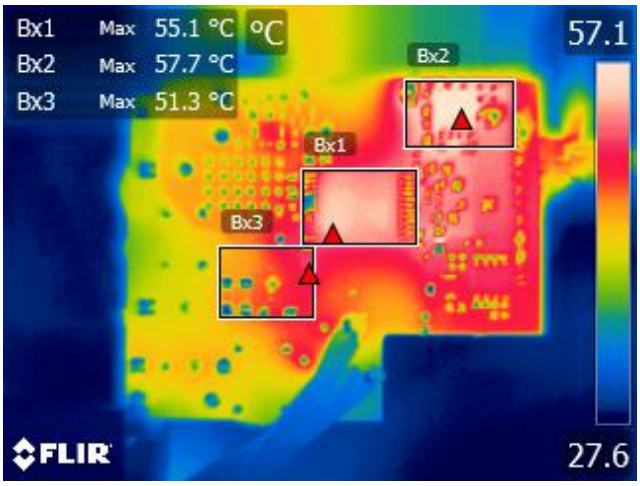

Figure 33 – Bottom Side Thermal Image.
Bx1: InnoSwitch3-Pro = 55.1 ºC.
Bx2: SR FET = 57.7 ºC.
Bx3: Primary Snubber = 51.3 ºC.

12.2 265 VAC Input 5 V / 3 A

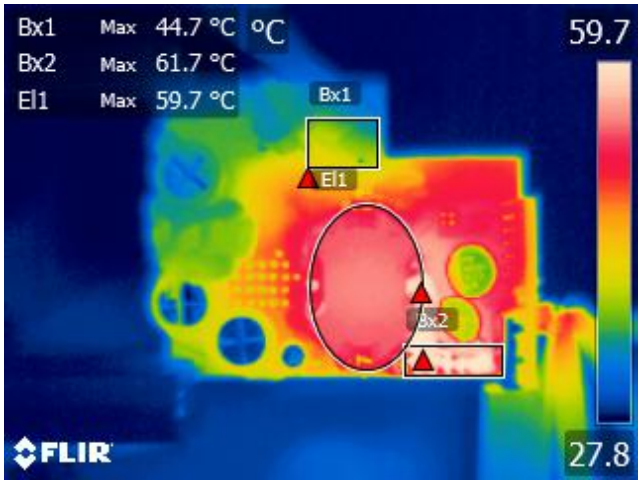

Figure 34 – Top Layer Thermal Image.
Bx1: Thermistor RT1 = 44.7 ºC.
Bx2: SR FET, PCB = 61.7 ºC.
El1: Transformer = 59.7 ºC.

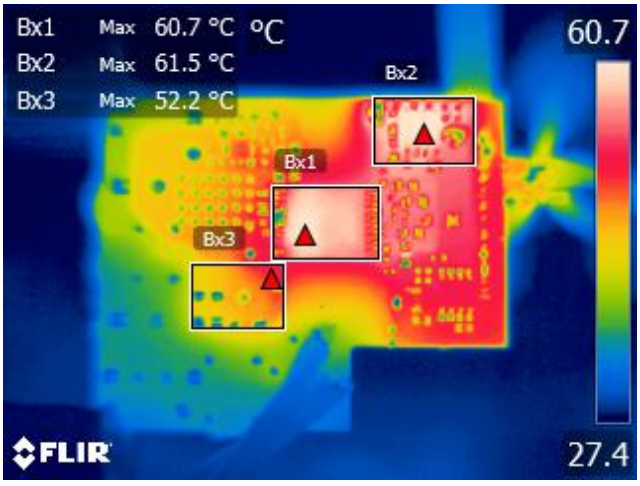

Figure 35 – Bottom Side Thermal Image.
Bx1: InnoSwitch3-Pro = 60.7 ºC.
Bx2: SR FET = 61.5 ºC.
Bx3: Primary Snubber = 52.2 ºC.

12.3 85 VAC Input 9 V / 3 A

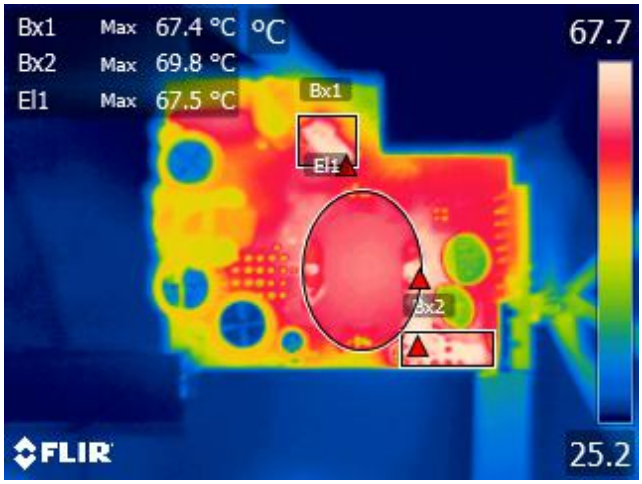

Figure 36 – Top Side Thermal Image.
Bx1: Thermistor RT1 = 67.4 ºC.
Bx2: SR FET, PCB = 69.8 ºC.
El1: Transformer = 67.5 ºC.

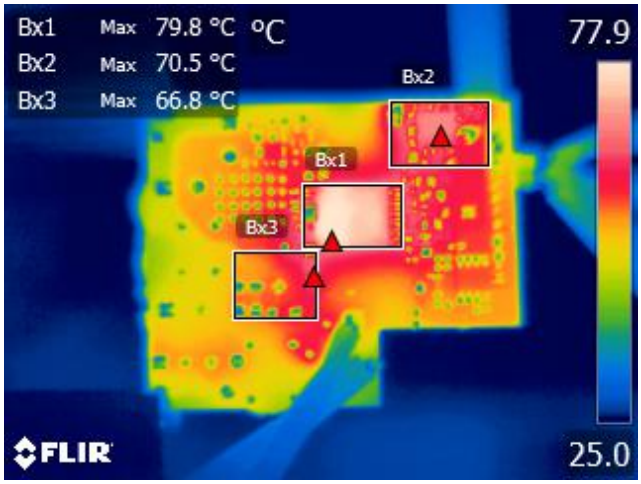

Figure 37 – Bottom Side Thermal Image.
Bx1: InnoSwitch3-Pro = 79.8 ºC.
Bx2: SR FET = 70.5 ºC.
Bx3: Primary Snubber = 66.8 ºC.

12.4 265 VAC Input 9 V / 3 A

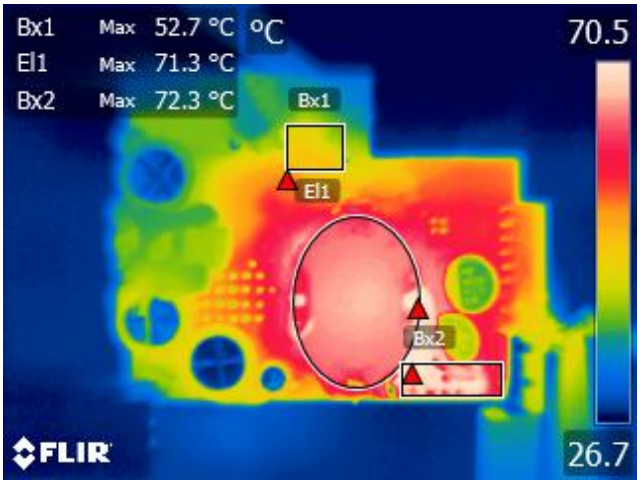

Figure 38 – Top Layer Thermal Image.
Bx1: Thermistor RT1 = 52.7 ºC.
Bx2: SR FET, PCB = 71.3 ºC.
El1: Transformer = 72.3 ºC.

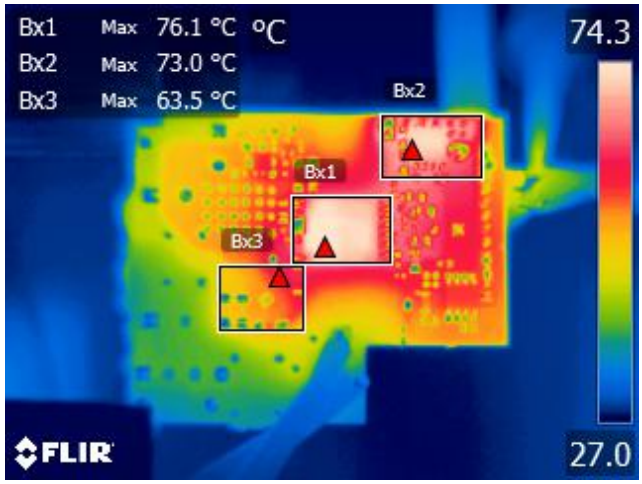

Figure 39 – Bottom Side Thermal Image.
Bx1: InnoSwitch3-Pro = 76.1 ºC.
Bx2: SR FET = 73.0 ºC.
Bx3: Primary Snubber = 63.5 ºC.

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12.5 85 VAC Input 11 V / 2.45 A

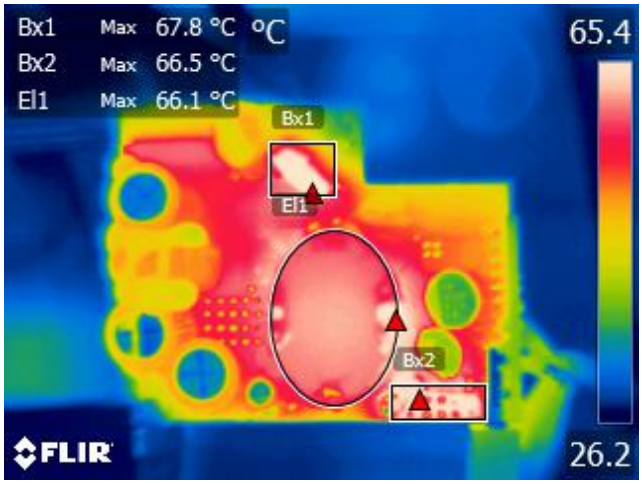

Figure 40 – Top Side Thermal Image.
Bx1: Thermistor RT1 = 67.8 ºC.
Bx2: SR FET, PCB = 66.5 ºC.
El1: Transformer = 66.1 ºC.

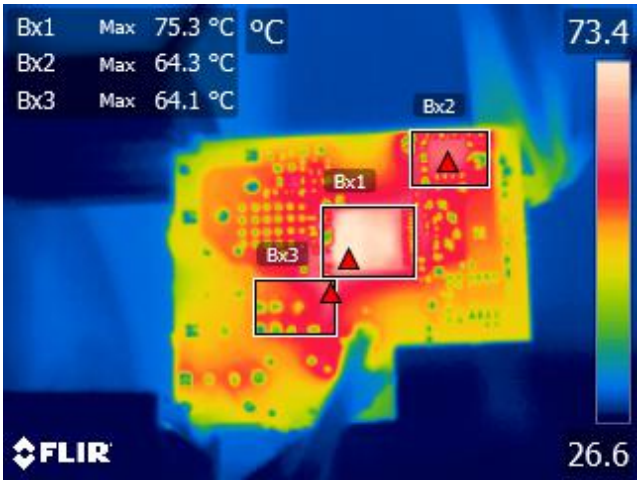

Figure 41 – Bottom Side Thermal Image.
Bx1: InnoSwitch3-Pro = 75.3 ºC.
Bx2: SR FET = 64.3 ºC.
Bx3: Primary Snubber = 64.1 ºC.

12.6 265 VAC Input 11 V / 2.45 A

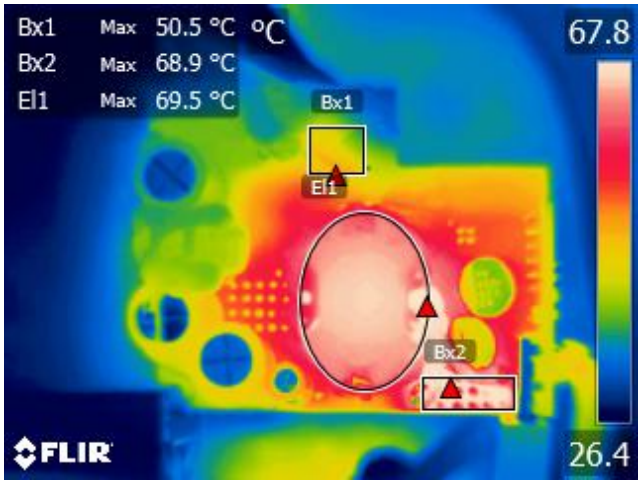

Figure 42 – Top Layer Thermal Image.
Bx1: Thermistor RT1 = 50.5 ºC.
Bx2: SR FET, PCB = 68.9 ºC.
El1: Transformer = 69.5 ºC.

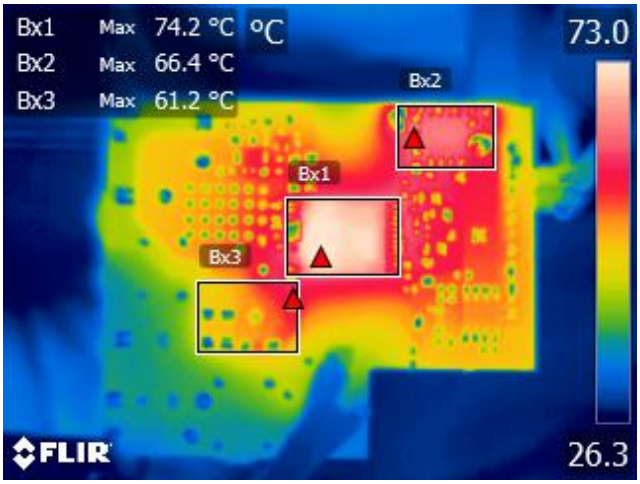

Figure 43 – Bottom Side Thermal Image.
Bx1: InnoSwitch3-Pro = 74.2 ºC.
Bx2: SR FET = 66.4 ºC.
Bx3: Primary Snubber = 61.2 ºC.

13 Output Voltage Ripple Measurements

13.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 47 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

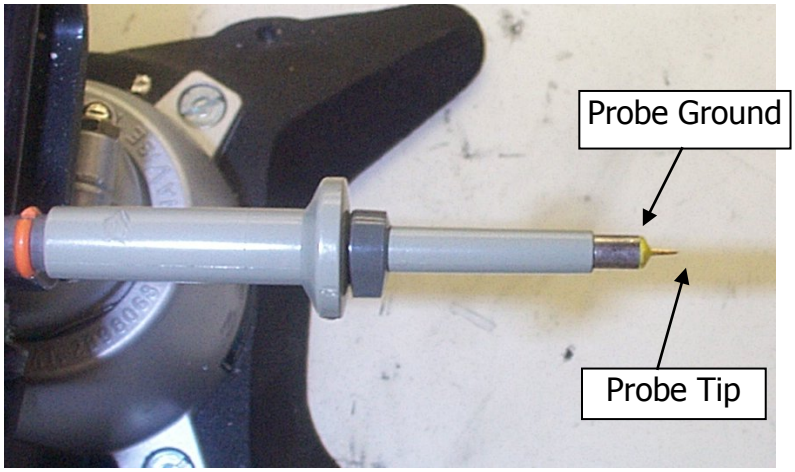

Figure 44 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

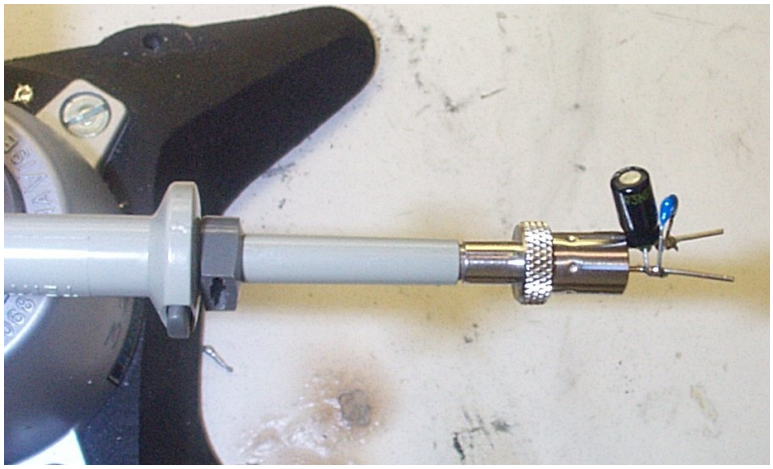

Figure 45 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added.)

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13.2 Output Voltage Ripple Waveforms

Note: Measurements are taken at the end of 100 mΩ cable.

13.2.1 Output: 3.3 V / 3 A

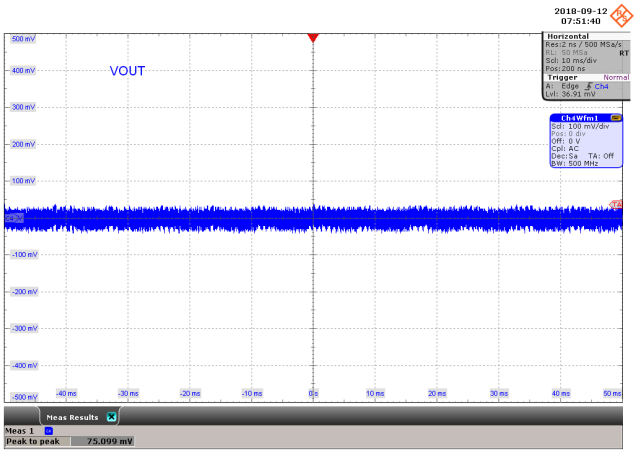

Figure 46 – Output Ripple (75 mV_{PK-PK}).
85 VAC, 3.3 V, 3 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.

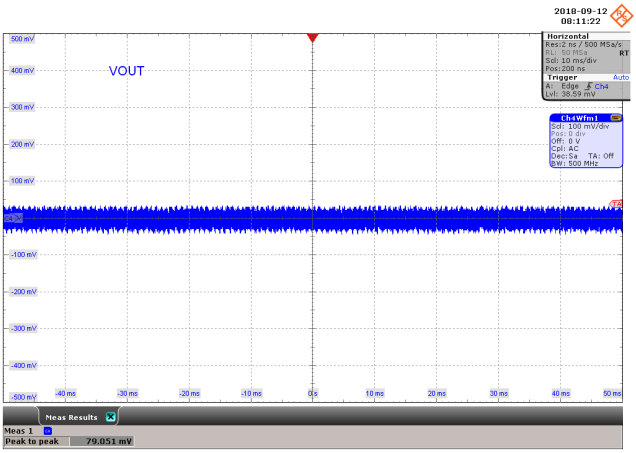

Figure 47 – Output Ripple (79 mV_{PK-PK}).
265 VAC, 3.3 V, 3 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.

13.2.2 Output: 5 V / 3 A

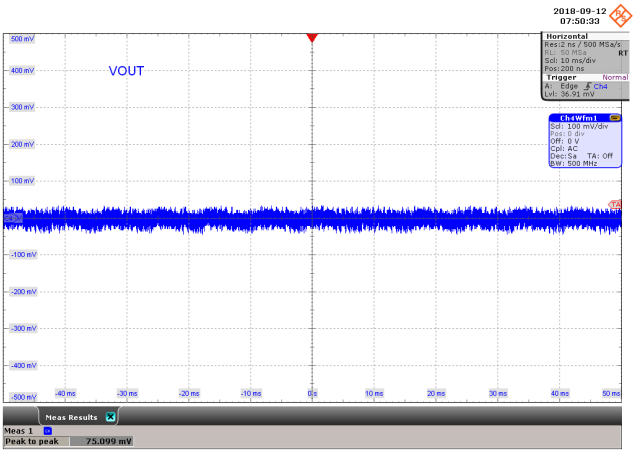

Figure 48 – Output Ripple (75 mV_{PK-PK}).
85 VAC, 5.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.

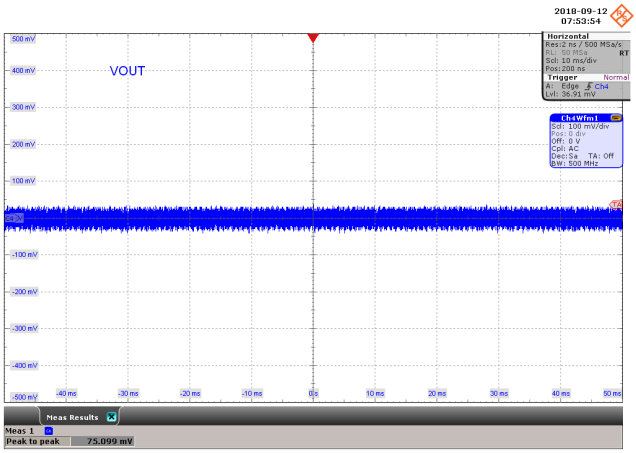

Figure 49 – Output Ripple (75 mV_{PK-PK}).
265 VAC, 5.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.

13.2.3 Output: 9 V / 3 A

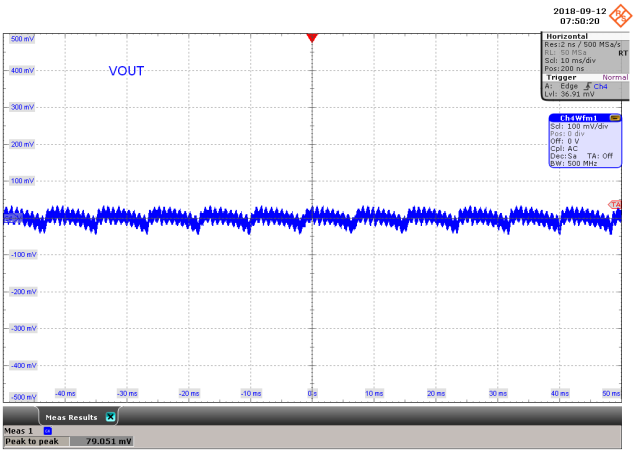

Figure 50 – Output Ripple (79 mV_{PK-PK}).
85 VAC, 9.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.

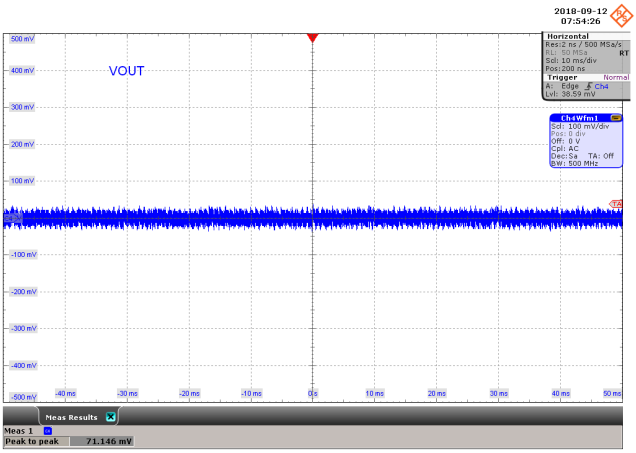

Figure 51 – Output Ripple (71 mV_{PK-PK}).
265 VAC, 9.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.

13.2.4 Output: 11 V / 2.45 A

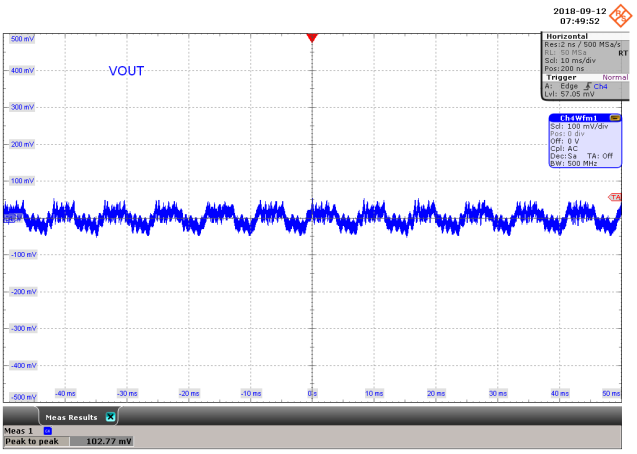

Figure 52 – Output Ripple (102 mV_{PK-PK}).
85 VAC, 11.0 V, 2.45 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.

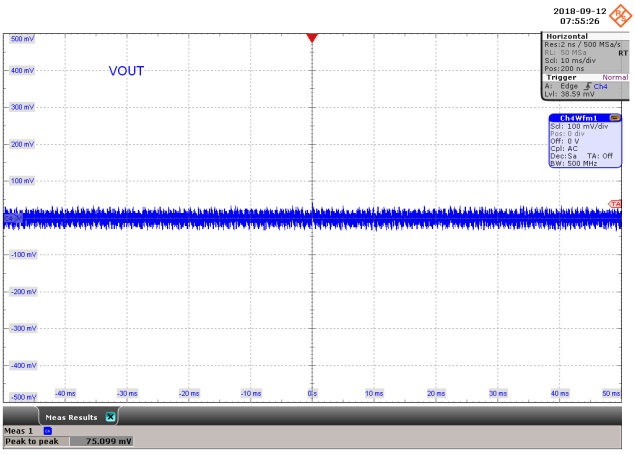

Figure 53 – Output Ripple (75 mV_{PK-PK}).
265 VAC, 11.0 V, 2.45 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.

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13.3 Output Voltage Ripple Amplitude vs. Load

13.3.1 Output: 3.3 V / 3 A

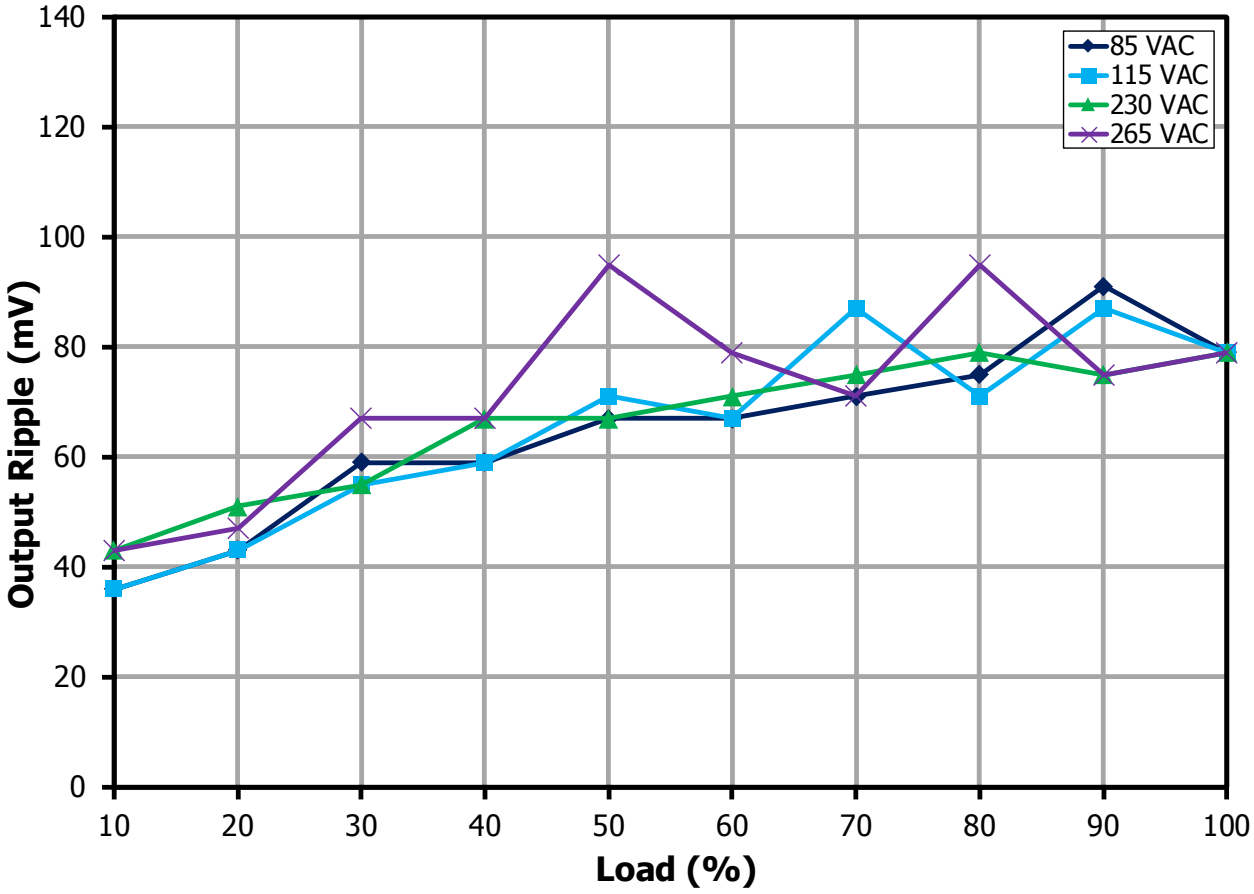

Figure 54 – 3.3 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.

13.3.2 Output: 5 V / 3 A

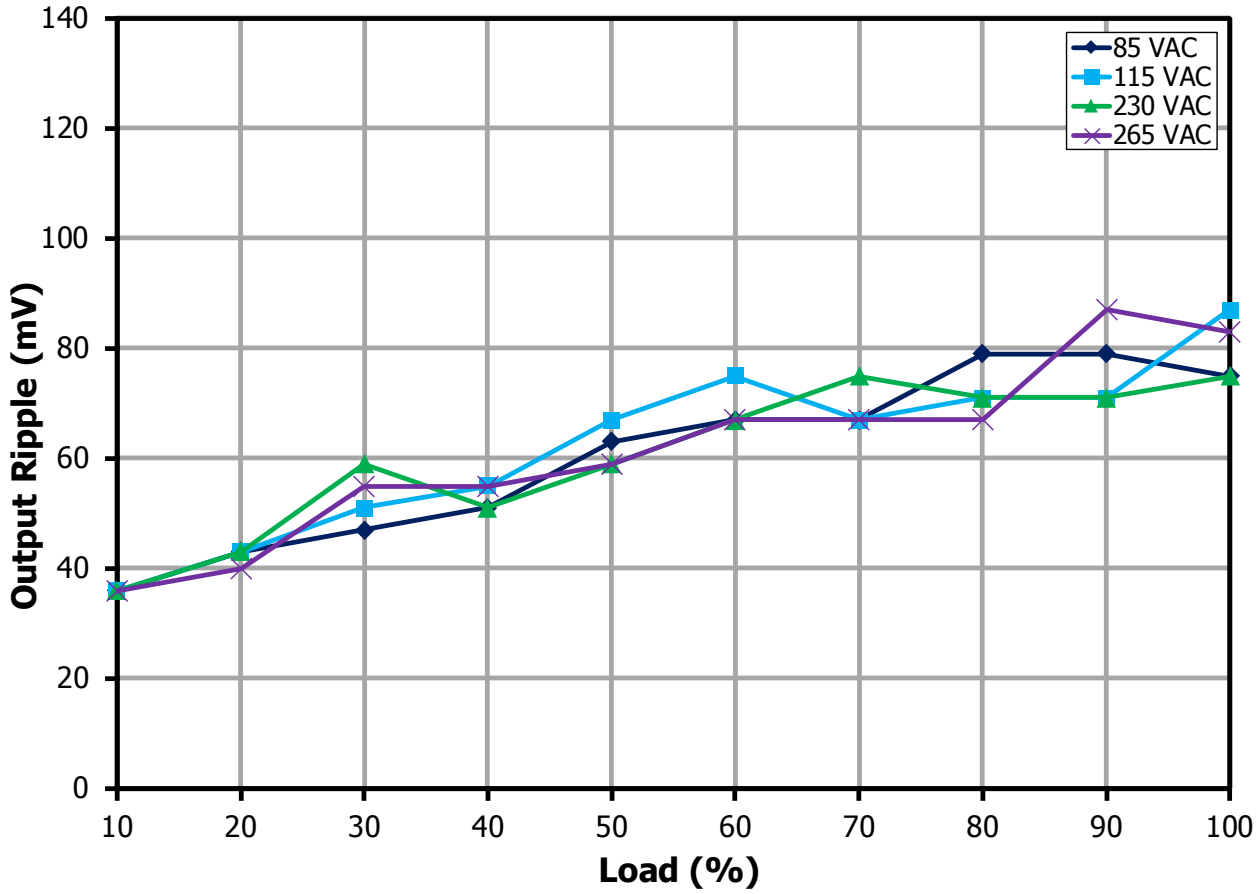

Figure 55 – 5 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.

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13.3.3 Output: 9 V / 3 A

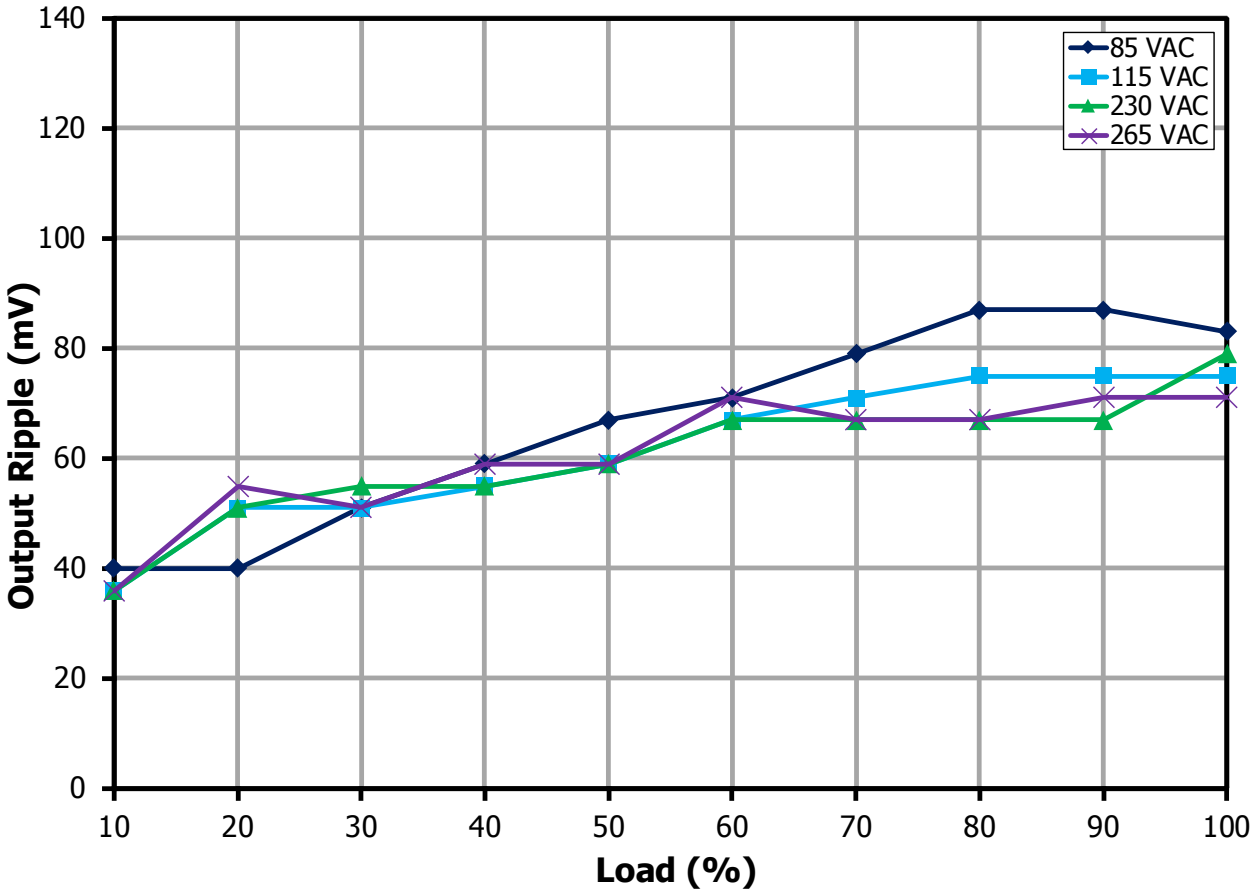

Figure 56 – 9 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.

13.3.4 Output: 11 V / 2.45 A

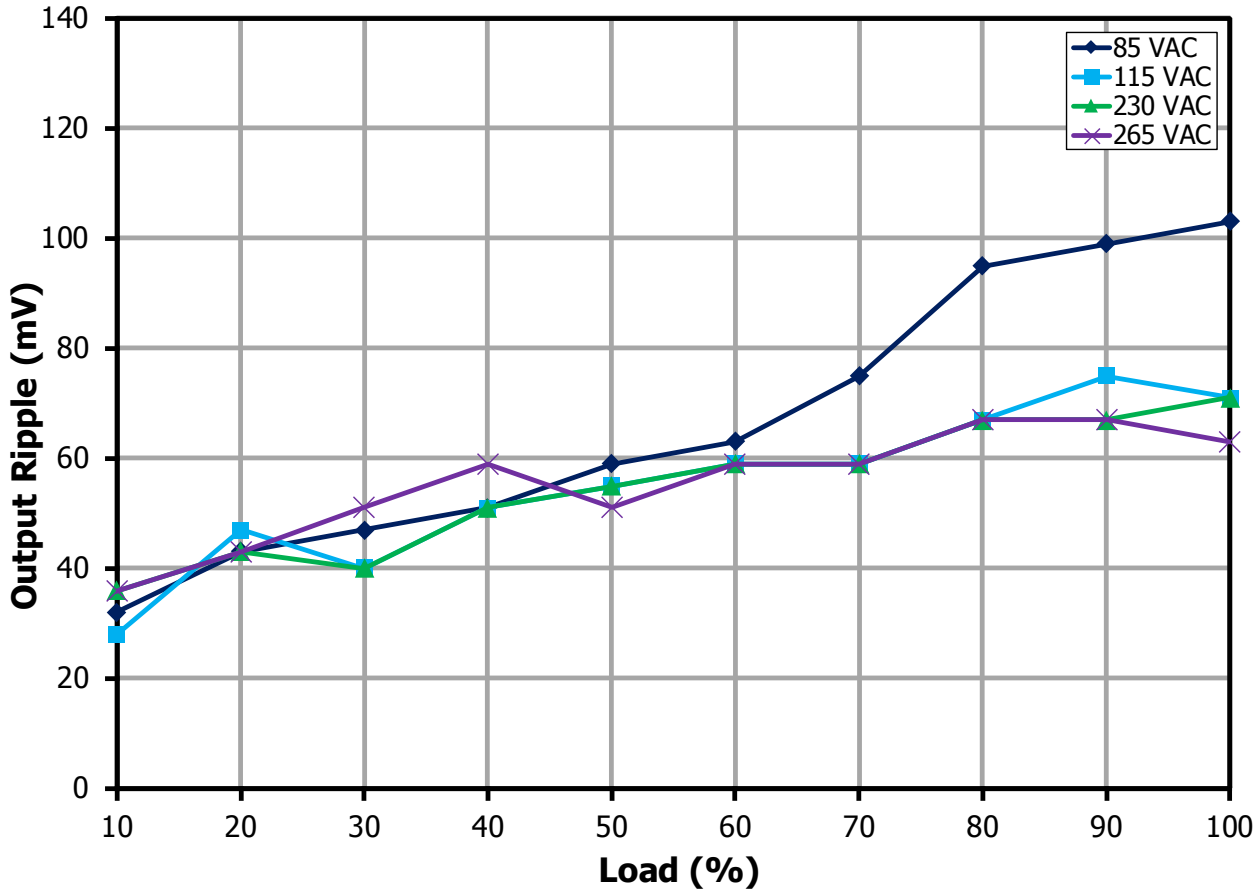

Figure 57 – 11 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.

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14 Waveforms

14.1 Load Transient Response (On the Board)

14.1.1 Load Step Response

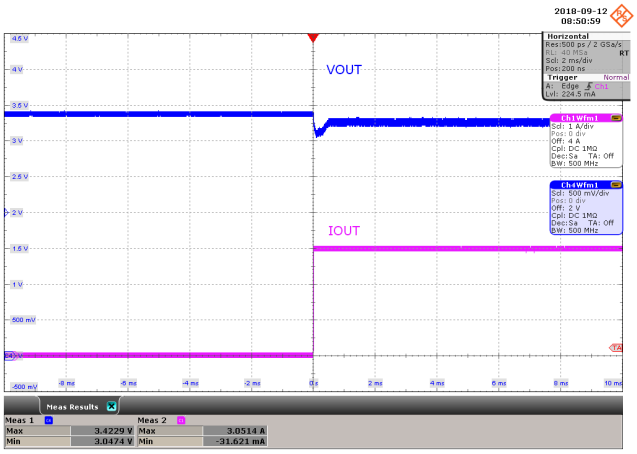

Figure 58 – Load Step Response (Rising).
85 VAC, 3.3 V, 0 – 3 A Load Step.
V_{MIN}: 3.04 V, V_{MAX}: 3.42 V.
Upper: V_{OUT}, 500 mV / div., 2 ms / div.
Lower: I_{LOAD}, 1 A / div.

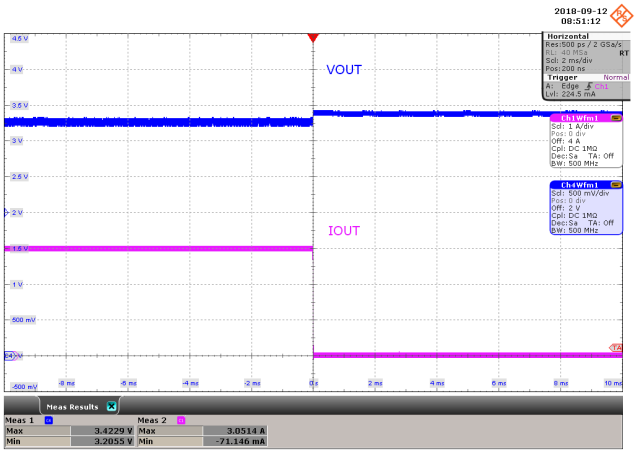

Figure 59 – Load Step Response (Falling).
85 VAC, 3.3 V, 3 – 0 A Load Step.
V_{MIN}: 3.20 V, V_{MAX}: 3.42 V.
Upper: V_{OUT}, 500 mV / div., 2 ms / div.
Lower: I_{LOAD}, 1 A / div.

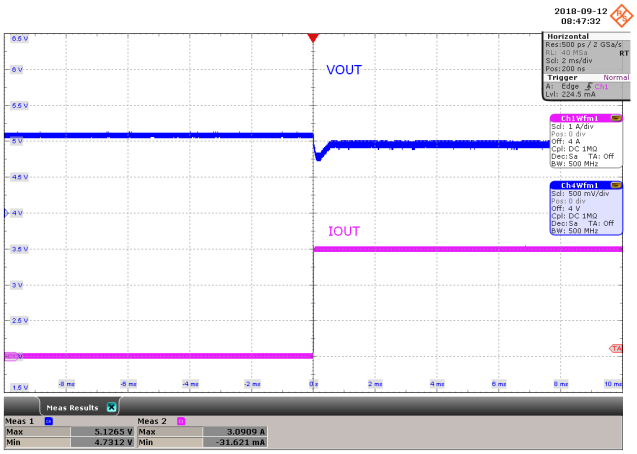

Figure 60 – Load Step Response (Rising).
85 VAC, 5.0 V, 0 – 3 A Load Step.
V_{MIN}: 4.73 V, V_{MAX}: 5.12 V.
Upper: V_{OUT}, 500 mV / div., 2 ms / div.
Lower: I_{LOAD}, 1 A / div.

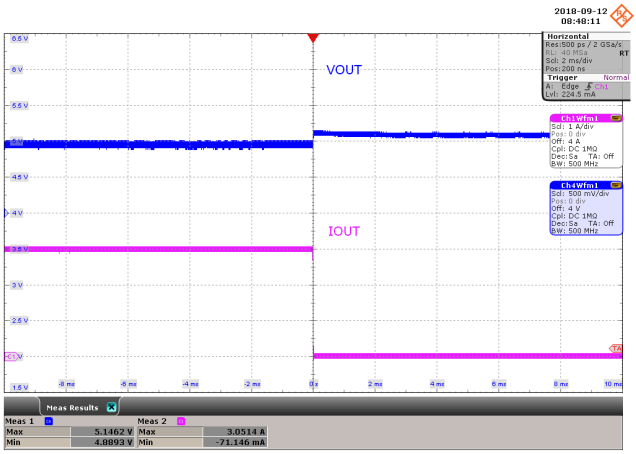

Figure 61 – Load Step Response (Falling).
85 VAC, 5.0 V, 3 – 0 A Load Step.
V_{MIN}: 4.88 V, V_{MAX}: 5.14 V.
Upper: V_{OUT}, 500 mV / div., 2 ms / div.
Lower: I_{LOAD}, 1 A / div.

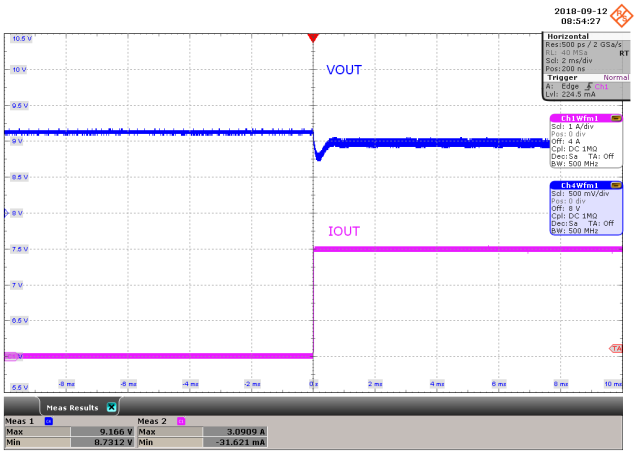

Figure 62 – Load Step Response (Rising).
85 VAC, 9.0 V, 0 – 3 A Load Step.
V_{MIN}: 8.73 V, V_{MAX}: 9.16 V.
Upper: V_{OUT}, 500 mV / div., 2 ms / div.
Lower: I_{LOAD}, 1 A / div.

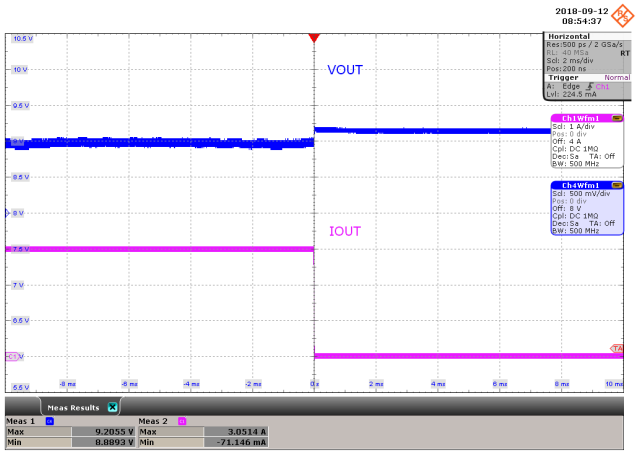

Figure 63 – Load Step Response (Falling).
85 VAC, 9.0 V, 3 – 0 A Load Step.
V_{MIN}: 8.88 V, V_{MAX}: 9.20 V.
Upper: V_{OUT}, 500 mV / div., 2 ms / div.
Lower: I_{LOAD}, 1 A / div.

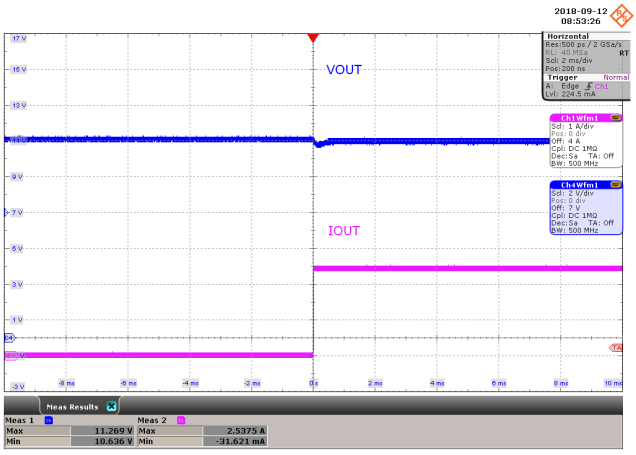

Figure 64 – Load Step Response (Rising).
85 VAC, 11.0 V, 0 – 2.45 A Load Step.
V_{MIN}: 10.63 V, V_{MAX}: 11.26 V.
Upper: V_{OUT}, 2 V / div., 2 ms / div.
Lower: I_{LOAD}, 1 A / div.

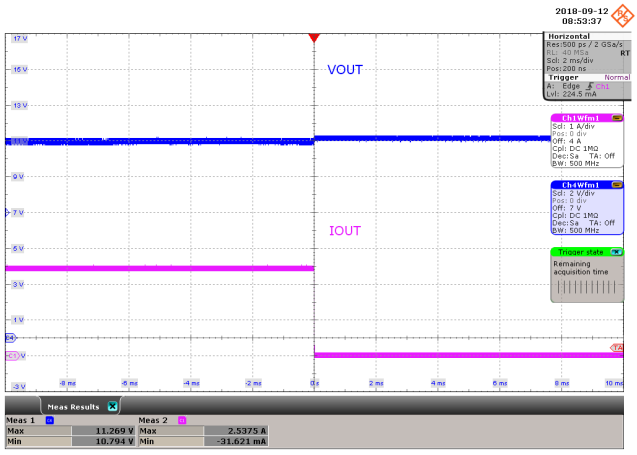

Figure 65 – Load Step Response (Falling).
85 VAC, 11.0 V, 2.45 – 0 A Load Step.
V_{MIN}: 10.79 V, V_{MAX}: 11.26 V.
Upper: V_{OUT}, 2 V / div., 2 ms / div.
Lower: I_{LOAD}, 1 A / div.

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14.1.2 Dynamic Load Response

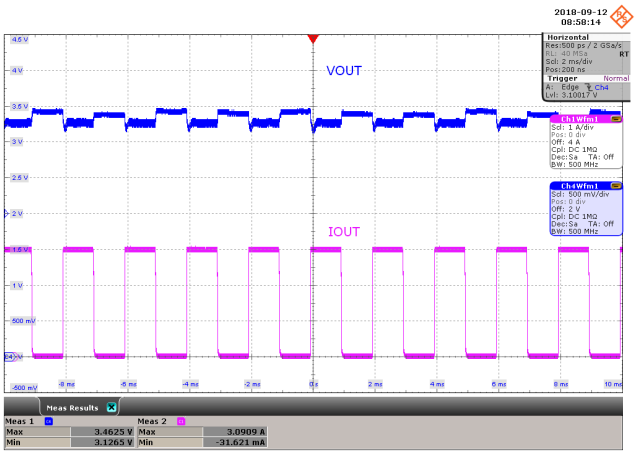

Figure 66 – Dynamic Load Response.
85 VAC, 3.3 V, 0 - 3 A Load.
V_{MIN}: 3.12 V, V_{MAX}: 3.46 V.
Upper: V_{OUT}, 500 mV / div., 2 ms / div.
Lower: I_{LOAD}, 1 A / div.

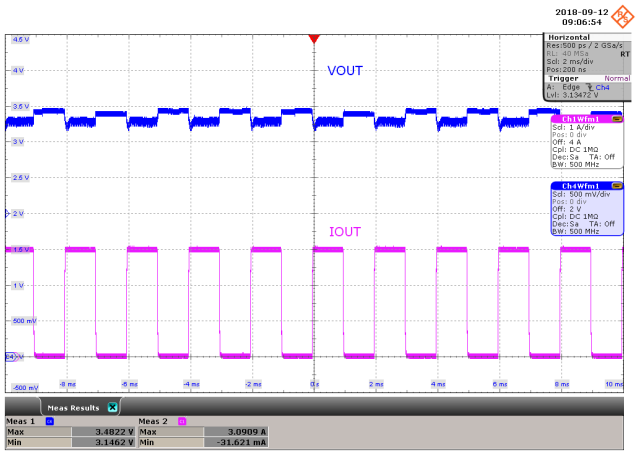

Figure 67 – Dynamic Load Response.
265 VAC, 3.3 V, 0 - 3 A Load.
V_{MIN}: 3.14 V, V_{MAX}: 3.48 V.
Upper: V_{OUT}, 500 mV / div., 2 ms / div.
Lower: I_{LOAD}, 1 A / div.

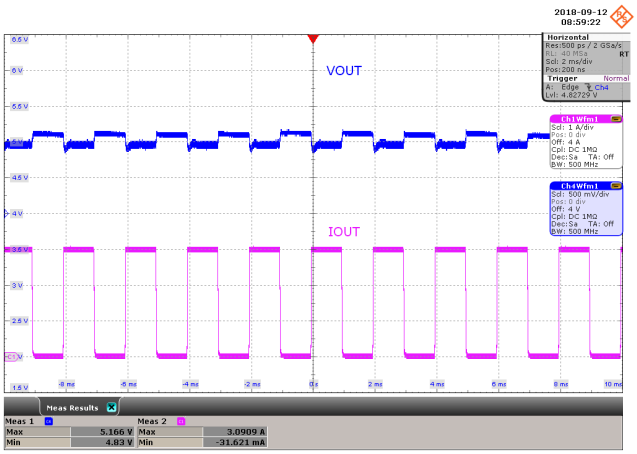

Figure 68 – Dynamic Load Response.
85 VAC, 5.0 V, 0 - 3 A Load.
V_{MIN}: 4.83 V, V_{MAX}: 5.16 V.
Upper: V_{OUT}, 500 mV / div., 2 ms / div.
Lower: I_{LOAD}, 1 A / div.

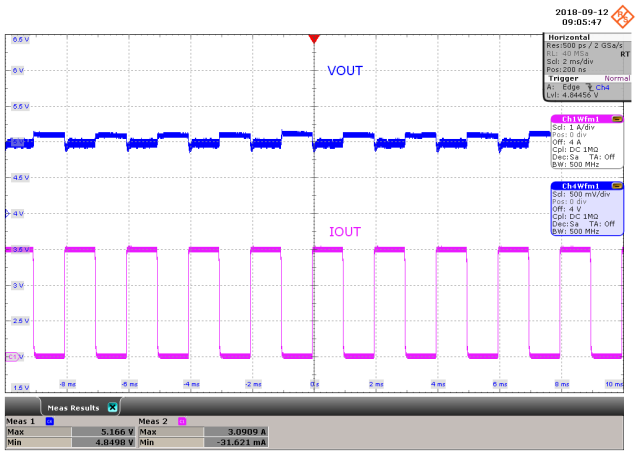

Figure 69 – Dynamic Load Response.
265 VAC, 5.0 V, 0 - 3 A Load.
V_{MIN}: 4.84 V, V_{MAX}: 5.16 V.
Upper: V_{OUT}, 500 mV / div., 2 ms / div.
Lower: I_{LOAD}, 1 A / div.

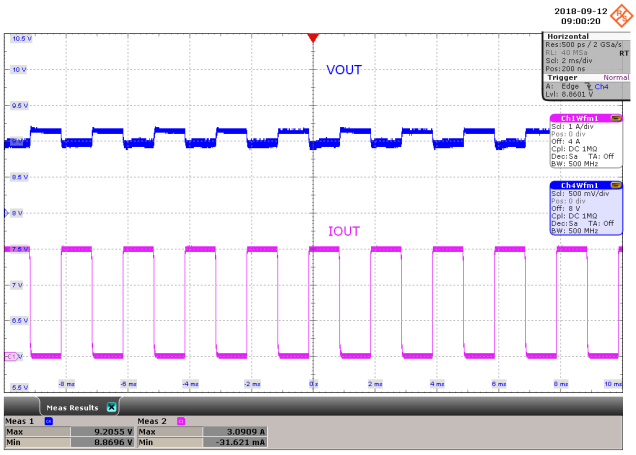

Figure 70 – Dynamic Load Response.
85 VAC, 9.0 V, 0 - 3 A Load.
V_{MIN}: 8.86 V, V_{MAX}: 9.20 V.
Upper: V_{OUT}, 500 mV / div., 2 ms / div.
Lower: I_{LOAD}, 1 A / div.

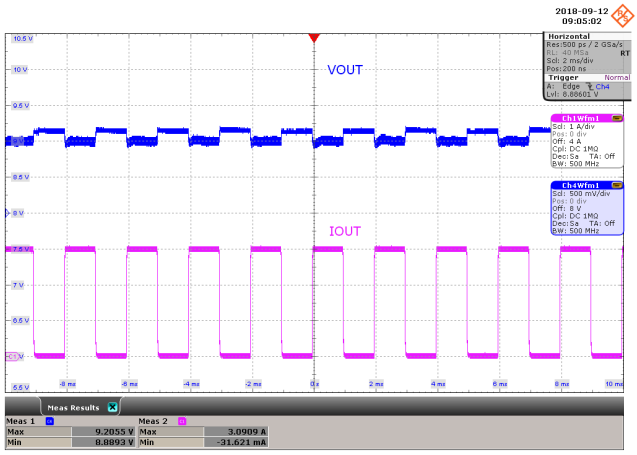

Figure 71 – Dynamic Load Response.
265 VAC, 9.0 V, 0 - 3 A Load.
V_{MIN}: 8.88 V, V_{MAX}: 9.20 V.
Upper: V_{OUT}, 500 mV / div., 2 ms / div.
Lower: I_{LOAD}, 1 A / div.

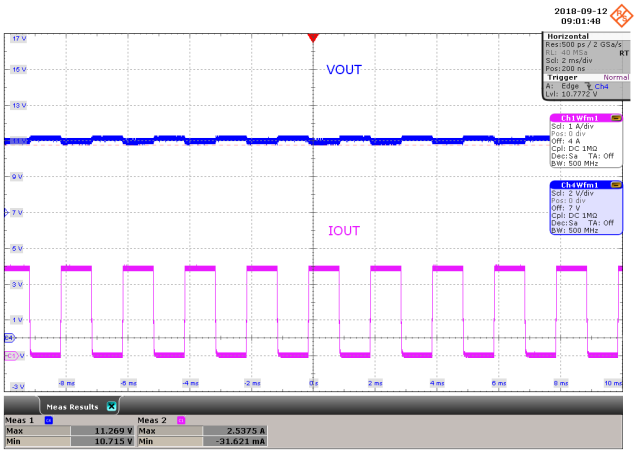

Figure 72 – Dynamic Load Response.
85 VAC, 11.0 V, 0 - 2.45 A Load.
V_{MIN}: 10.71 V, V_{MAX}: 11.26 V.
Upper: V_{OUT}, 2 V / div., 2 ms / div.
Lower: I_{LOAD}, 1 A / div.

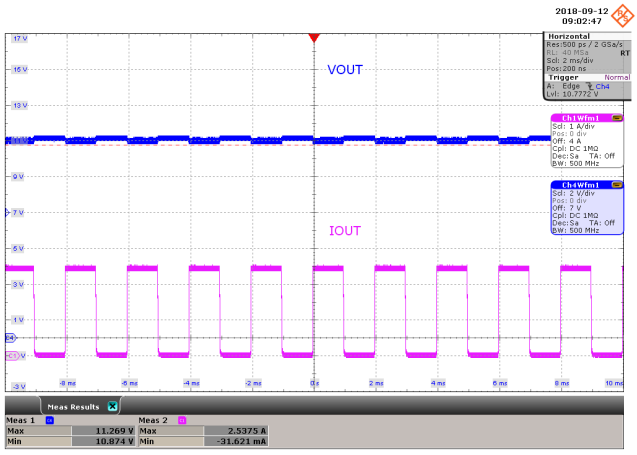

Figure 73 – Dynamic Load Response.
265 VAC, 11.0 V, 0 - 2.45 A Load.
V_{MIN}: 10.87 V, V_{MAX}: 11.26 V.
Upper: V_{OUT}, 2 V / div., 2 ms / div.
Lower: I_{LOAD}, 1 A / div.

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14.2 Switching Waveforms

14.2.1 Drain Voltage and Current

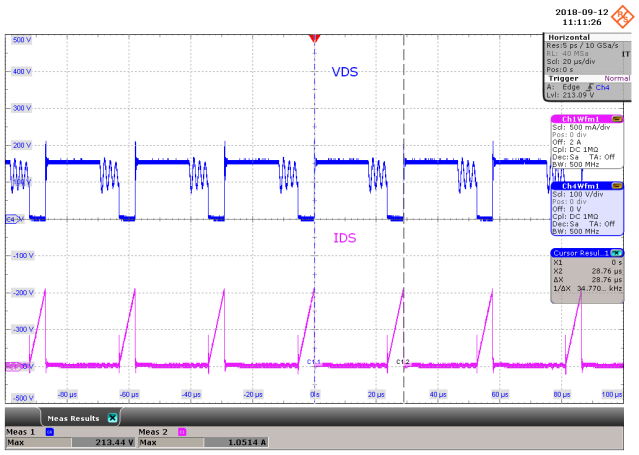

Figure 74 – Drain Voltage and Current Waveforms.
85 VAC, 3.3 V, 3 A Load (213 V_{MAX}).
Upper: V_{DRAIN}, 100 V / div., 20 µs / div.
Lower: I_{DRAIN}, 500 mA / div.

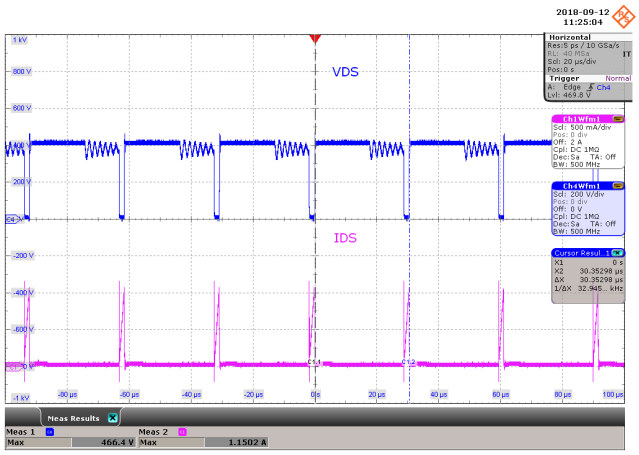

Figure 75 – Drain Voltage and Current Waveforms.
265 VAC, 3.3 V, 3 A Load (466 V_{MAX}).
Upper: V_{DRAIN}, 200 V / div., 20 µs / div.
Lower: I_{DRAIN}, 500 mA / div.

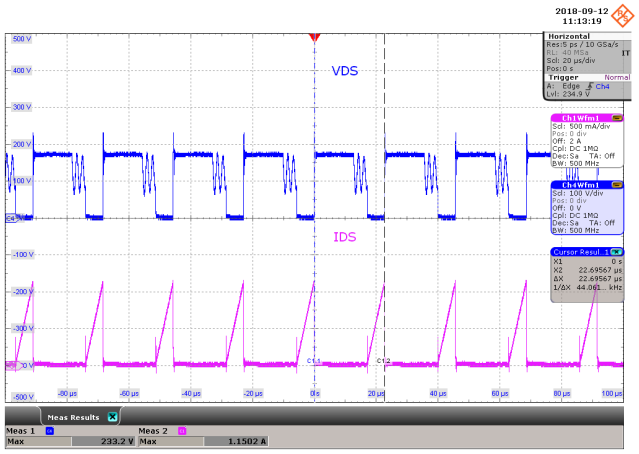

Figure 76 – Drain Voltage and Current Waveforms.
85 VAC, 5.0 V, 3 A Load (233 V_{MAX}).
Upper: V_{DRAIN}, 100 V / div., 20 µs / div.
Lower: I_{DRAIN}, 500 mA / div.

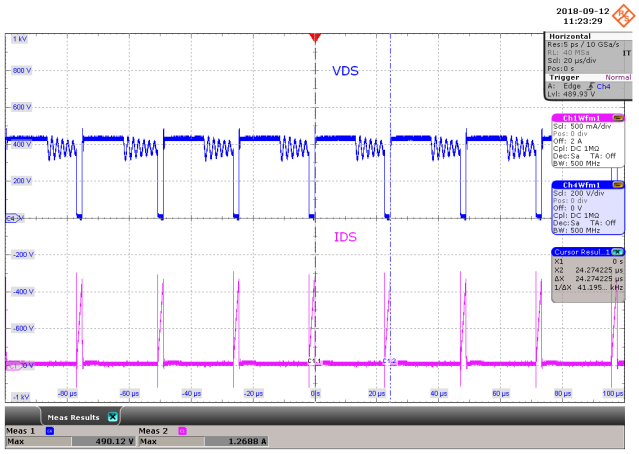

Figure 77 – Drain Voltage and Current Waveforms.
265 VAC, 5.0 V, 3 A Load (490 V_{MAX}).
Upper: V_{DRAIN}, 200 V / div., 20 µs / div.
Lower: I_{DRAIN}, 500 mA / div.

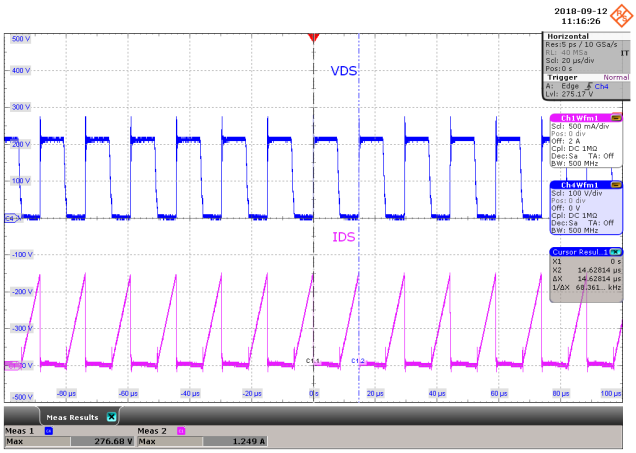

Figure 78 – Drain Voltage and Current Waveforms.
85 VAC, 9.0 V, 3 A Load (276 V_{MAX}).
Upper: V_{DRAIN}, 100 V / div., 20 µs / div.
Lower: I_{DRAIN}, 500 mA / div.

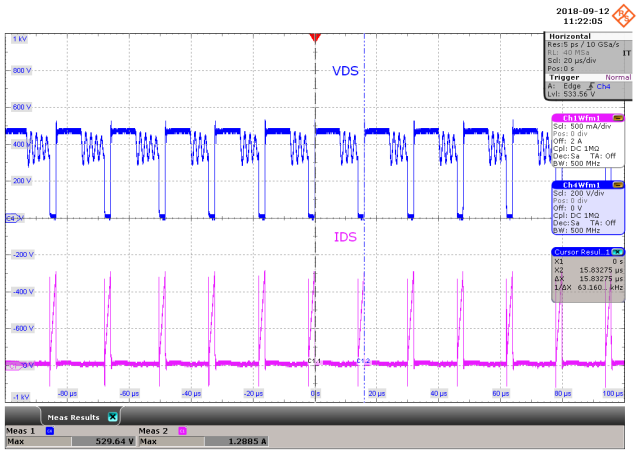

Figure 79 – Drain Voltage and Current Waveforms.
265 VAC, 9.0 V, 3 A Load (529 V_{MAX}).
Upper: V_{DRAIN}, 200 V / div., 20 µs / div.
Lower: I_{DRAIN}, 500 mA / div.

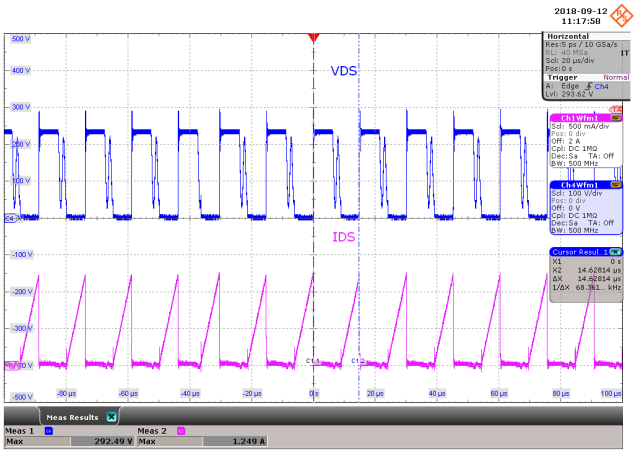

Figure 80 – Drain Voltage and Current Waveforms.
85 VAC, 11.0 V, 2.45 A Load (292 V_{MAX}).
Upper: V_{DRAIN}, 100 V / div., 20 µs / div.
Lower: I_{DRAIN}, 500 mA / div.

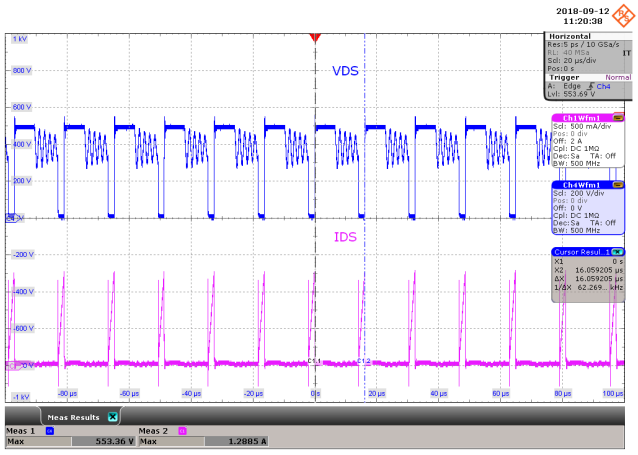

Figure 81 – Drain Voltage and Current Waveforms.
265 VAC, 11.0 V, 2.45 A Load (553 V_{MAX}).
Upper: V_{DRAIN}, 200 V / div., 20 µs / div.
Lower: I_{DRAIN}, 500 mA / div.

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14.2.2 Drain Voltage and Current During Output Voltage Transition

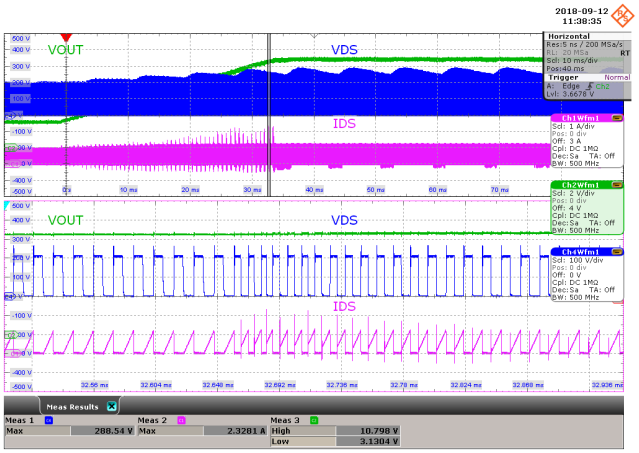

Figure 82 – Drain Voltage, Current, and Output Voltage Waveforms.
85 VAC, 3.3 V – 11.0 V, 2.45 A Load (288 V_{MAX}).
V_{DRAIN}, 100 V / div., 10 ms / div.
I_{DRAIN}, 500 mA / div.
V_{OUT}, 2 V / div.

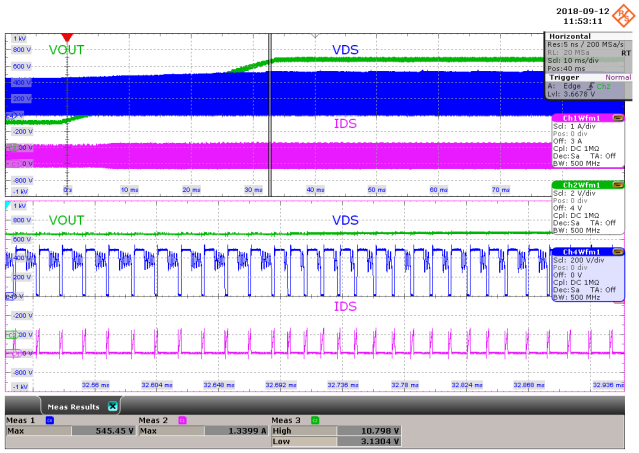

Figure 83 – Drain Voltage, Current, and Output Voltage Waveforms.
265 VAC, 3.3 V – 11.0 V, 2.45 A Load (545 V_{MAX}).
V_{DRAIN}, 200 V / div., 10 ms / div.
I_{DRAIN}, 500 mA / div.
V_{OUT}, 2 V / div.

14.2.3 Drain Voltage and Current at Start-up

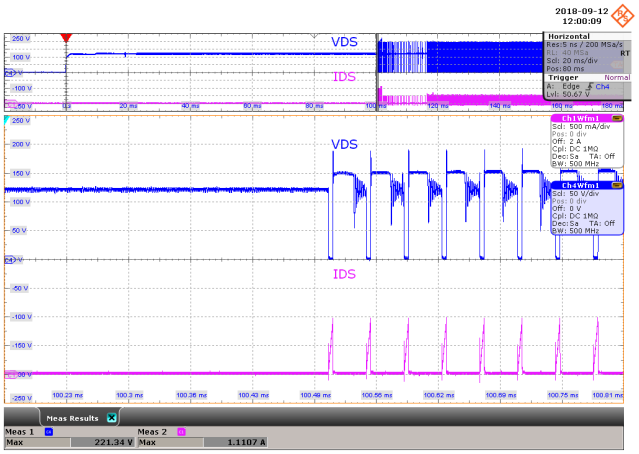

Figure 84 – Drain Voltage and Current Waveforms.
85 VAC, 5.0 V, 3.0 A Load (221 V_{MAX}).
Upper: V_{DRAIN}, 50 V / div., 20 ms / div.
Lower: I_{DRAIN}, 500 mA / div.

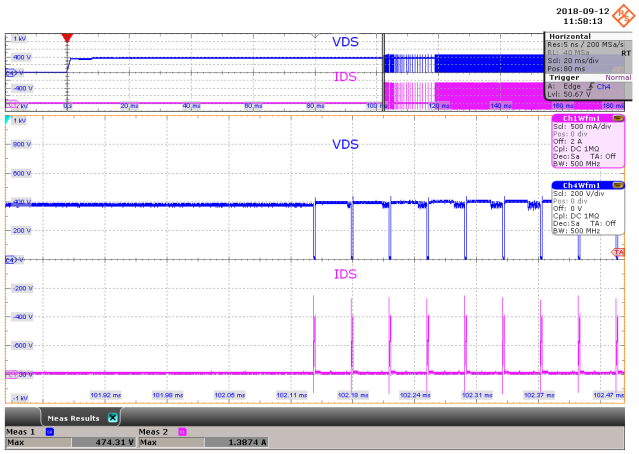

Figure 85 – Drain Voltage and Current Waveforms.
265 VAC, 5.0 V, 3.0 A Load (474 V_{MAX}).
Upper: V_{DRAIN}, 200 V / div., 20 ms / div.
Lower: I_{DRAIN}, 500 mA / div.

14.2.4 SR FET Voltage

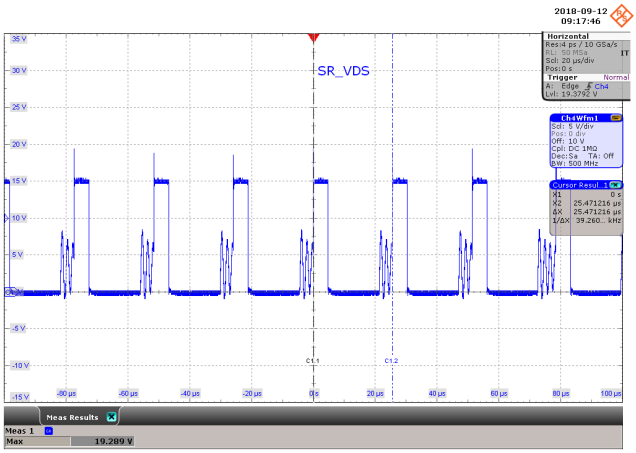

Figure 86 – SR FET Voltage Waveform.
85 VAC, 3.3 V, 3 A Load (19.28 V_{MAX}).
SR_V_{DRAIN}, 5 V / div., 20 µs / div.

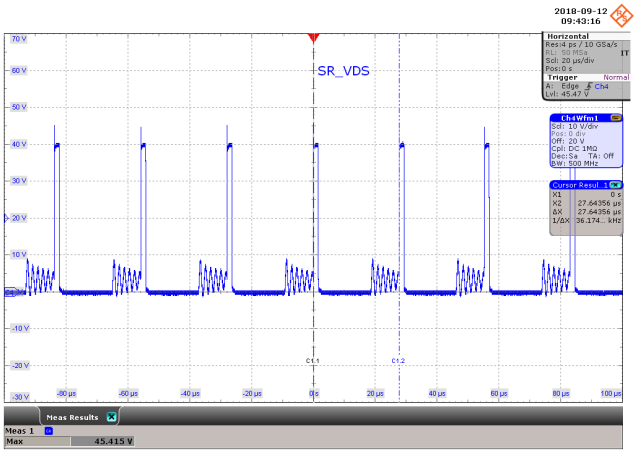

Figure 87 – SR FET Voltage Waveform.
265 VAC, 3.3 V, 3 A Load (45.41 V_{MAX}).
SR_V_{DRAIN}, 10 V / div., 20 µs / div.

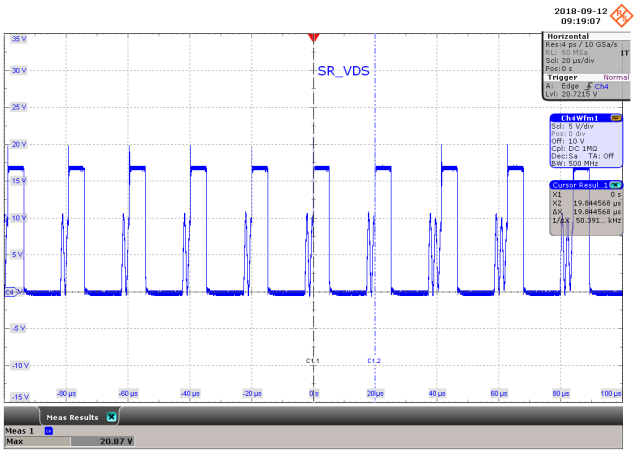

Figure 88 – SR FET Voltage Waveform.
85 VAC, 5.0 V, 3 A Load (20.87 V_{MAX}).
SR_V_{DRAIN}, 5 V / div., 20 µs / div.

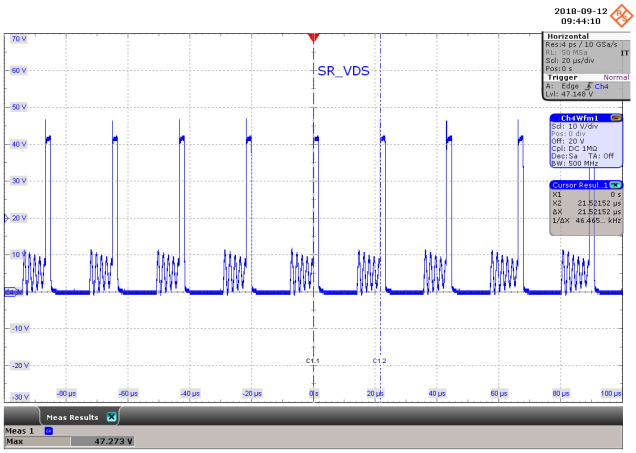

Figure 89 – SR FET Voltage Waveform.
265 VAC, 5.0 V, 3 A Load (47.27 V_{MAX}).
SR_V_{DRAIN}, 10 V / div., 20 µs / div.

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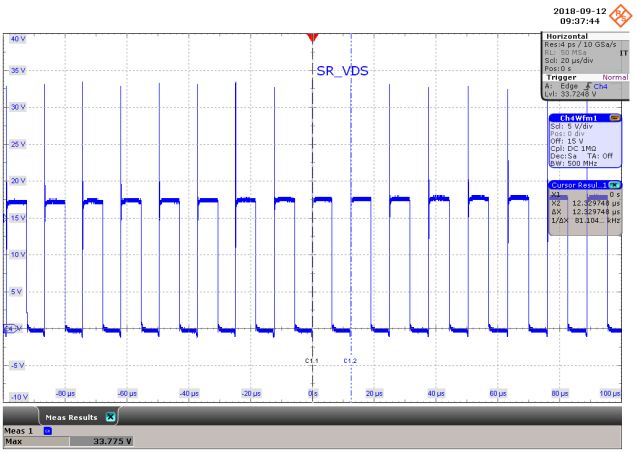

Figure 90 – SR FET Voltage Waveform.
85 VAC, 9.0 V, 3 A Load (33.77 V_{MAX}).
SR_V_{DRAIN}, 5 V / div., 20 µs / div.

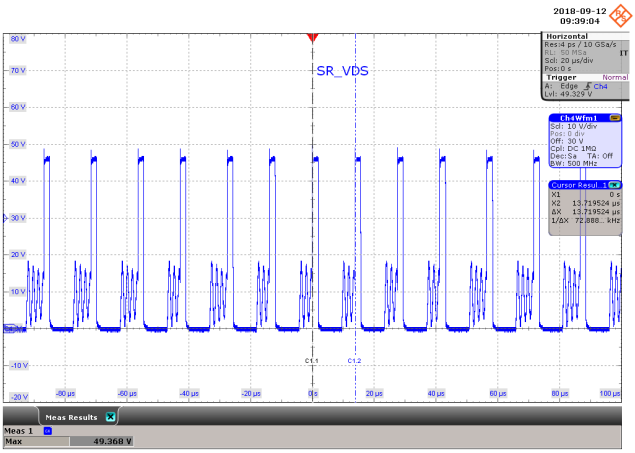

Figure 91 – SR FET Voltage Waveform.
265 VAC, 9.0 V, 3 A Load (49.36 V_{MAX}).
SR_V_{DRAIN}, 10 V / div., 20 µs / div.

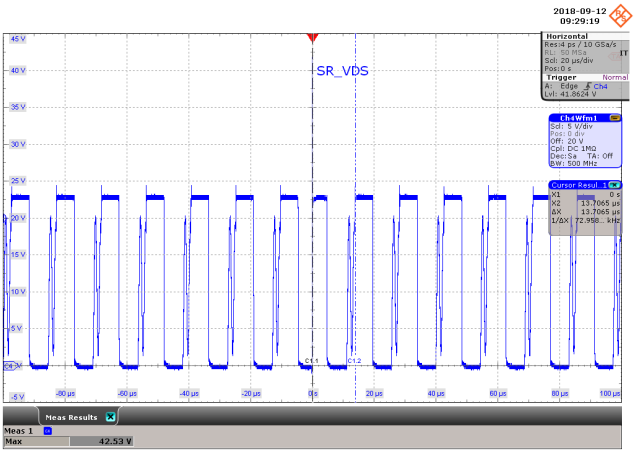

Figure 92 – SR FET Voltage Waveform.
85 VAC, 11.0 V, 2.45 A Load (42.53 V_{MAX}).
SR_V_{DRAIN}, 5 V / div., 20 µs / div.

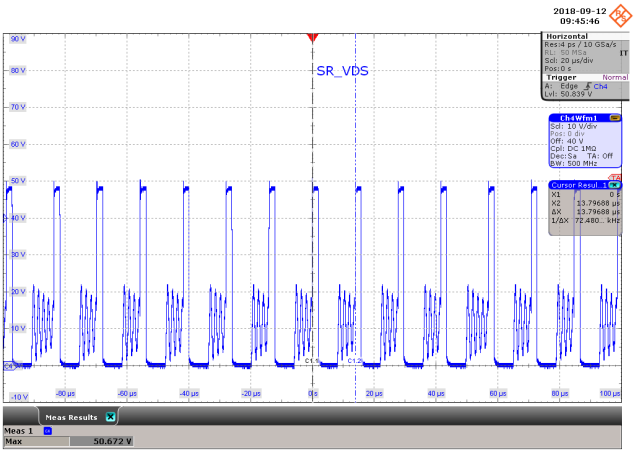

Figure 93 – SR FET Voltage Waveform.
265 VAC, 11.0 V, 2.45 A Load (50.67 V_{MAX}).
SR_V_{DRAIN}, 10 V / div., 20 µs / div.

14.2.5 SR FET Voltage During Output Voltage Transition

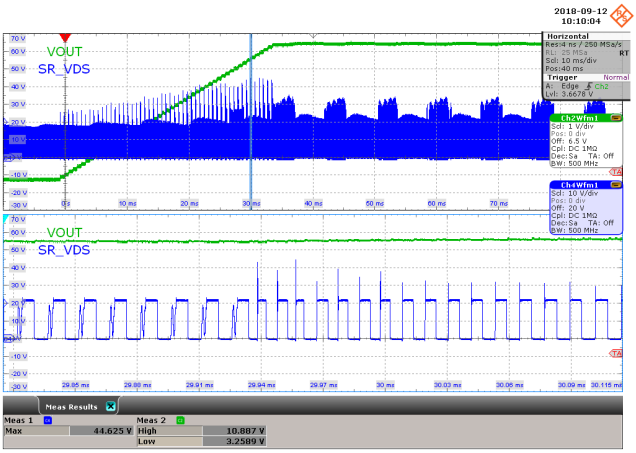

Figure 94 – SR FET and Output Voltage Waveforms.
85 VAC, 3.3 V – 11.0 V, 2.45 A Load
(44.62 V_{MAX}).
SR_V_{DRAIN}, 10 V / div., 10 ms / div.
V_{OUT}, 1 V / div.

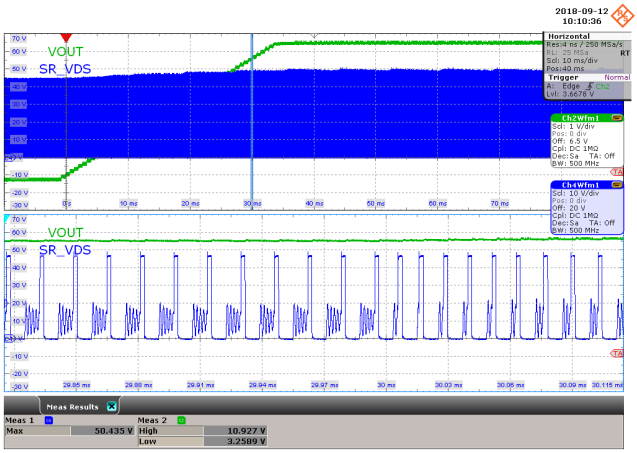

Figure 95 – SR FET and Output Voltage Waveforms.
265 VAC, 3.3 V – 11.0 V, 2.45 A Load
(50.43 V_{MAX}).
SR_V_{DRAIN}, 10 V / div., 10 ms / div.
V_{OUT}, 1 V / div.

14.3 Output Voltage and Current at Start-up (On the Board)

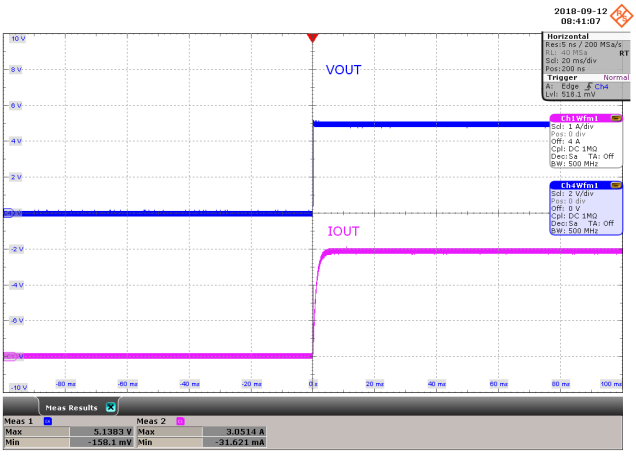

Figure 96 – Output Voltage and Current Waveforms.
85 VAC, 5 V, 3 A Load.
Upper: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A / div., 20 ms / div.

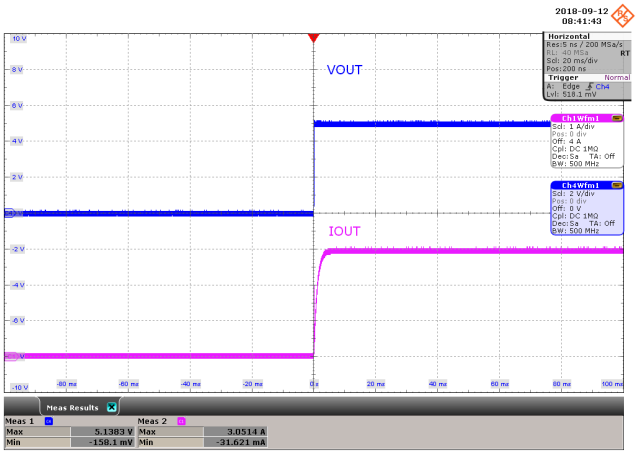

Figure 97 – Output Voltage and Current Waveforms.
265 VAC, 5 V, 3 A Load.
Upper: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A / div., 20 ms / div.

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15 Voltage and Current Step Test using Quadramax and Total Phase Analyzer

15.1 Voltage Step Test (VST)

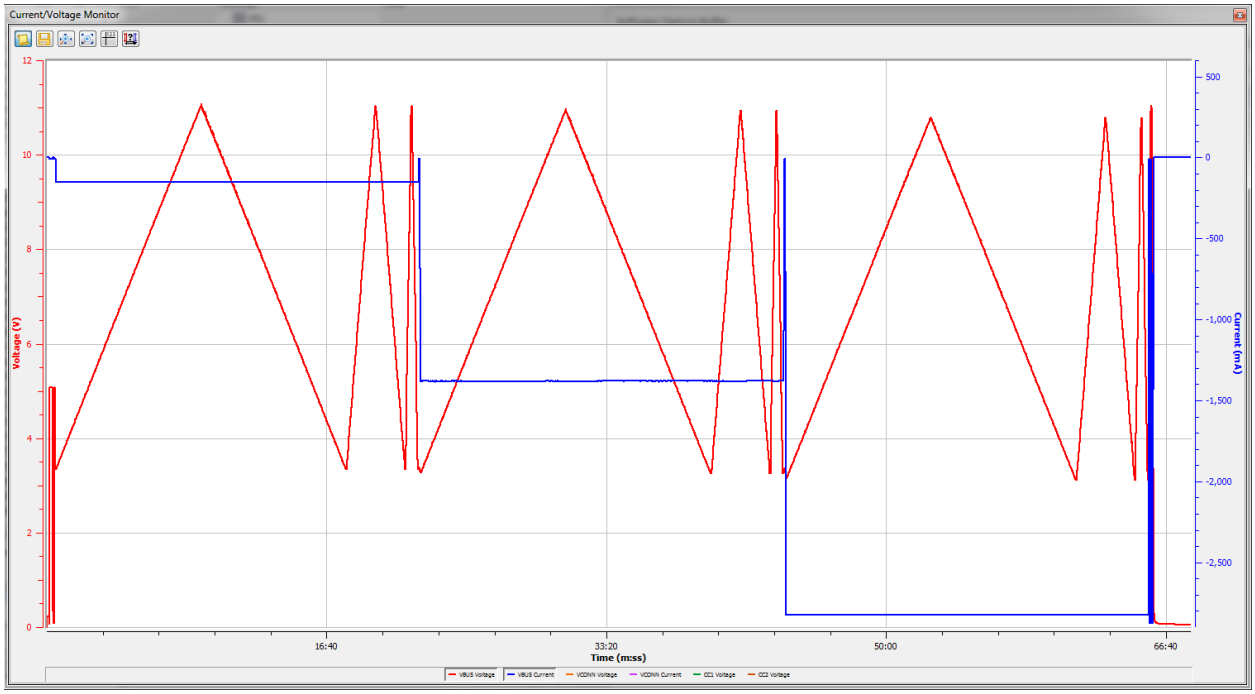

Figure 98 – Plot of SPT.6 VST from Total Phase Analyzer.

15.2 Current Limit Test (CLT)

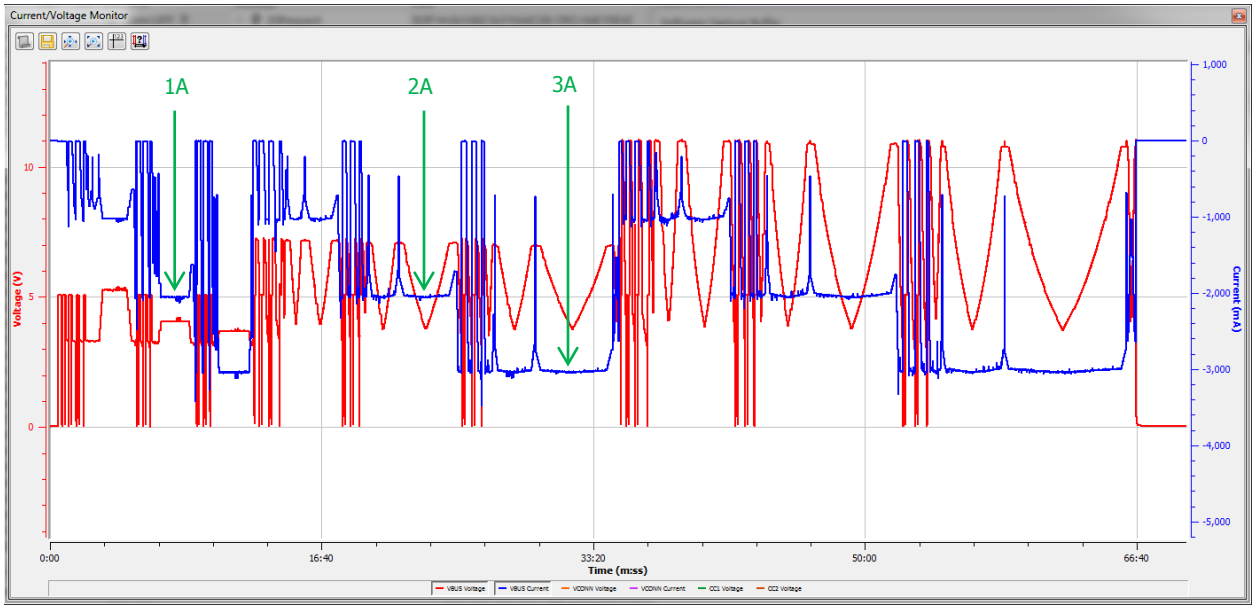

Figure 99 – Plot of SPT.7 CLT from Total Phase Analyzer.

16 Conducted EMI

16.1 Floating Output

16.1.1 Output: 5 V / 3 A

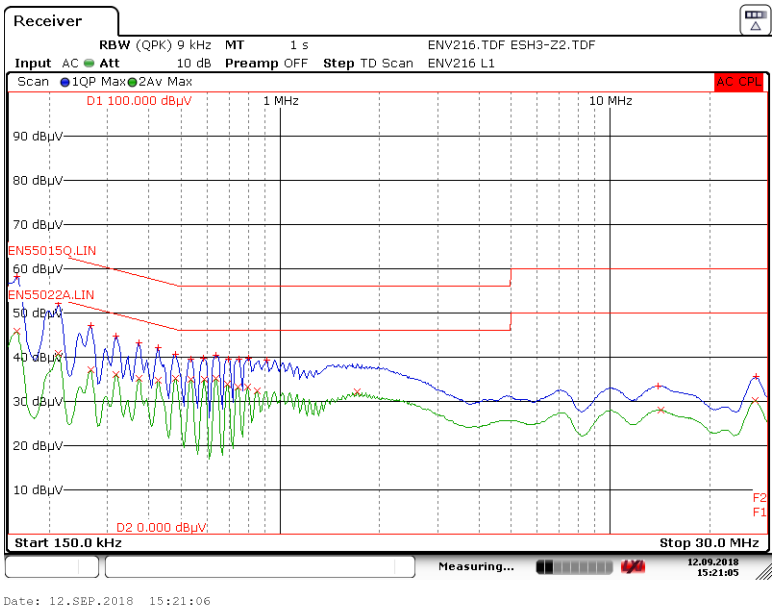

Figure 100 – Floating Ground EMI, 5 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

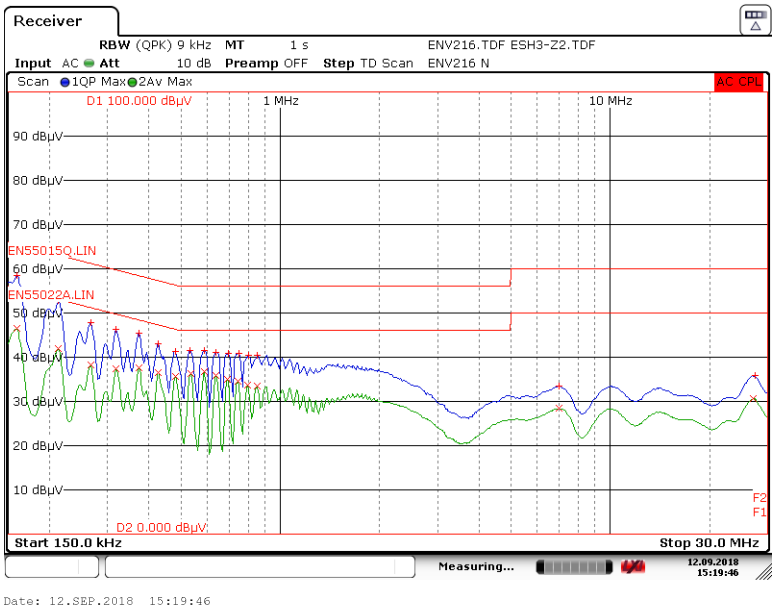

Figure 101 – Floating Ground EMI, 5 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

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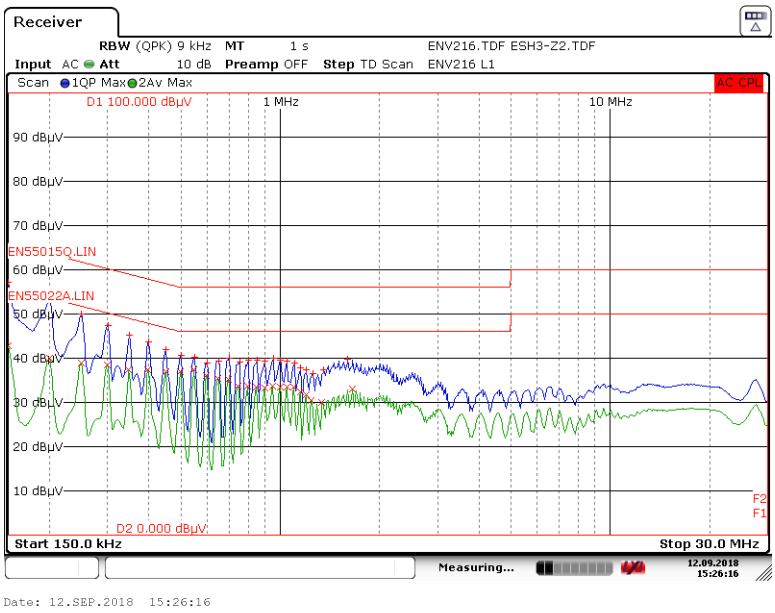

Figure 102 – Floating Ground EMI, 5 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).

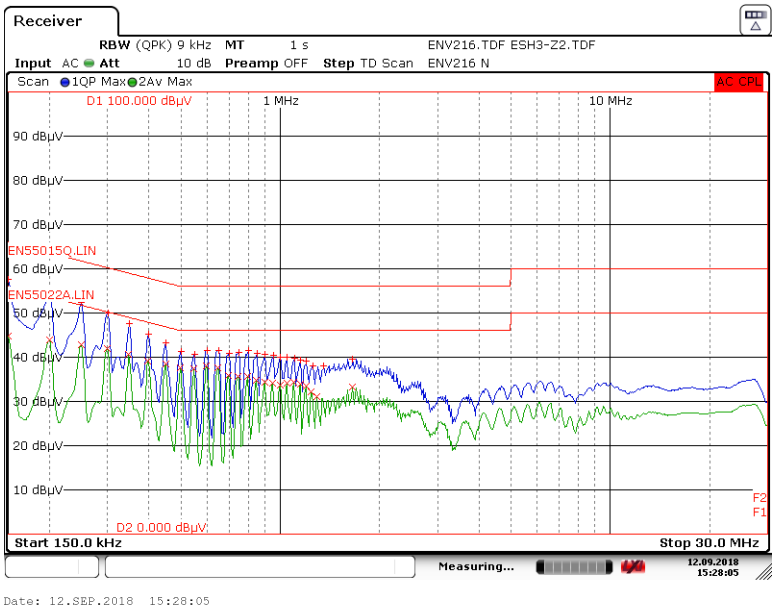

Figure 103 – Floating Ground EMI, 5 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).

16.1.2 Output: 9 V / 3 A

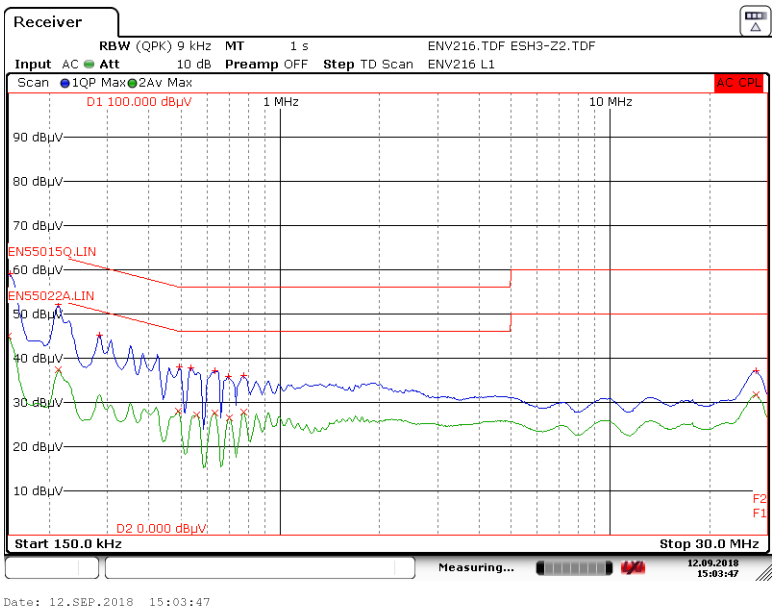

Figure 104 – Floating Ground EMI, 9 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

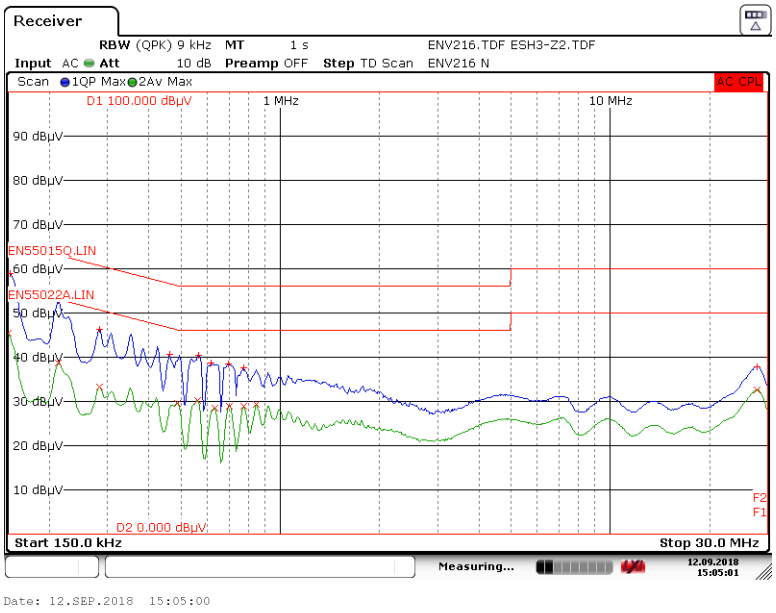

Figure 105 – Floating Ground EMI, 9 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

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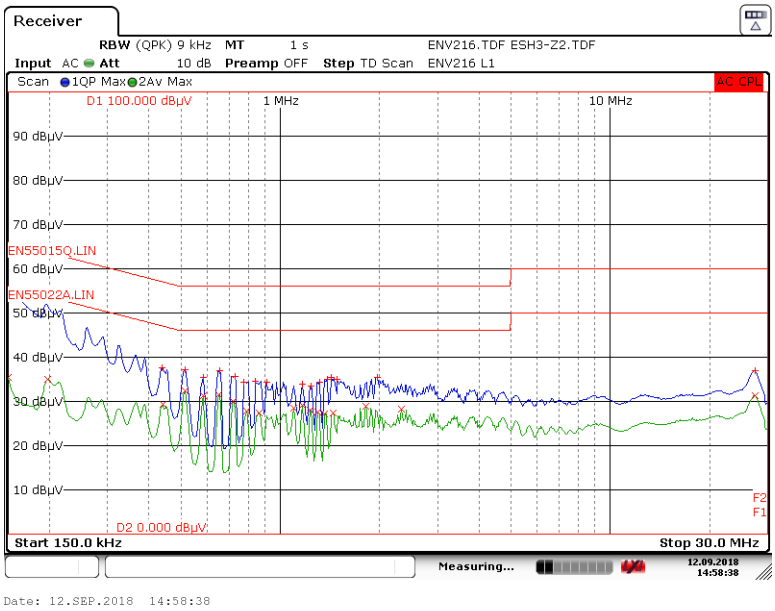

Figure 106 – Floating Ground EMI, 9 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).

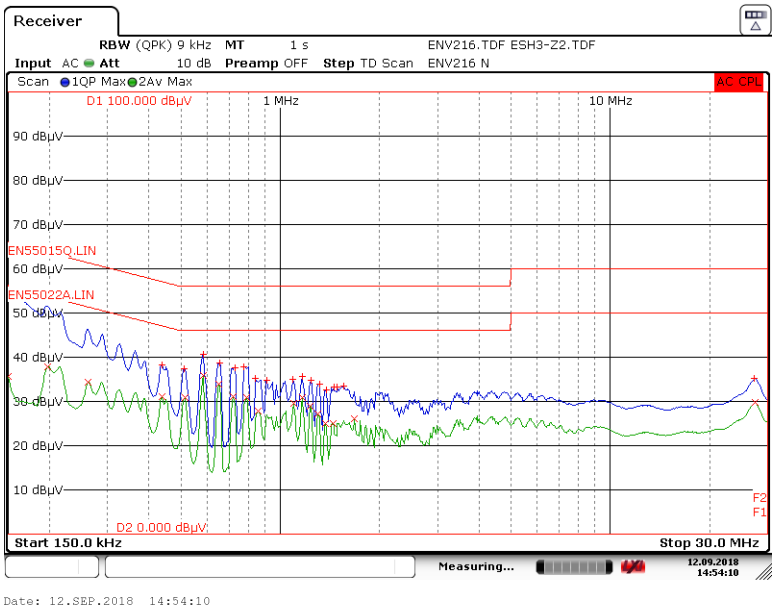

Figure 107 – Floating Ground EMI, 9 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).

16.1.3 Output: 11 V / 2.45 A

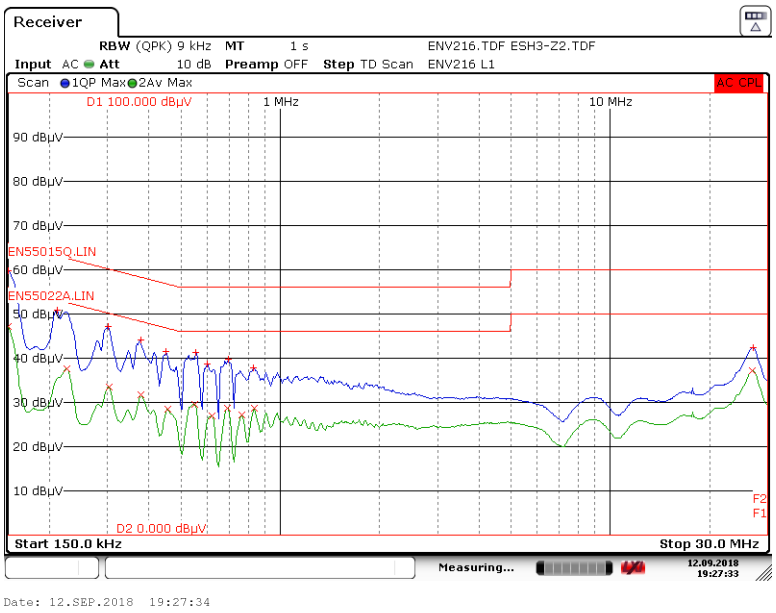

Figure 108 – Floating Ground EMI, 11 V / 2.45 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

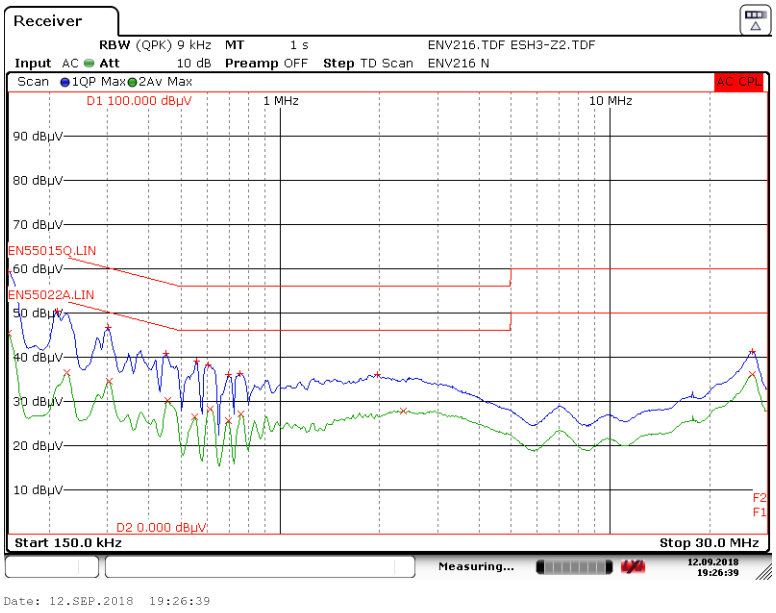

Figure 109 – Floating Ground EMI, 11 V / 2.45 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

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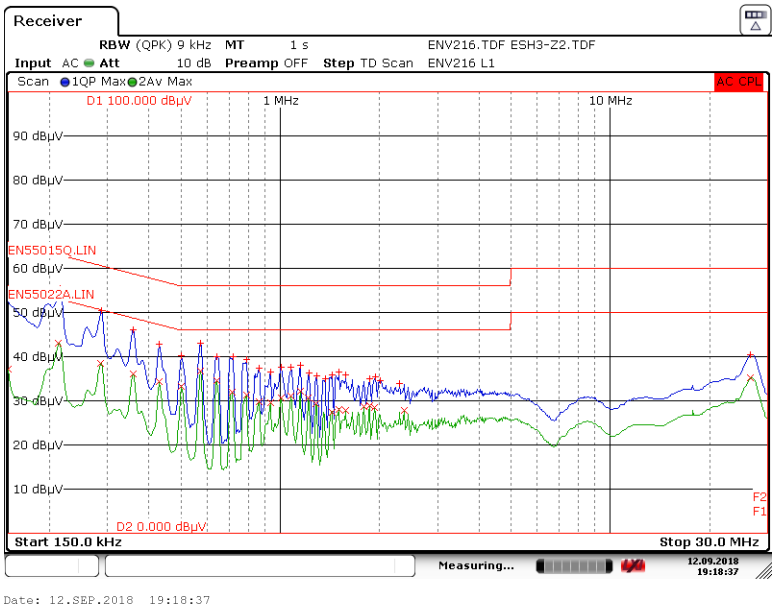

Figure 110 – Floating Ground EMI, 11 V / 2.45 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).

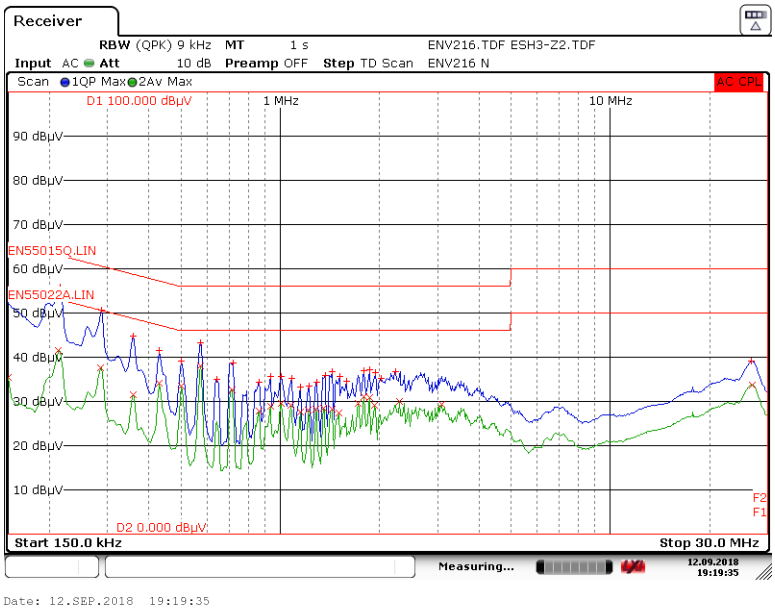

Figure 111 – Floating Ground EMI, 11 V / 2.45 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).

16.2 Artificial Hand

16.2.1 Output: 5 V / 3 A

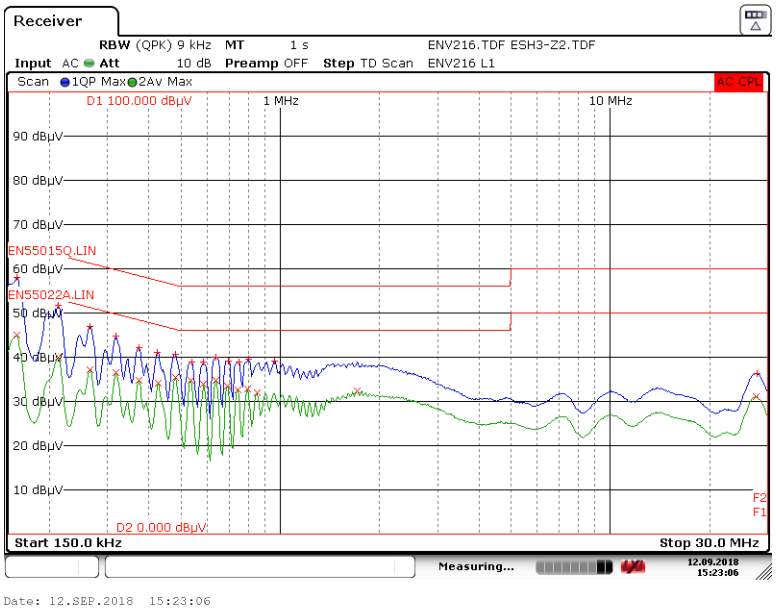

Figure 112 – Artificial Hand EMI, 5 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

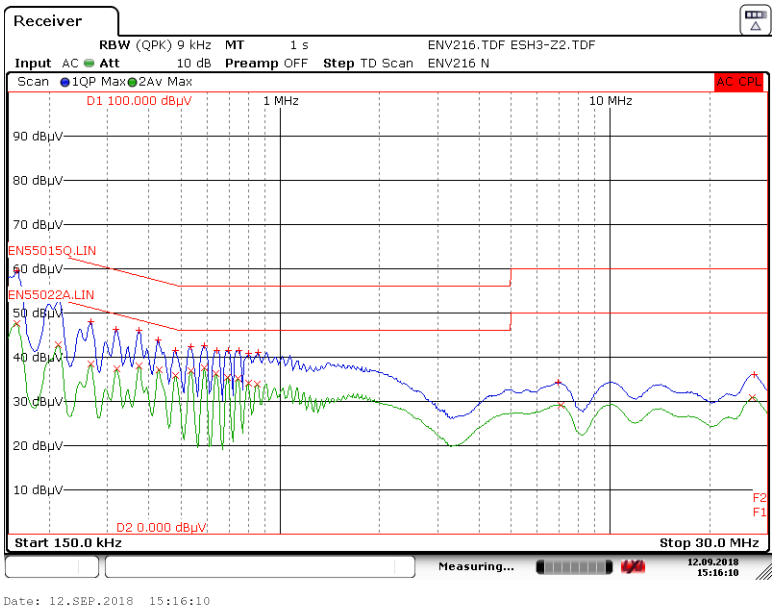

Figure 113 – Artificial Hand EMI, 5 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

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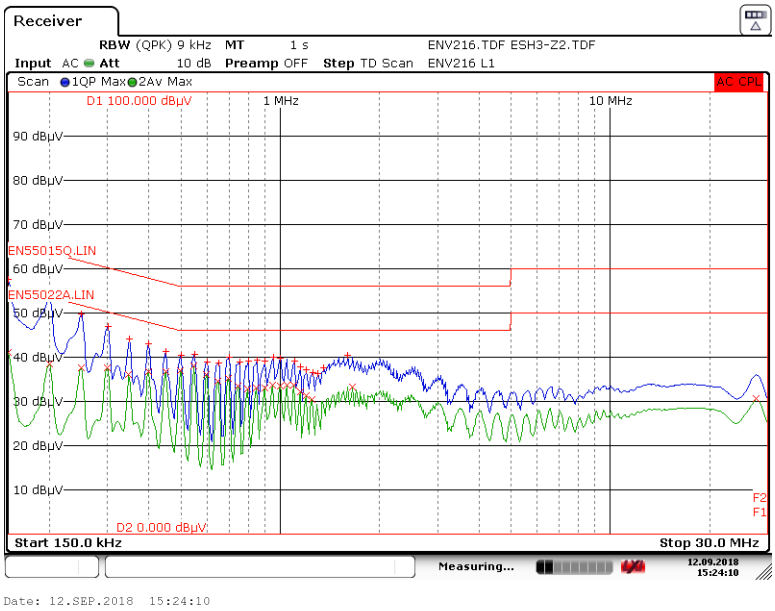

Figure 114 – Artificial Hand EMI, 5 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).

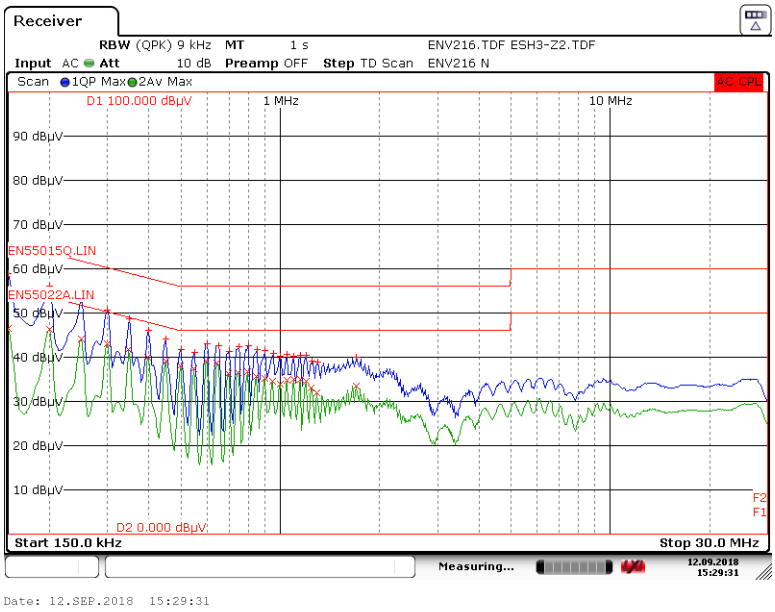

Figure 115 – Artificial Hand EMI, 5 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).

16.2.2 Output: 9 V / 3 A

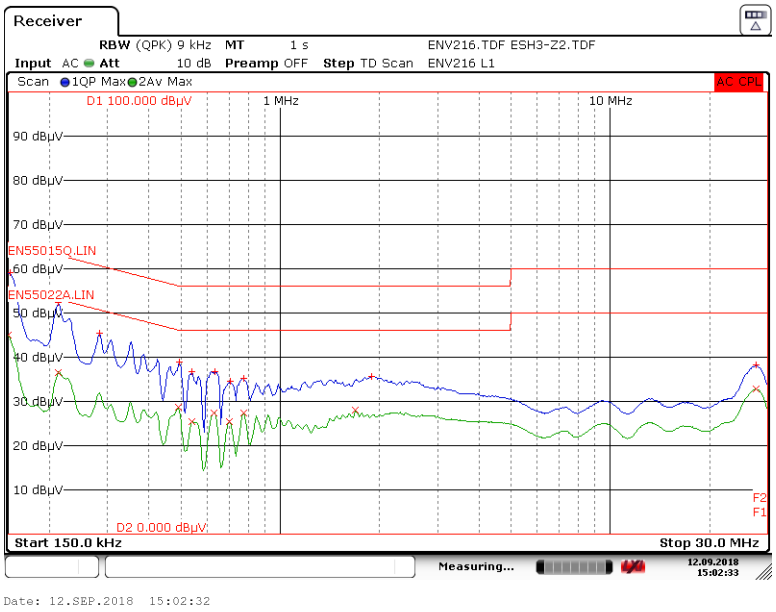

Figure 116 – Artificial Hand EMI, 9 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

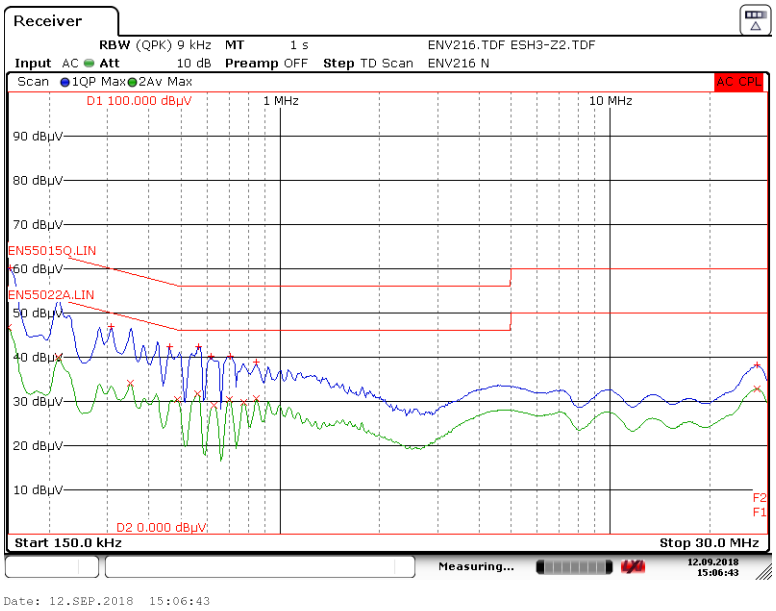

Figure 117 – Artificial Hand EMI, 9 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

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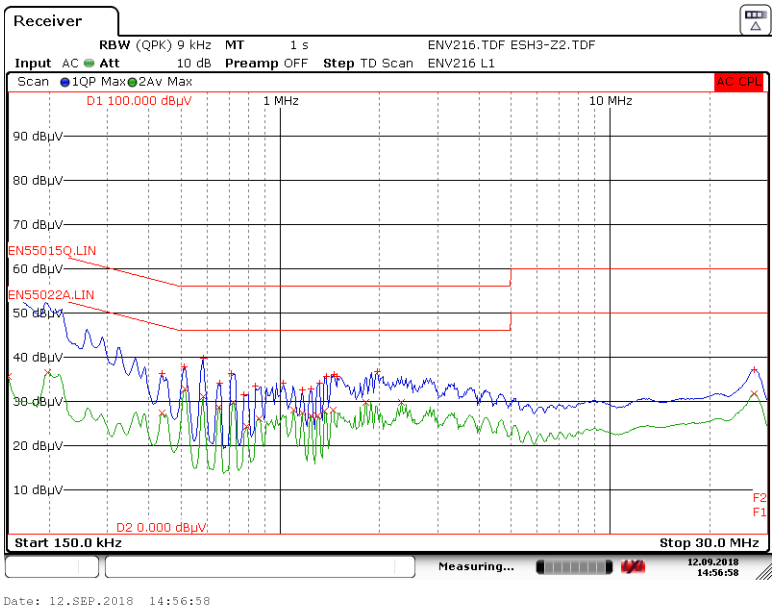

Figure 118 – Artificial Hand EMI, 9 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).

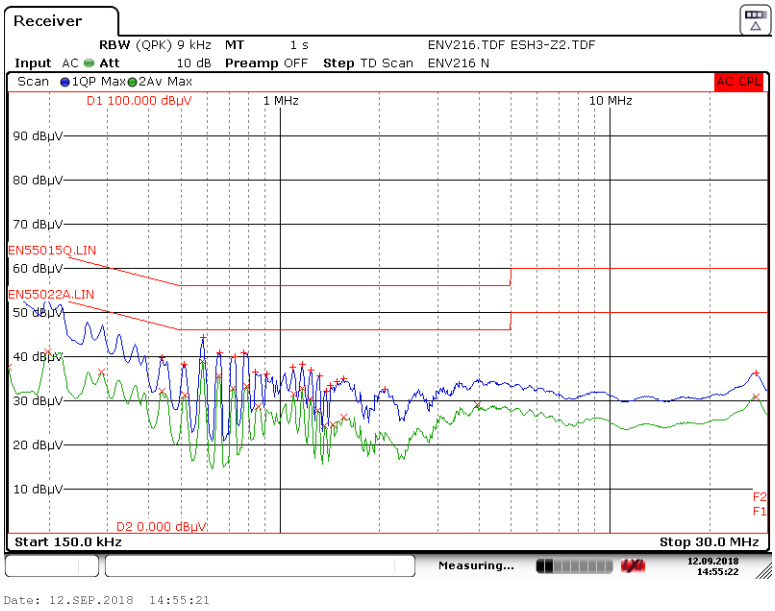

Figure 119 – Artificial Hand EMI, 9 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).

16.2.3 Output: 11 V / 2.45 A

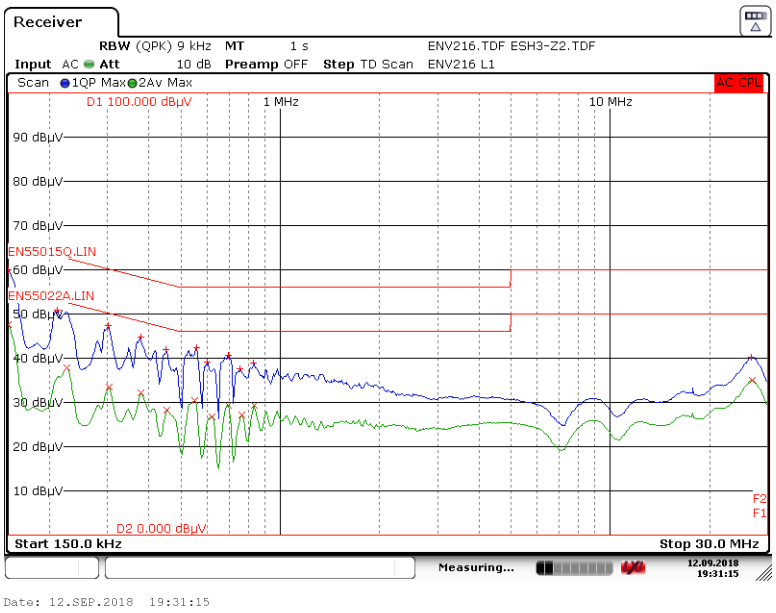

Figure 120 – Artificial Hand EMI, 11 V / 2.45 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

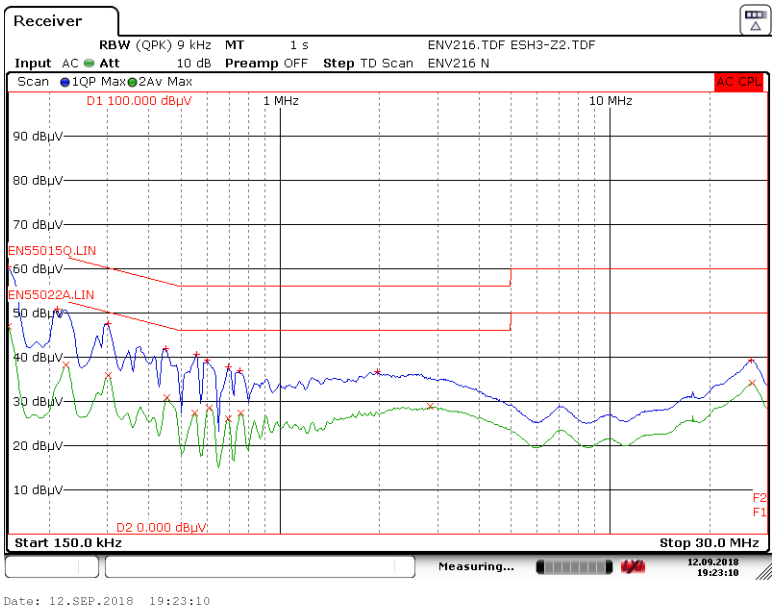

Figure 121 – Artificial Hand EMI, 11 V / 2.45 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

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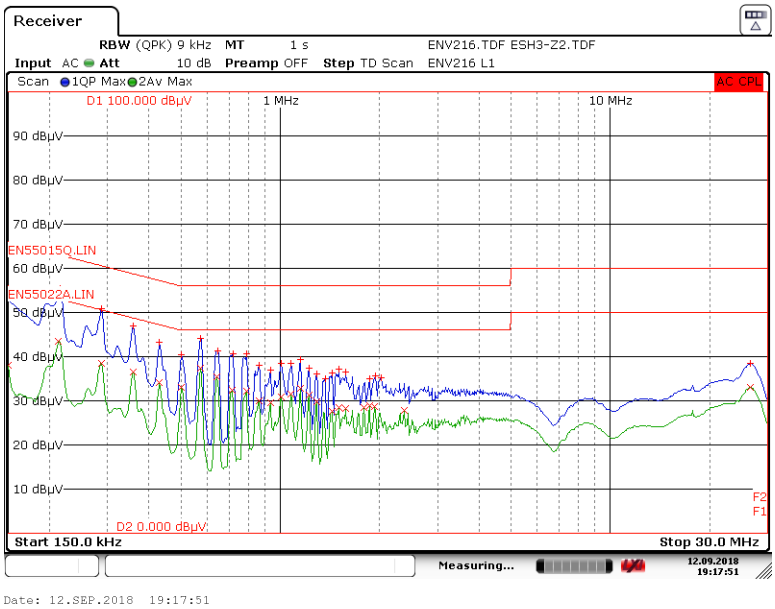

Figure 122 – Artificial Hand EMI, 11 V / 2.45 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).

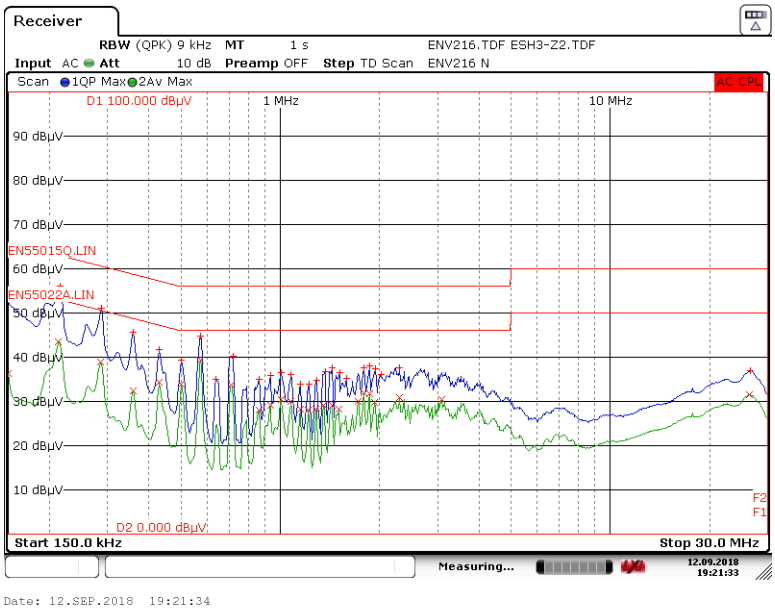

Figure 123 – Artificial Hand EMI, 11 V / 2.45 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).

16.3 Earth Ground

16.3.1 Output: 5 V / 3 A

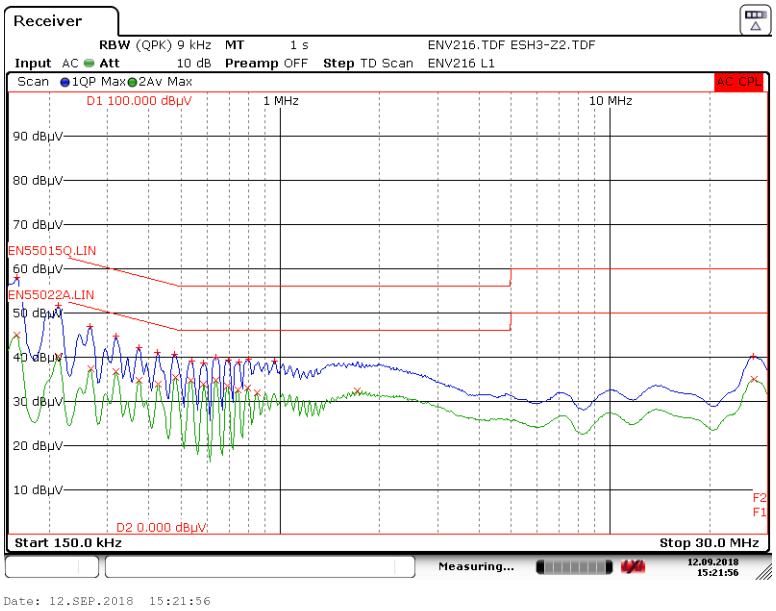

Figure 124 – Earth Ground EMI, 5 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

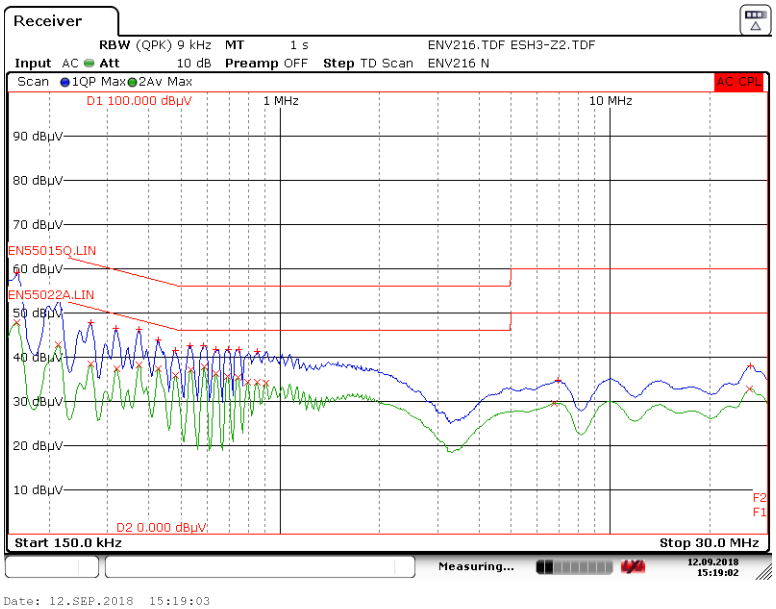

Figure 125 – Earth Ground EMI, 5 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

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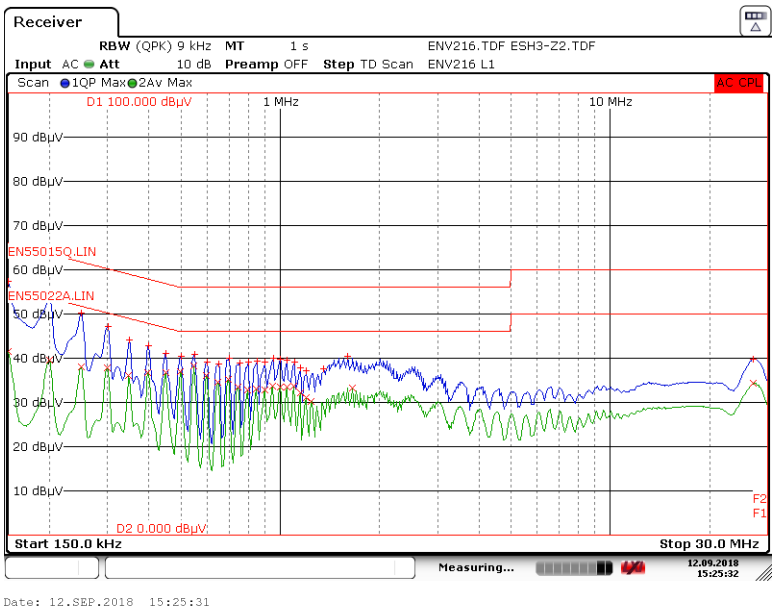

Figure 126 – Earth Ground EMI, 5 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).

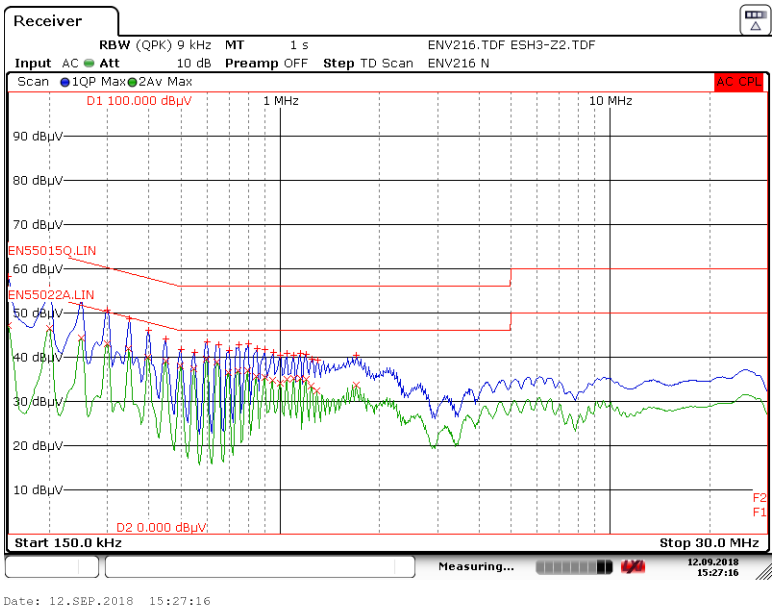

Figure 127 – Earth Ground EMI, 5 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).

16.3.2 Output: 9 V / 3 A

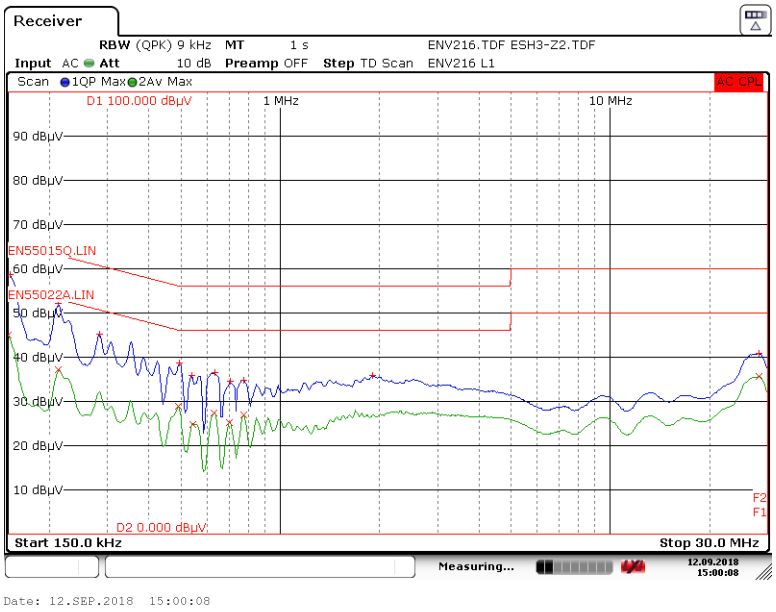

Figure 128 – Earth Ground EMI, 9 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

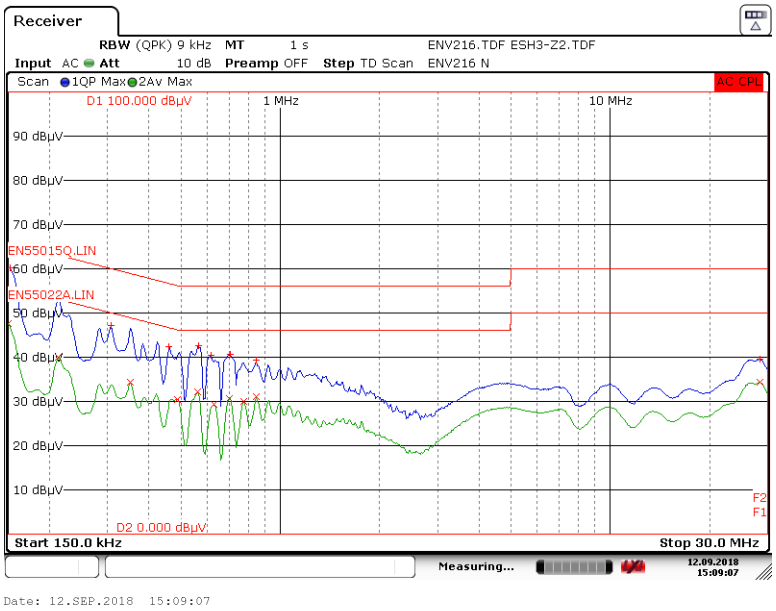

Figure 129 – Earth Ground EMI, 9 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

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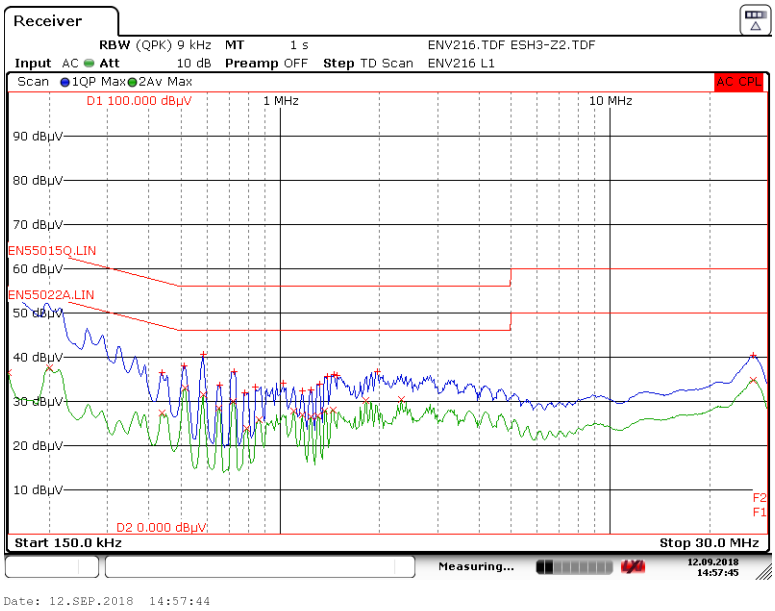

Figure 130 – Earth Ground EMI, 9 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).

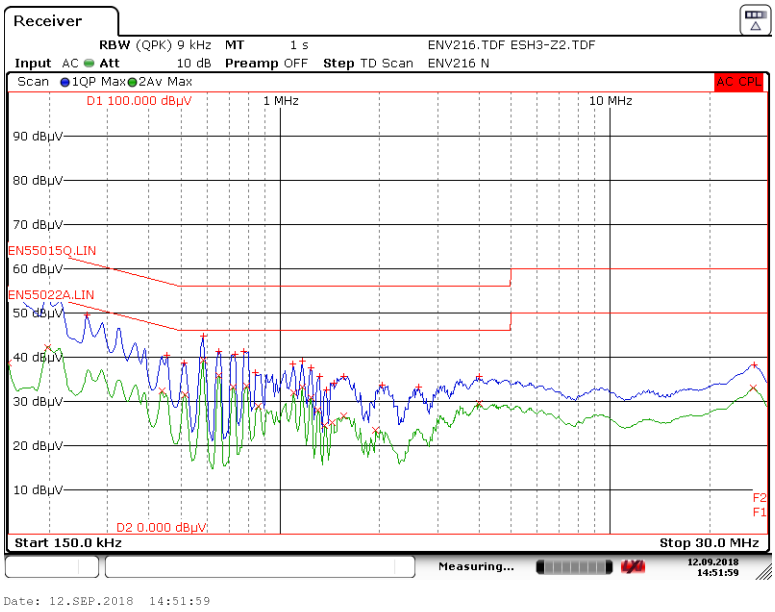

Figure 131 – Earth Ground EMI, 9 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).

16.3.3 Output: 11 V / 2.45 A

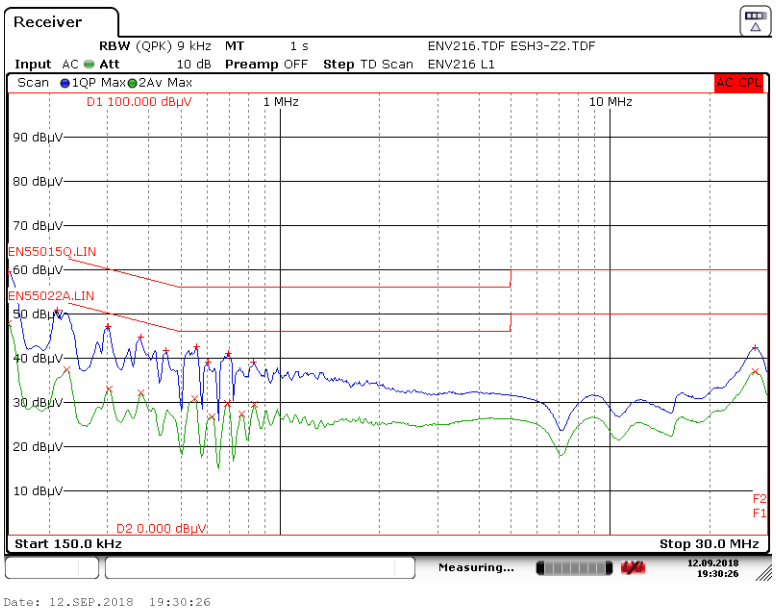

Figure 132 – Earth Ground EMI, 11 V / 2.45 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

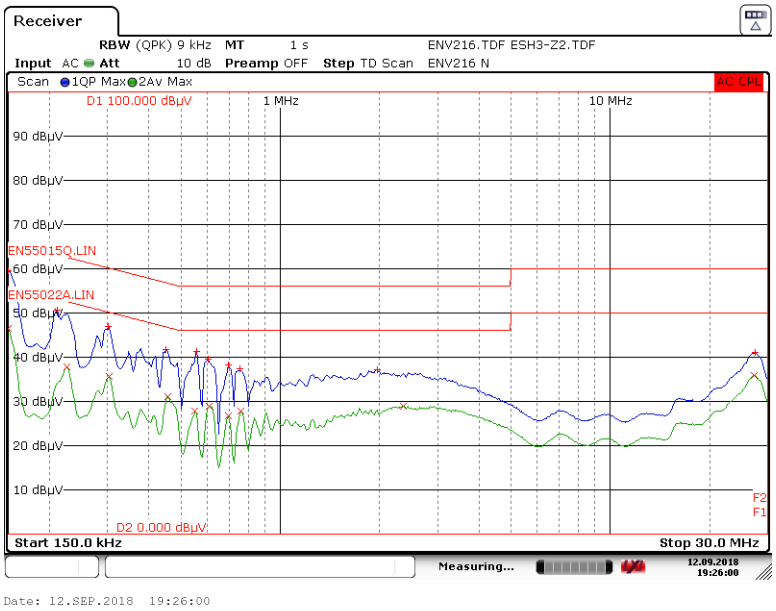

Figure 133 – Earth Ground EMI, 11 V / 2.45 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

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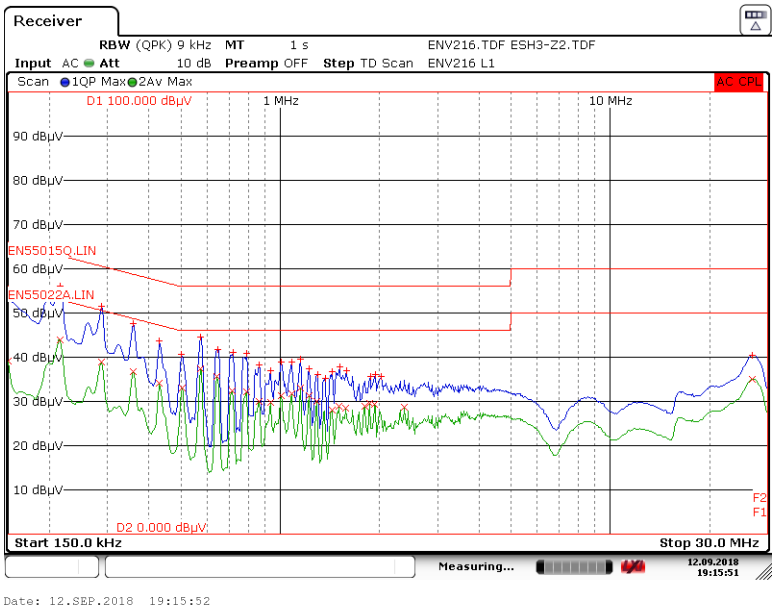

Figure 134 – Earth Ground EMI, 11 V / 2.45 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).

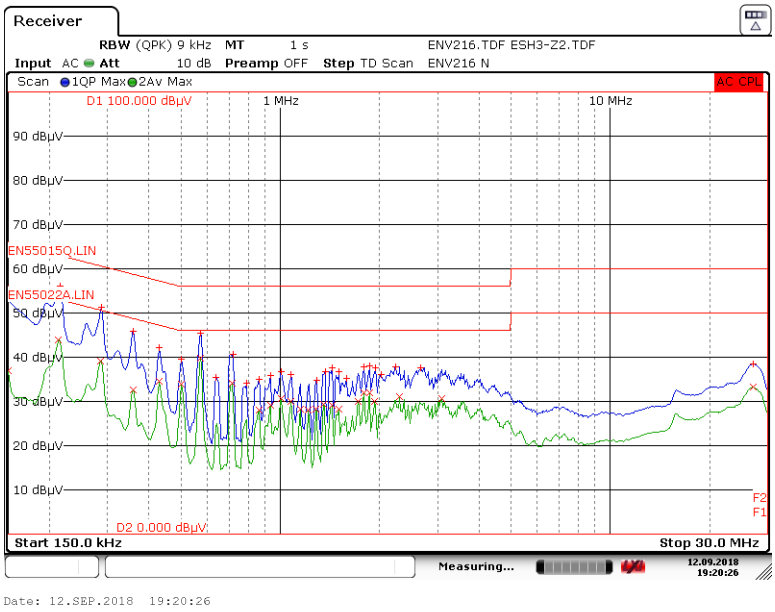

Figure 135 – Earth Ground EMI, 11 V / 2.45 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).

17 Line Surge

The unit was subjected to ±2000 V common mode surge and ±1000 V differential surge with 10 strikes for each condition. A test failure was defined as a temporary interruption of output, even if it is self-recoverable or needs operator intervention to recover, or a complete loss of function which is not recoverable.

17.1 Differential Surge

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result 5 V / 3 A (Pass/Fail)	Test Result 9 V / 3 A (Pass/Fail)
+1000	230	L1 to L2	0	Pass	Pass
-1000	230	L1 to L2	0	Pass	Pass
+1000	230	L1 to L2	90	Pass	Pass
-1000	230	L1 to L2	90	Pass	Pass
+1000	230	L1 to L2	180	Pass	Pass
-1000	230	L1 to L2	180	Pass	Pass
+1000	230	L1 to L2	270	Pass	Pass
-1000	230	L1 to L2	270	Pass	Pass

17.2 Common Mode Surge

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result 5 V / 3 A (Pass/Fail)	Test Result 9 V / 3 A (Pass/Fail)
+2000	230	L1 to PE	0	Pass	Pass
-2000	230	L1 to PE	0	Pass	Pass
+2000	230	L1 to PE	90	Pass	Pass
-2000	230	L1 to PE	90	Pass	Pass
+2000	230	L1 to PE	180	Pass	Pass
-2000	230	L1 to PE	180	Pass	Pass
+2000	230	L1 to PE	270	Pass	Pass
-2000	230	L1 to PE	270	Pass	Pass

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result 5 V / 3 A (Pass/Fail)	Test Result 9 V / 3 A (Pass/Fail)
+2000	230	L2 to PE	0	Pass	Pass
-2000	230	L2 to PE	0	Pass	Pass
+2000	230	L2 to PE	90	Pass	Pass
-2000	230	L2 to PE	90	Pass	Pass
+2000	230	L2 to PE	180	Pass	Pass
-2000	230	L2 to PE	180	Pass	Pass
+2000	230	L2 to PE	270	Pass	Pass
-2000	230	L2 to PE	270	Pass	Pass

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18 Revision History

Date	Author	Revision	Description & Changes	Reviewed
27-Sep-18	DB / AP	1.0	Initial Release.	Apps & Mktg
28-Jun-19	AP	1.1	Updated Schematic and BOM	Apps & Mktg

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