Design Example Report

Title	***140 W USB PD 3.1 / EPR Power Supply with 5 V / 9 V / 15 V / 20 V / 28 V Output Using InnoSwitch™4-CZ PowiGaN™ INN4077C-H182, ClampZero™ CPZ1076M and HiperPFS™-5 PFS5177F***
Specification	90 VAC – 265 VAC Input; 5 V / 3 A; 9 V / 3 A; 15 V / 3 A; 20 V / 5 A; 28 V / 5 A Outputs
Application	USB PD Power Adapter
Author	Applications Engineering Department
Document Number	DER-966
Date	July 13, 2022
Revision	1.0

Summary and Features

- InnoSwitch4-CZ - active clamp flyback switcher IC with integrated high-voltage PowiGaN, synchronous rectification and FluxLink™ feedback
- Zero voltage switching in both CCM and DCM operating conditions
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
- Meets DOE6 and CoC v5 2016 efficiency requirement
- Output overvoltage and overcurrent protection
- Integrated thermal protection
- 140 W USB PD 3.1 design supports EPR 28 V / 5 A output
- >94.5 % full load efficiency at 230 VAC
- <75 mW no-load input power
- Ultra-compact 88 x 65 x 20 mm PCB design includes AC prong space

Power Integrations

5245 Hellyer Avenue, San Jose, CA 95138 USA.

Tel: +1 408 414 9200 Fax: +1 408 414 9201

www.power.com

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a high power density 140 W USB PD 3.1 external power supply that can provide 5 V / 3 A, 9 V / 3 A, 15 V / 3 A, 20 V / 5 A and 28 V / 5 A outputs. This was made possible using three innovative PowiGaN-based devices InnoSwitch4-CZ INN4077C, ClampZero CPZ1076M, and HiperPFS-5 PFS5177F. The PSU contains a highly-efficient boost Power Factor Corrector (PFC) and flyback DC-DC converter.

The report contains the power supply specification, schematic diagram, printed circuit board layout, bill of materials, magnetics and adapter case specifications, and performance data.

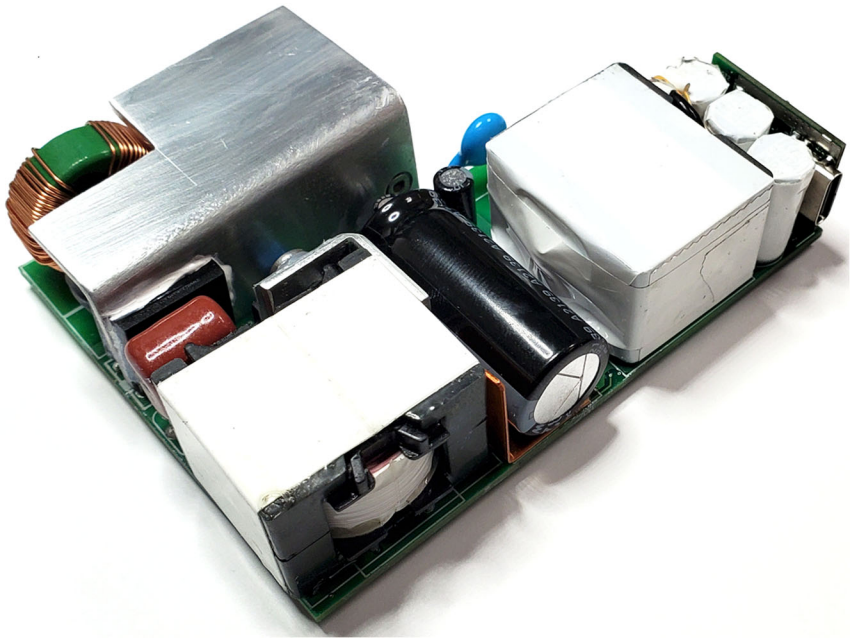


Figure 1 – DER-966 Board Picture

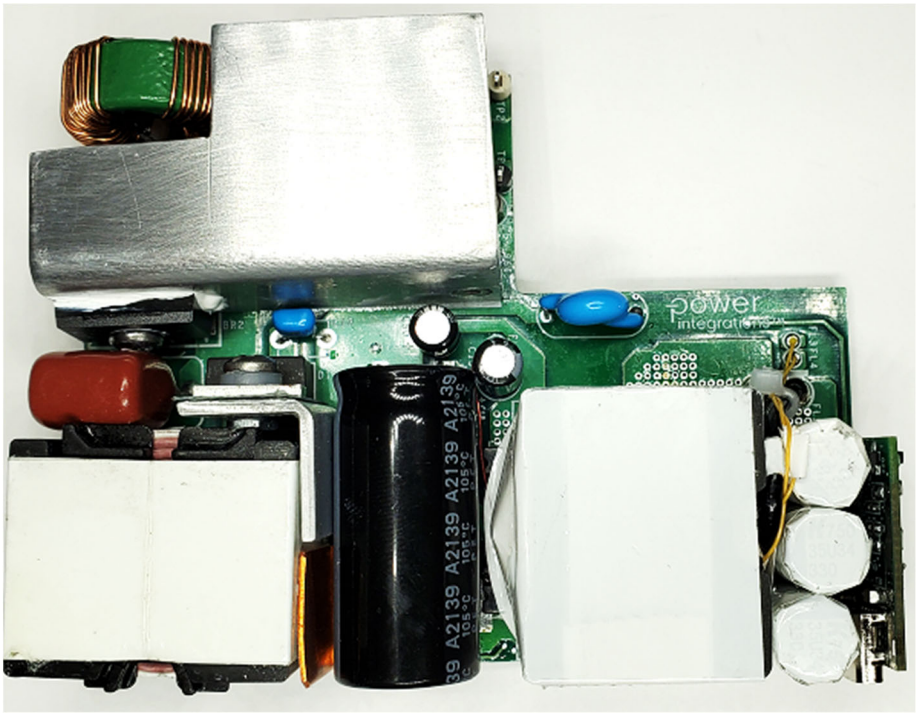


Figure 2 – Populated Circuit Board Photograph – Top Main.

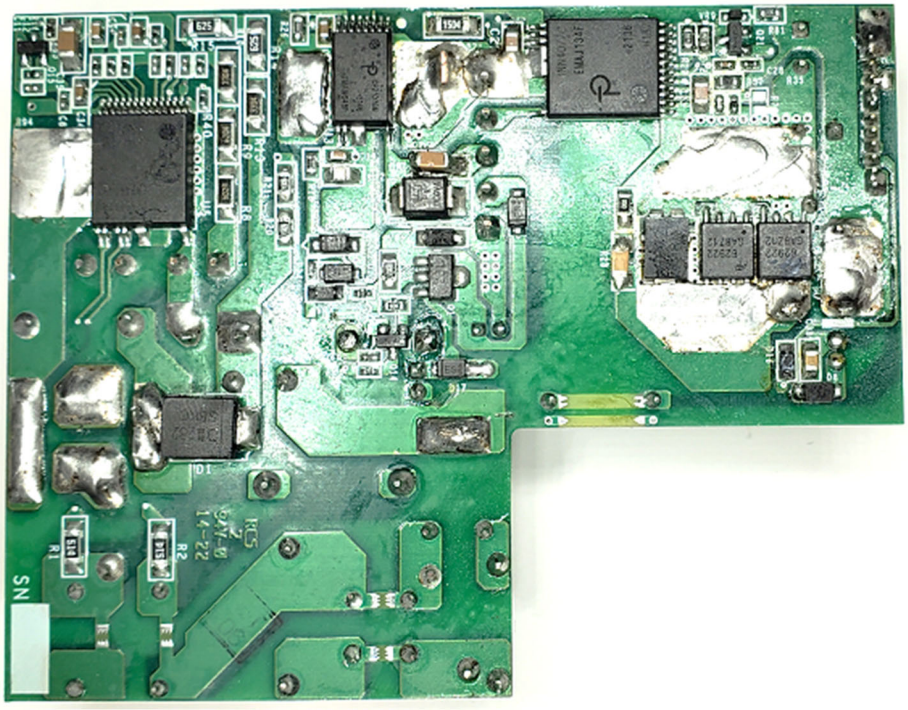


Figure 3 – Populated Circuit Board Photograph – Bottom Main.

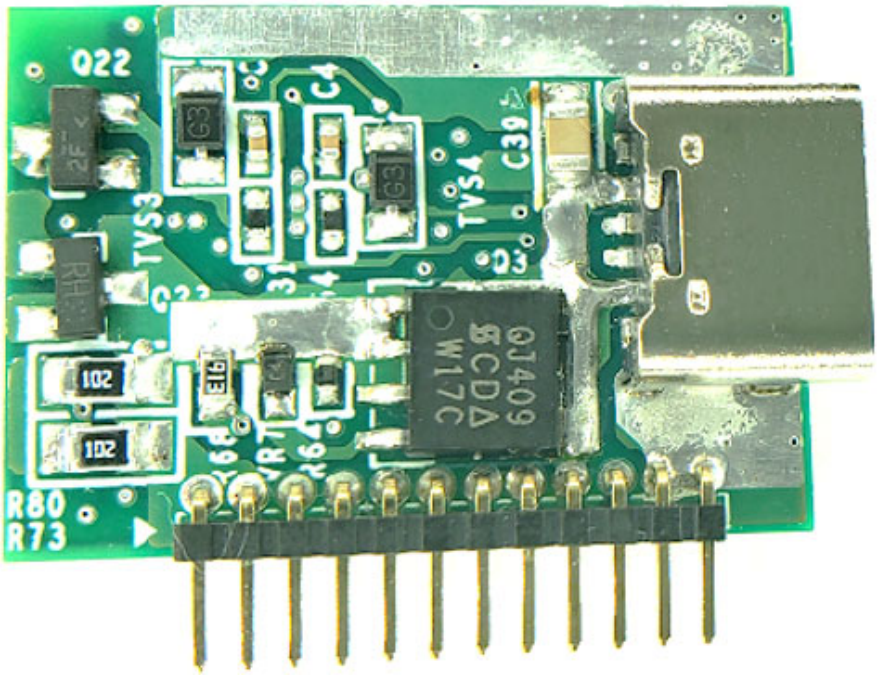


Figure 4 – Populated Circuit Board Photograph – Daughter Board Top.

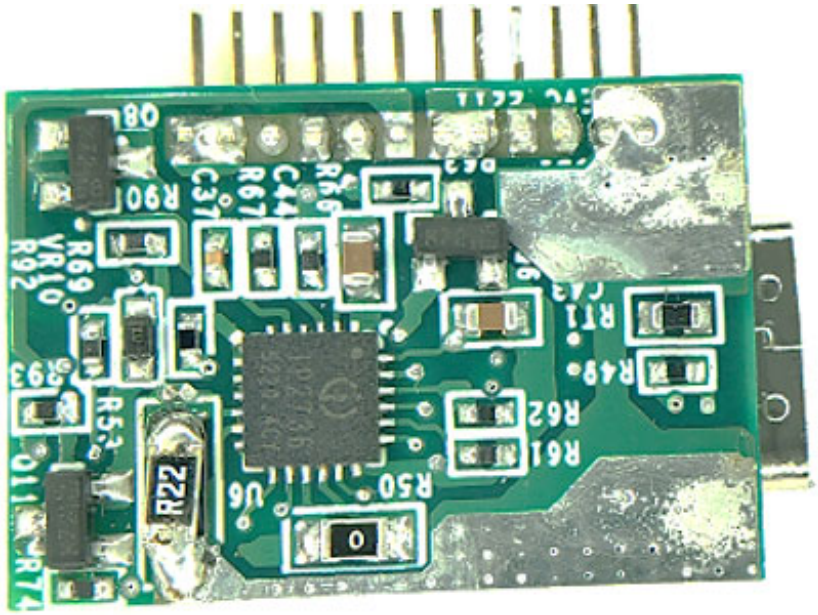


Figure 5 – Populated Circuit Board Photograph – Daughter Board Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
No-load Input Power				75	mW	Measured at 230 VAC.
5 V Setting						
Output Voltage	$V_{OUT(5\ V)}$		5.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(5\ V)}$			150	mV	Measured at End of Cable. (20 MHz Bandwidth).
Output Current	$I_{OUT(5\ V)}$			3.0	A	±3%
Full Load Efficiency	$\eta_{(5\ V)}$		91.3		%	Measured at 230 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(5\ V)}$			15	W	
9 V Setting						
Output Voltage	$V_{OUT(9\ V)}$		9.0		V	±2%
Output Voltage Ripple	$V_{RIPPLE(9\ V)}$			150	mV	Measured at End of Cable. (20 MHz Bandwidth).
Output Current	$I_{OUT(9\ V)}$			3.0	A	±3%
Full Load Efficiency	$\eta_{(9\ V)}$		93.3		%	Measured at 230 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(9\ V)}$			27	W	
15 V Setting						
Output Voltage	$V_{OUT(15\ V)}$		15.0		V	±2%
Output Voltage Ripple	$V_{RIPPLE(15\ V)}$			150	mV	Measured at End of Cable. (20 MHz Bandwidth).
Output Current	$I_{OUT(15\ V)}$			3.0	A	±3%
Full Load Efficiency	$\eta_{(15\ V)}$		94.2		%	Measured at 230 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(15\ V)}$			45	W	
20 V Setting						
Output Voltage	$V_{OUT(20\ V)}$		20.0		V	±2%
Output Voltage Ripple	$V_{RIPPLE(20\ V)}$			150	mV	Measured at End of Cable. (20 MHz Bandwidth).
Output Current	$I_{OUT(20\ V)}$			5	A	±3%
Full Load Efficiency	$\eta_{(20\ V)}$		94.5		%	Measured at 230 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(20\ V)}$			100	W	
28 V Setting						
Output Voltage	$V_{OUT(28\ V)}$		28.0		V	±2%
Output Voltage Ripple	$V_{RIPPLE(28\ V)}$			150	mV	Measured at End of Cable. (20 MHz Bandwidth).
Output Current	$I_{OUT(28\ V)}$			5	A	±3%
Full Load Efficiency	$\eta_{(28\ V)}$		95.0		%	Measured at 230 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(28\ V)}$			140	W	
Conducted EMI		Meets CISPR22B / EN55022B				
Ambient Temperature	T_{AMB}	0		40	ºC	Free Convection, Sea Level.

3 Schematic

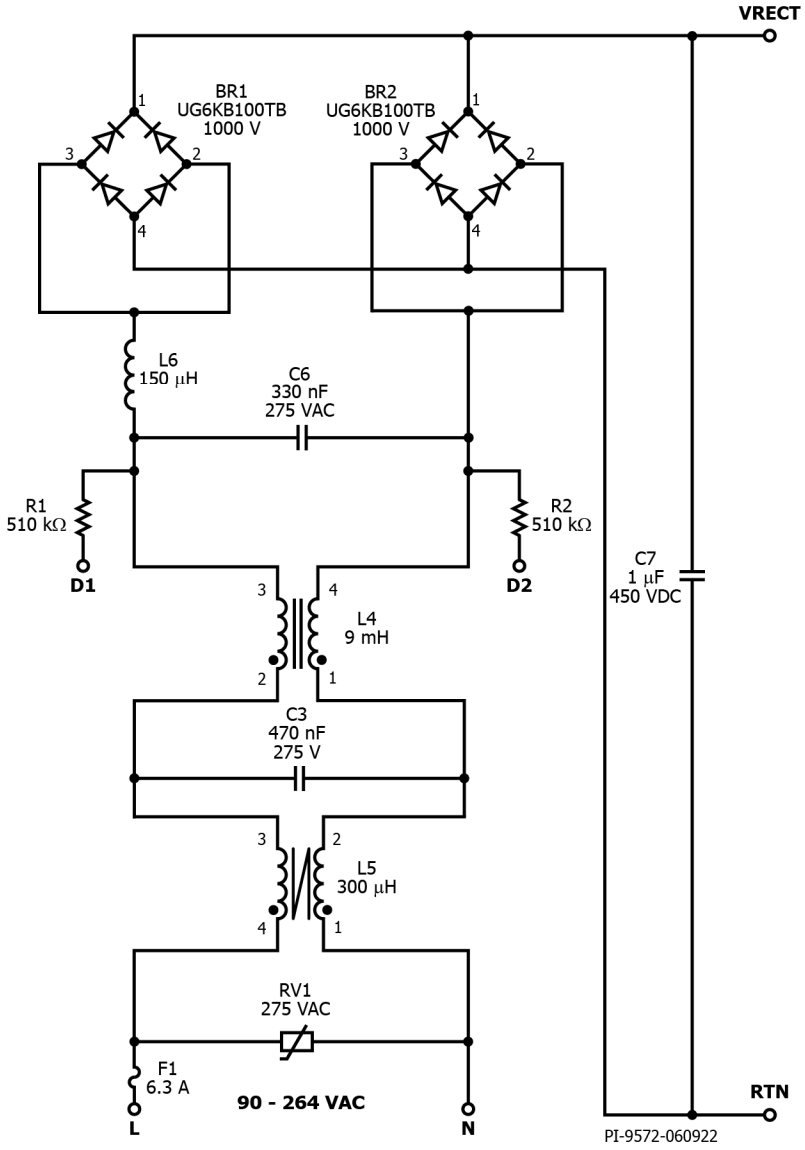


Figure 6 – Schematic, Input Section

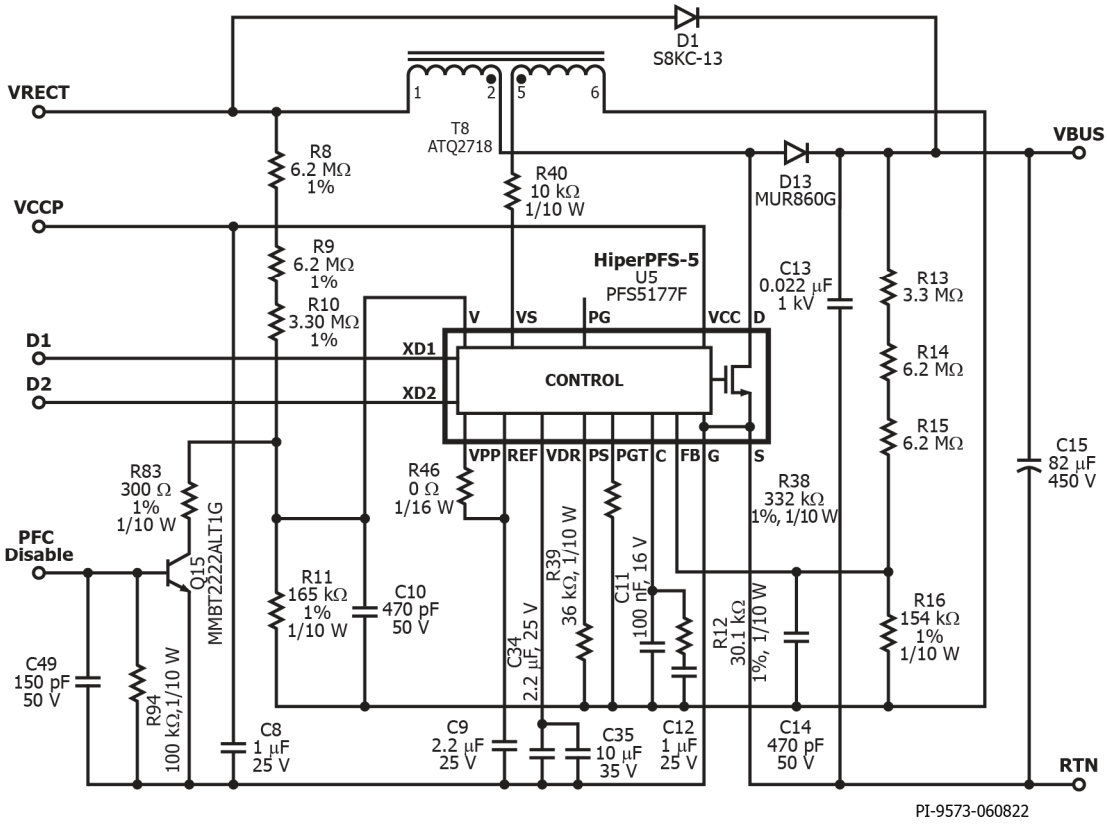


Figure 7 – Schematic, PFC Section.

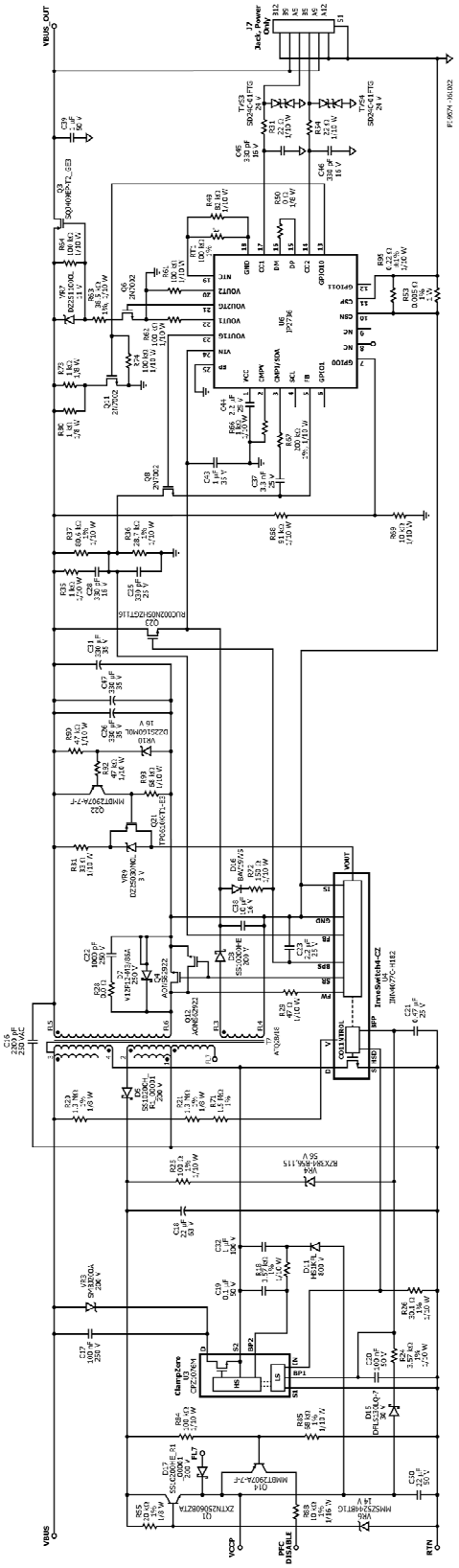


Figure 8 – Schematic, Power Section.

4 Circuit Description

The input stage is a boost PFC powered by HiperPFS-5 and the second stage is a DC-DC flyback converter using InnoSwitch4-CZ paired with ClampZero active clamp IC.

4.1 *Input Rectifier and EMI Filter*

Input fuse F1 provides safety protection from catastrophic failure, varistor RV1 protects against line transients, bridge rectifiers BR1 and BR2 rectify the AC line voltage and provide a full wave rectified DC across the filter capacitor C7. EMI suppression components are comprised of common-mode chokes L5 and L4, X capacitors C3 and C6, and differential-mode choke L6. Resistors R1 and R2 are required to discharge the energy stored in the X capacitors once the AC input lines are disconnected.

4.2 *HiperFPS-5 PFC Controller*

The HiperPFS-5 family incorporates a novel quasi-resonant DCM PFC controller with 750 V PowiGaN, X capacitor discharge, and high-voltage self-start-up in a low-profile power package. HiperPFS-5 devices eliminate need for external current sense resistors and their associated power loss and use an innovate control technique that adjusts the switching frequency over output load, input line voltage, and input line cycle. Low switching and conduction losses from PowiGAN, and other efficiencies of high integration allows for designs of up to 220 W without a heat sink.

The PFC power stage is comprised of the boost inductor T8, boost diode D13, bypass diode D1, bulk capacitor C15, and HiperPFS-5 U5. A small decoupling capacitor C13 is added for EMI.

The VALLEY SENSING (VS) pin is connected to the auxiliary winding on inductor T8 through an external resistor R40. The resistor is used to limit the current through VS pin and for fine adjustment of timing for valley switching.

The VOLTAGE MONITOR (V) pin is tied to the rectified high-voltage DC rail through an approximately 100:1 high impedance resistor dividers R8, R9, R10 and R11. A small ceramic capacitor C10 form an 80 μs time constant to bypass any switching noise present on the rectified DC bus.

The POWER SELECTION (PS) resistor R39 programs the power limit of the device to 80% of its nominal output power. This scheme maximizes the efficiency by selecting PFS5177F that has lower $R_{DS(ON)}$ while keeping the RMS current low.

The REF pin is connected to a bypass capacitor C9 while the VPP pin must be connected to REF pin via R46. Capacitor C12 and series R-C circuit R12/C12 connected to COMPENSATION (C) pin for loop pole / zero compensation.

The FEEDBACK (FB) pin is connected to the main voltage regulation feedback resistor divider network of upper FB resistors R13, R14, and R15 and bottom FB resistor R16. The divider ratio was selected to ensure that nominal PFC output voltage is 400 V. A small ceramic filter capacitor C14 is added to form an 80 μs time constant with the bottom FB resistor.

The BIAS POWER (VCC) pin is used to power the IC and comes from the output of the linear regulator used to supply InnoSwitch-CZ and ClampZero as well. Capacitor C8 is the bypass capacitor of VCC.

4.2.1 PFC Disable Circuit

The PFC disable circuit is implemented to optimize the system efficiency when the PSU is operating at lower output power (input power <75 W). This is when output voltage is at 5 V, 9 V and 15 V. The circuit senses the output voltage through the bias winding and turn off the PFC when output voltage is <16 V. It works by pulling the V pin low via resistor R83 and transistor Q15. The voltage divider resistors R84 and R85 set the PFC disable voltage threshold at 15 V. The PFC disable threshold can be easily modified by adjusting these voltage divider resistors. When the output voltage is 15 V or lower, Q14 and Q15 turns on to turn off the PFC by pulling down the V pin of U5. Capacitor C49 and resistor R94 are added to filter the noise that could turn on Q15. Resistor R88 limits the base current of Q15 to reduced power dissipation.

4.3 *InnoSwitch4-CZ IC Primary*

Innoswitch4-CZ IC (U4) controls the DCDC stage flyback converter. One end of the transformer T7 primary is connected to the PFC output DC bus; the other is connected to the drain terminal of the switch inside the InnoSwitch4-CZ IC (U4).

The UNDER/OVER INPUT VOLTAGE (V) pin of the InnoSwitch4-CZ IC provide input under/over voltage sensing and is connected to the DC bus via resistor network R20, R21, and R71.

The value of PRIMARY BYPASS (BPP) capacitor C21 sets the current limit of the InnoSwitch4-CZ to STANDARD mode. The BYPASS pin of InnoSwitch4-CZ also supplies the ClampZero IC (U3) BP1 pin during start-up.

The primary clamp capacitor C17 limits the peak drain voltage of U4 at the instant of turn-off of the switch inside U4. The energy stored in the leakage inductance of transformer T6 will be transferred to capacitor C17. Part of the magnetizing energy will also get transferred to C17 depending on the capacitance value used. VR3 is used to protect the InnoSwitch4-CZ from excessive drain voltages if there is any malfunction of the power supply.

When the FluxLink signal is received from the secondary-side, the InnoSwitch4-CZ generates an HSD signal to turn on the ClampZero device. When the ClampZero IC (U3) turns on, to achieve soft switching of the InnoSwitch4-CZ primary switch, clamp capacitor

C17 starts to charge the leakage inductance of the transformer in the case of CCM operation and both the leakage and the magnetizing inductance of the transformer in the case of DCM operation. A small delay is provided from the instant the high-side switch turns off to achieve zero voltage switching on the primary switch. This delay is programmable by different resistor values of R26.

Capacitor C20 is used to provide local decoupling at the BP1 pin of IC U3. Capacitor C19 provides the decoupling for BP2 pin. Diode D11 and capacitor C32 form a bootstrap circuit to provide the bias for the high-side BP2 pin. Resistor R18 limits the current flowing into the BP2 pin.

The InnoSwitch4-CZ IC is self-starting, using an internal high-voltage current source to charge C21 when AC is first applied. During normal operation, the primary-side block of the IC is powered by the primary auxiliary bias supply. There are 2 auxiliary bias supply that help supply the primary depends on the output voltage. When output voltage is 15 V or lower, the primary is supplied by the bias coming from D5 and C18. The voltage across C18 has a huge fluctuation base from the output voltage that is why a linear regulator (Q1, VR6 and R55) is added to provide a constant bias supply across the output range. When output voltage is 20 V and 28 V, the primary bias is supplied by the Auxiliary forward bias supply circuit. This auxiliary supply is a forward type converter with respect to the bulk voltage (395 VDC). During 28 V – 20 V output, this forward auxiliary supplies a constant 15V voltage directly through a 1 turn winding from FL7 to Pin 1. The voltage is rectified by diode D17 and filtered by C50. Also, during 28 V and 20 V output, the primary linear regulator Q1 is off due to its emitter voltage is higher than the base voltage (14 V). This significantly eliminate the power dissipation across Q1 at high output voltage operation. When the output voltage is 15 V, 9 V and 5 V, the bulk voltage will drop to $V_{IN}*\sqrt{2}$ since the PFC is purposely disabled by the PFC disable circuit. Consequently, the voltage across C50 will become lower than 14 V therefore it will turn on the linear regulator Q1 supplying the primary side at much lower power dissipation.

BPP resistor R24 limits the current supplied to BPP. Diode D15 blocks BPP from sourcing current to the PFC disable circuit during start-up. Without D15, U4 might not be able to start-up properly.

Output regulation is achieved using modulation control, where the frequency and I_{LIM} of switching cycles are adjusted based on the output load. At high load, most switching cycles are enabled for a high value of I_{LIM} in the selected I_{LIM} range, and at light load or no-load, most cycles are disabled, and the ones enabled have a low value of I_{LIM} in the selected I_{LIM} range. Once a cycle is enabled, the switch remains on until the primary current ramps to the device current limit for the specific operating state.

The latch-off/auto-restart primary-side overvoltage protection is obtained using Zener diode VR4 with current limiting resistor R25. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at the output of

the converter, the auxiliary winding voltage increases and causes breakdown of VR4, which then causes a current to flow into the BPP pin of InnoSwitch4-CZ IC U4. If the current flowing into the BPP pin increases above the I_{SD} threshold, the U4 controller latches off to prevent any further increase in output voltage.

Y capacitor C16 is connected between primary DC ground and secondary VBUS rail is used to reduce EMI.

4.4 *InnoSwitch4-CZ IC Secondary*

The secondary-side of the InnoSwitch4-CZ IC provides output voltage, output current sensing, and drive to a MOSFET providing synchronous rectification. The secondary of the transformer is rectified by SR FETs Q4, Q12, and diode D7, and filtered by capacitors C26, C31 and C47. Capacitor C39 is used to reduce the high-frequency output voltage ripple. Resistor R28 and capacitor C22 reduces the peak voltage of SR FETs.

The gates of Q4/Q12 are turned on by the secondary-side controller of IC U4, based on the winding voltage sensed via resistor R29 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the SR MOSFET is turned off just prior to the secondary side commanding a new switching cycle from the primary. In discontinuous mode of operation, the power MOSFET is turned off, when the voltage drop across the MOSFET falls below a threshold of approximately $V_{SR(TH)}$ mV.

The secondary-side of the IC U4 is self-powered from either the secondary winding forward voltage or the output voltage. However, to improve the system efficiency and reduce the secondary-side internal consumption, a bias winding circuit was used. It is designed to supply current to the IC when the output voltage is set to 28 V. At lower output voltage setting, the supply comes from the OUTPUT VOLTAGE (VOUT) pin. Bias winding voltage is rectified by diode D8 and filtered by capacitor C38. Resistor R72 limits the current flowing to the BPS pin of U4. Diode D16 blocks BPS from charging C38 that might affect start-up operation. Capacitor C23 connected to the BPS pin of IC U4 provides decoupling for the internal circuitry.

The VOUT pin is connected to the output voltage via resistor R81 and Zener diode VR9. It provides current to the IC when the output is lower than 28 V. Zener diode VR9 has a bypass circuit that activates whenever the output is below 16 V. This is to ensure that the additional drop on the Zener will not hinder the ability of the output rail to supply current the IC. This is critical especially when the output is set to 5 V. The bypass circuit is comprised of Q21, R86, R93, Q22, R92, R90 and VR10.

The device is configured to operate in constant voltage mode. In this mode, output voltage regulation is achieved through sensing the output voltage via divider resistors R36 and R37. The voltage across R36 is fed into the FB pin with an internal reference voltage

threshold of 1.265 V. The output voltage is regulated to achieve a voltage of 1.265 V on the FB pin. Capacitor C25 provides noise filtering of the signal at the FB pin. Resistor R35 and capacitor C28 connected across R37 help reduce output voltage ripple.

Current limiting is implemented on the external PD controller.

4.5 *USB Type-C and PD Interface*

In this design, Injoinic IP2736 (U6) is the USB Type-C and USB PD3.1/EPR 28 V controller.

At 28 V output, the supply for U6 comes from the secondary bias winding. At lower output voltage, the supply comes from a linear regulator circuit formed by connecting the Drain of MOSFET Q23 to the flyback output rail, the gate of Q23 to BPS pin, and the SOURCE of Q23 to VIN pin of IP2736. This configuration minimizes the power dissipation of Q23 by disabling it when the output is at 28 V.

IP2736 (U6) monitors and sets the feedback divider ratio such that InnoSwitch4-CZ IC U4 regulates the output voltage at required level. IP2736 (U6) changes the output voltage divider ratio to required level when there is a request through CC1 and CC2 lines. The default output voltage is maintained at 5 V.

USB PD protocol is communicated over either CC1 or CC2 line depending on the orientation in which Type-C plug is connected.

P-MOSFET Q3 makes the USB Type-C receptacle cold socket when no device is attached to the charger as per the USB Type-C specification. It is driven by MOSFET Q6, which is controlled by VOUT2G pin of U6. Zener diode VR7 clamps the voltage across Q3 Source-Gate to 11 V. Resistor R64 is the pull-down resistor for Q3. Resistor R63 limits the current of VR7. Resistor R53 is used to sense the output current for the microcontroller.

Capacitor C43 is used as decoupling capacitor on VIN pin of U6 and capacitor C44 is used as decoupling capacitor on VCC pin of U6. Resistor R31, R54, C45, C46, TVS3 and TVS4 are used to protect the CC1 and CC2 lines from ESD surge events.

Thermistor RT1 is used to sense USB Type-C connector temperature. Resistor R49 fine tunes the temperature sensing. Resistor R66 and RC network of R67 and C37 provide compensation for U6. Divider resistors R28 and R69 provide rail voltage information to U6.

5 PCB Layout

5.1 *Main Board*

Material: FR4, 2 oz copper, 0.062 inches thick

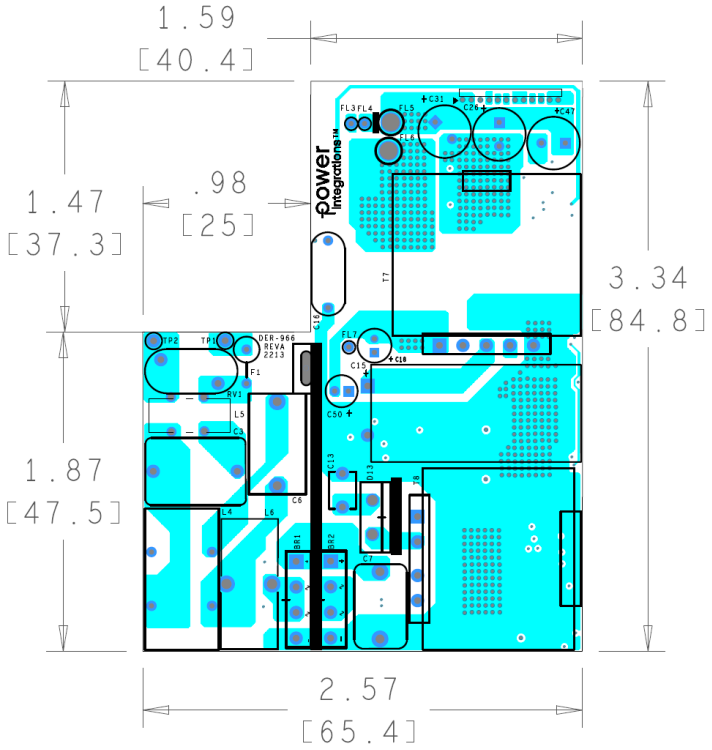


Figure 9 – Main Board Printed Circuit Layout, Top

Figure 10 – Main Board Printed Circuit Layout, Inner 1.

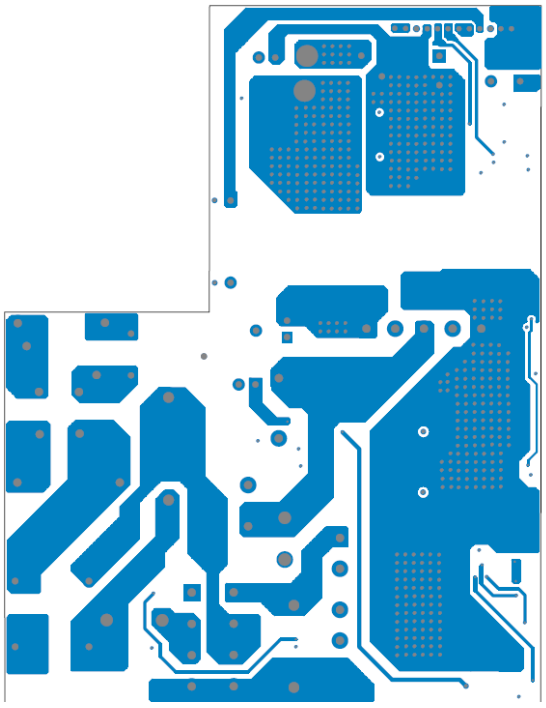


Figure 11 – Main Board Printed Circuit Layout, Inner 2

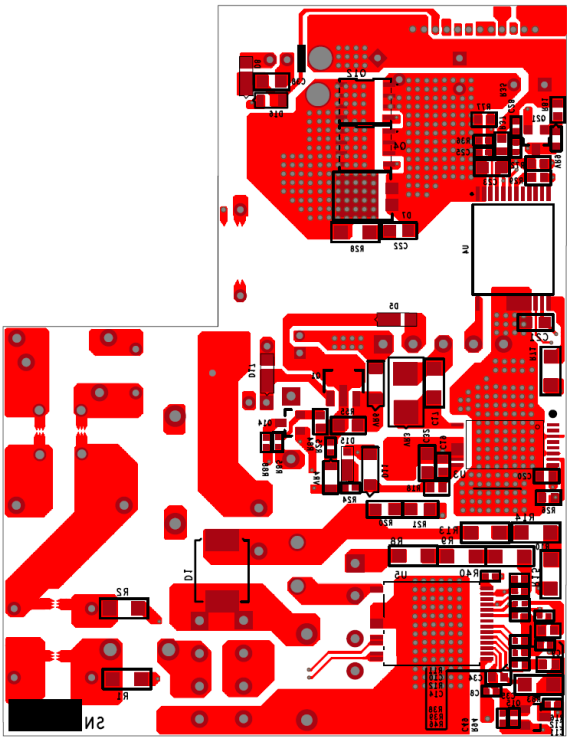


Figure 12 – Main Board Printed Circuit Layout, Bottom.

Note: For ESD consideration, please refer to ESD test on section 21.

5.2 *Daughter Board*

Material: FR4, 2 oz copper, 0.04 inches thick

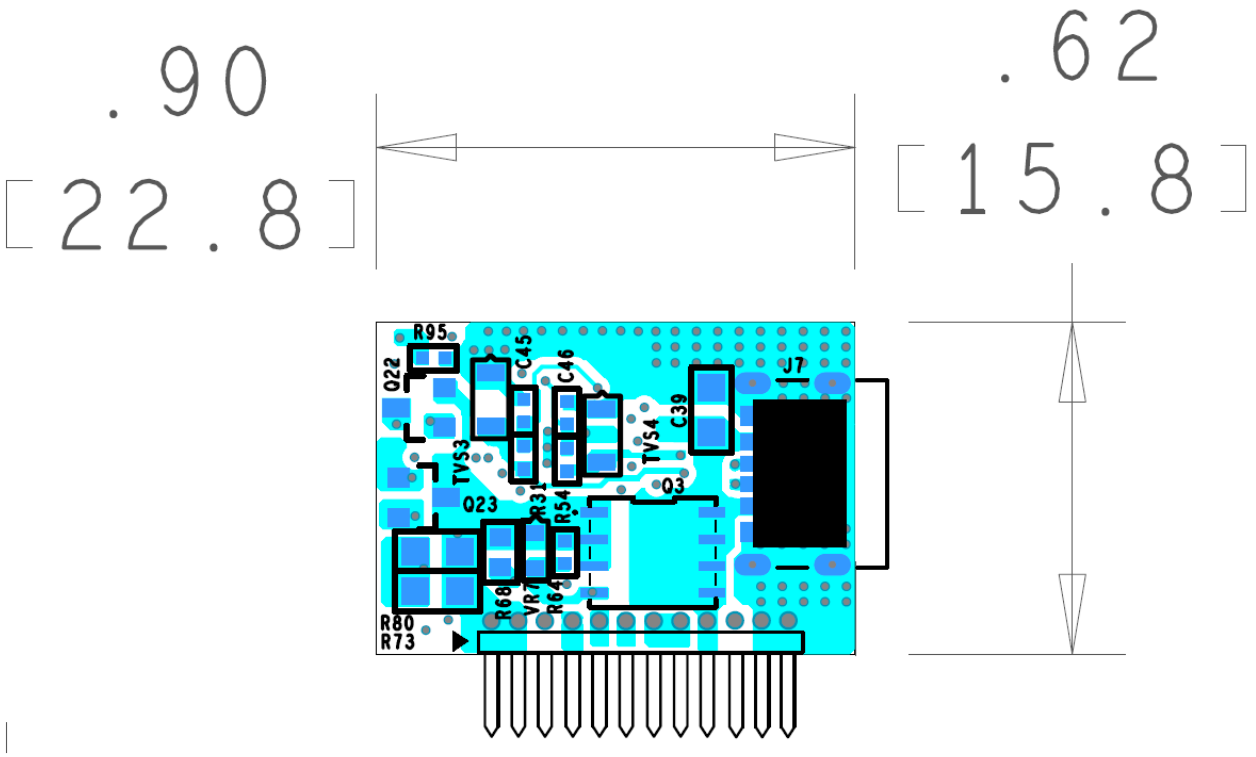


Figure 13 – Daughter Board Printed Circuit Layout, Top.

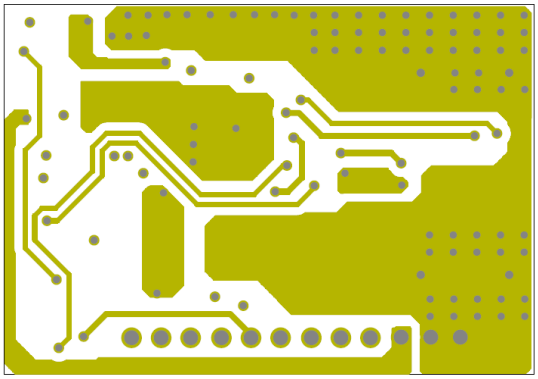


Figure 14 – Daughter Board Printed Circuit Layout, Inner 1.

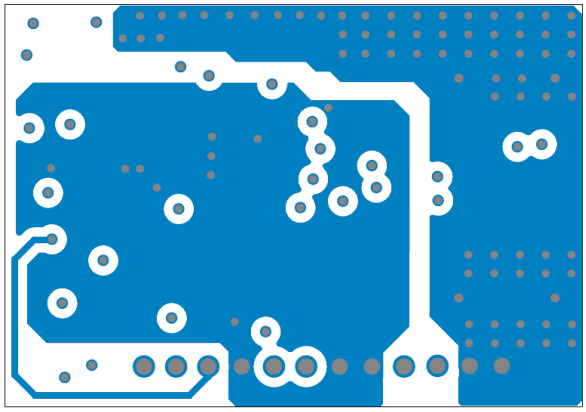


Figure 15 – Daughter Board Printed Circuit Layout, Inner 2.

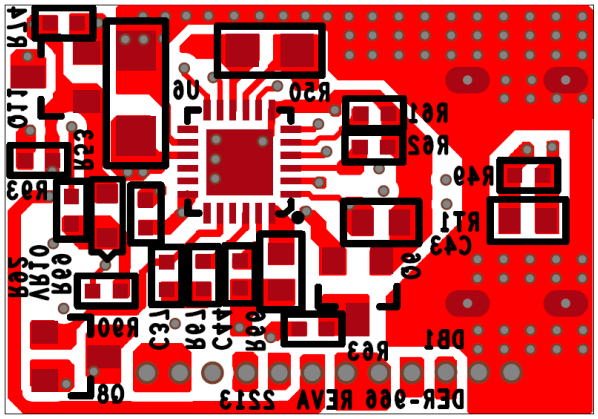


Figure 16 – Daughter Board Printed Circuit Layout, Bottom.

6 Bill of Materials

6.1 *Electrical Parts*

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	2	BR1 BR2	Bridge Rectifier, 6 A, Single Phase Standard, 1 kV Through Hole, 4-ESIP, D3K	UG6KB100TB	SMC Diode
2	1	C3	FILM, 0.47 µF, 10%, 275 VAC, X2, RAD	890324024005	Wurth
3	1	C6	330 nF, ±10%, 275 VAC, Polypropylene Film, X2, 15.00 mm x 8.50 mm	890324024003CS	Wurth
4	1	C7	FILM, 1.0 µF, 10%, 450 VDC, RADIAL	ECW-FD2W105Q1	Panasonic
5	1	C8	1 µF 25 V, Ceramic, X5R, 0402	TMK105BJ105MV-F	Taiyo Yuden
6	2	C9 C34	2.2 µF, ±10%, 25 V, Ceramic, X5R, 0603	GRM188R61E225KA12D	Murata
7	2	C10 C14	470 pF, ±5%, 50 V, C0G, NP0, -55°C ~ 125°C, Low ESL, 0402	C0402C471J5GACTU	Kemet
8	1	C11	100 nF 16 V, Ceramic, X7R, 0402	L05B104KO5NNNC	Samsung
9	1	C12	1 µF, ±10%, 25 V, Ceramic, X7R, 0603	CGA3E1X7R1E105K080AE	TDK
10	1	C13	0.022 µF, ±10%, 1 kV, X7R, Radial, -55 °C ~ 125 °C, 0.217" L x 0.157" W (5.50 mm x 4.00 mm)	RDER73A223K3M1H03A	Murata
11	1	C15	82 µF, 450 V, Electrolytic, General Purpose, (14.5 x 32)	450HXW82MEFR14.5X30	Rubycon
12	1	C16	2200 pF, ±20%, 300 VAC, Ceramic, Safety X1, Y1	DE1E3RA222MN4AP01F	Murata
13	1	C17	100 nF, 250 V, Ceramic, X7R, 1206	CGA5L3X7R2E104M160AA	TDK
14	1	C18	22 µF, ±20%, 63 V, Electrolytic, (5 x 12.5), LS 2 mm	63YXJ22M5X11	Rubycon
15	1	C19	0.1 µF ±10% 50 V Ceramic X7R 0603	CGA3E2X7R1H104K080AA	TDK
16	1	C20	100 nF , ±10%, 50 V, Ceramic, X7R,0603	06035D104KAT2A	AVX
17	1	C21	0.47 µF, ±10%,25 V, Ceramic, X7R, 0805	CGA4J2X7R1E474K125AA	TDK
18	1	C22	1000 pF ±10% 250 V Ceramic X7R 0805	CS0805KRX7RYBB102	Yageo
19	1	C23	2.2 µF, 25 V, Ceramic, X7R, 0805	CL21B225KAFVPNE	Samsung
20	1	C25	330 pF, ±5%, 25 V, Ceramic, C0G, NP0, 0402	C0402C331J3GAC7867	Kemet
21	3	C26 C31 C47	330 µF, ±20%, 35 V, Aluminum - Polymer Radial, Can, 20 mΩ, 2000 Hrs @ 105 °C, (8 x 16)	A750KW337M1VAAE020	KEMET
22	3	C28 C45 C46	330 pF 16 V, Ceramic, X7R, 0402	C0402C331K4RACTU	Kemet
23	1	C32	1 µF, 100 V, Ceramic, X7S, 0805	C2012X7S2A105K125AB	TDK
24	1	C35	10 µF, ±10%, 35 V, Ceramic, X7R, 1206	C3216X7R1V106K160AC	TDK
25	1	C37	3.3 nF 25 V, Ceramic, X7R, 0402	C0402C332K3RACTU	Kemet
26	1	C38	10 µF, ±10%, 16 V, X7R, Ceramic, SMT, MLCC 0805	CL21B106KOQNNNE	Samsung
27	1	C39	1 µF, 50 V, Ceramic, X5R, 0805	08055D105KAT2A	AVX
28	1	C43	1 µF, ±10%,35 V, Ceramic, X7R, 0603	CGA3E1X7R1V105K080AE	TDK
29	1	C44	2.2 µF,±10%, 25 V, Ceramic, X7R, 0603,-55 to 125 °C	GRM188Z71E225KE43D	Murata
30	1	C49	150 pF, ±10%, 50 V, Ceramic X7R, 0402	C0402C151K5RAC7867	KEMET
31	1	C50	22 µF, 50 V, Electrolytic, Very Low ESR, 340 mΩ, (5 x 11)	EKZE500ELL220ME11D	Nippon Chemi-Con
32	1	D1	Diode GEN PURPOSE, 800 V, 8 A, SMC	S8KC-13	Diodes, Inc.
33	3	D5 D8 D17	Diode, Schottky, 200 V, 1 A, SMT SOD-123HE	SS10200HE_R1_00001	Panjit International
34	1	D7	Diode, Schottky, 120 V, 12 A, SMT, TO-277A (SMPC)	V12P12-M3/86A	Vishay Semi
35	1	D11	800 V, 1 A, High Efficiency Fast Recovery, SOD-123FL	HS1KFL	Taiwan Semi
36	1	D13	600 V, 8 A, Ultrafast Recovery, 35 ns, TO-220AC	MUR860G	ON Semi
37	1	D15	Diode, Schottky, 30 V, 1 A, SMT PowerDI™ 123	DFLS130LQ-7	Diodes, Inc.
38	1	D16	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
39	1	F1	6.3 A, 250 V, Slow, 3.6 mm x 10 mm, Axial	087706.3MXEP	Littelfuse
43	1	L4	9 mH, 2 A, Common Mode Choke	T18107V-902S P.I. Custom	Fontaine
44	1	L5	CMC, 300 µH @ 100 kHz, Toroidal, wound on 32-00315-00 toroidal core, using 10 turns #24 AWG wire per side	32-00429-00	Power Integrations
45	1	L6	150 µH, 20%, 2.5 A, Rdc=0.01, INDUCTOR, TOROID, HI AMP, VERT, 16.5 mm Diam, 8.5 mm Thick, 8.5 mm LS	7447018	Wurth
46	1	Q1	Bipolar (BJT) Transistor, NPN, 60 V, 5 A, 185MHz, 2.4 W, Surface Mount SOT-89-3,	ZXTN25060BZTA	Diodes, Inc.
47	1	Q3	MOSFET, P-Channel 40 V, 60 A (Tc), 68 W (Tc), Surface Mount PowerPAK® SO-8,	SQJ409EP-T2_GE3	Vishay
48	2	Q4 Q12	MOSFET, N-CH, 120 V, 85 A (at VGS=10 V), Trench Power	AONS62922	Alpha & Omega Semi
49	3	Q6 Q8 Q11	60 V, 115 mA, SOT23-3	2N7002-7-F	Diodes, Inc.

50	2	Q14 Q22	PNP, Small Signal BJT, 60 V, 0.3 A, SOT-23	MMBT2907A-7-F	Diodes, Inc.
51	1	Q15	NPN, Small Signal BJT, 40 V, 0.6 A, SOT-23	MMBT2222ALT1G	On Semi
52	1	Q21	60 V, 0.185 A, , P-Channel, SOT 23-3	TP0610K-T1-E3	Vishay
53	1	Q23	N-Channel, 50 V, 200 mA (Ta), 350 mW (Ta), SMT SST3, TO-236-3, SC-59, SOT-23-3	RUC002N05HZGT116	Rohm
54	2	R1 R2	RES, 510 kΩ, 5%, 1/4 W, Thick Film, 1206	RC1206JR-07510KL	Yageo
55	2	R8 R9	RES, 6.2 MΩ, 1%, 1/4 W, Thick Film, 1206	KTR18EZPF6204	Rohm
56	2	R10 R13	RES, 3.30 MΩ, 1%, 1/4 W, Thick Film, 1206	KTR18EZPF3304	Rohm
57	1	R11	RES, 165.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF1653X	Panasonic
58	1	R12	RES, 30.1 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF3012X	Panasonic
59	2	R14 R15	RES, 6.2 MΩ, 5%, 1/4 W, Thick Film, 1206	CRCW12066M20JNEA	Vishay
60	1	R16	RES, 154.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF1543X	Panasonic
61	1	R18	RES, 3.57 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF3571V	Panasonic
62	2	R20 R21	RES, 1.3 MΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1304V	Panasonic
63	1	R24	RES, 3.57 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF3571X	Panasonic
64	1	R25	RES, 100 Ω, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ101X	Panasonic
65	1	R26	RES, 30.1 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF3012V	Panasonic
66	1	R28	RES, 0 Ω, 5%, 1/4 W, Thick Film, 1206	RC1206JR-070RL	Panasonic
67	1	R29	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
68	2	R31 R54	RES, 22 Ω, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ220X	Panasonic
69	2	R35 R66	RES, 1 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ102X	Panasonic
70	1	R36	RES, 28.7 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF2872X	Panasonic
71	1	R37	RES, 80.6 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF8062V	Panasonic
72	1	R38	RES, 332.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF3323X	Panasonic
73	1	R39	RES, 36 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ363X	Panasonic
74	2	R40 R69	RES, 10 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ103X	Panasonic
75	1	R46	RES, 0 Ω, 1/16 W, Thick Film, 0402	CRCW04020000Z0ED	Vishay
76	1	R49	RES, 82 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ823X	Panasonic
77	1	R50	RES, 0 Ω, 5%, 1/8 W, Thick Film, 0805	RMCF0805ZT0R00	Stackpole
78	1	R53	RES, 5 mΩ, ±1%, 1 W, Chip Resistor 1206	CRF1206-FZ-R005ELF	Bourns
79	1	R55	RES, 20.0 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2002V	Panasonic
80	5	R61 R62 R64 R74 R94	RES, 100 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ104X	Panasonic
81	1	R63	RES, 36.5 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF3652X	Panasonic
82	1	R67	RES, 200.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF2003X	Panasonic
83	1	R68	RES, 91 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ913V	Panasonic
84	1	R71	RES, 1.50 MΩ, 1%, 1/4 W, Thick Film, 1206		Panasonic
85	1	R72	RES, 150 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ151V	Panasonic
86	2	R73 R80	RES, 1 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ102V	Panasonic
87	1	R81	RES, 33 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ330V	Panasonic
88	1	R83	RES, 300 Ω, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF3000X	Panasonic
89	1	R84	RES, 100 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ104V	Panasonic
90	1	R85	RES, 68.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF6802X	Panasonic
91	1	R88	RES, 10 kΩ, 5%, 1/16 W, Thick Film, 0402	RC0402JR-0710KL	Yageo
92	2	R90 R92	RES, 47 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ473X	Panasonic
93	1	R93	RES, 68 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ683X	Panasonic
94	1	R95	RES, 0.22 Ω, 1%, 1/10 W, Thick Film, 0402	SR731ETTPR220F	KOA
95	1	RT1	NTC Thermistor, 100 kΩ, 1%, 0603	NTCG164KF104FT1S	TDK
96	1	RV1	275Vac, 80J, 10 mm, RADIAL	ERZ-V10D431	Panasonic
97	1	T7	Bobbin, ATQ28/18, Vertical, 4 or 5 pins. Mates with core 99-00071-00.		
98	1	T8	Bobbin, ATQ27/18, Horizontal, 3 pins. (A fourth pin can be added)		
102	2	TVS3 TVS4	Bidirectional TVS Diode, Voltage - Reverse Standoff (Typ) 24 Vmax, 42 V Clamp	SD24C-01FTG	Littelfuse, Inc.
103	1	U3	Clampzero, MinSOP-16	CPZ1076M	Power Integrations
104	1	U4	InnoSwitch4-CZ, 115 W, insop-24D	INN4077C-H182	Power Integrations
105	1	U5	HiperPFS-5, 185 W, InSOP-T28F	PFS5177F	Power Integrations
106	1	U6	IC, Fast Charging Controller IC for USB Interfaces	IP2736	INJOINIC TECHNOLOGY
107	1	VR3	200 V, 224 V breakdown, 1.9 A peak Pulse, 600 W peak pulse, DO214AA (SMB)(SMBJ)	SMBJ200A	Littelfuse, Inc.
108	1	VR4	56 V, 2%, 300 mW, SOD323	BZX384-B56,115	NXP Semi
109	1	VR6	Diode ZENER 14 V 500 mW SOD123	MMSZ5244BT1G	ON Semi

110	1	VR7	Diode ZENER 11 V 300 mW SOD523	CMOZ11V TR PBFREE	Central Semi
111	1	VR9	Diode ZENER 3 V 150 mW SOD523	EDZVT2R3.0B	Rohm
112	1	VR10	Diode ZENER 16 V 150 mW SOD523	EDZVFHT2R16B	Rohm

6.2 *Mechanical Parts*

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	J7	USB-C (USB TYPE-C) Receptacle Connector 24 (6+18 Dummy) Position Surface Mount, Right Angle; Through Hole	UJC-HP-3-SMT-TR	CUI Devices
2	1	TE1	Terminal, Eyelet, Tin Plated Brass, Zierick PN 190		
2	1	TP1	Wire, #22 AWG, UL1213-22/19-0, Blk, PVC, Length: 58 mm, stripped and tinned 2.5 mm one end, and 6 mm at the other end.	66-00417-00	PI
3	1	TP2	Wire, #22 AWG, UL1213-22/19-0, White, PVC, Length: 58 mm, stripped and tinned 2.5 mm one end, and 6 mm at the other end.	66-00418-00	PI

7 Flyback Transformer (T7) Specification

7.1 *Electrical Diagram*

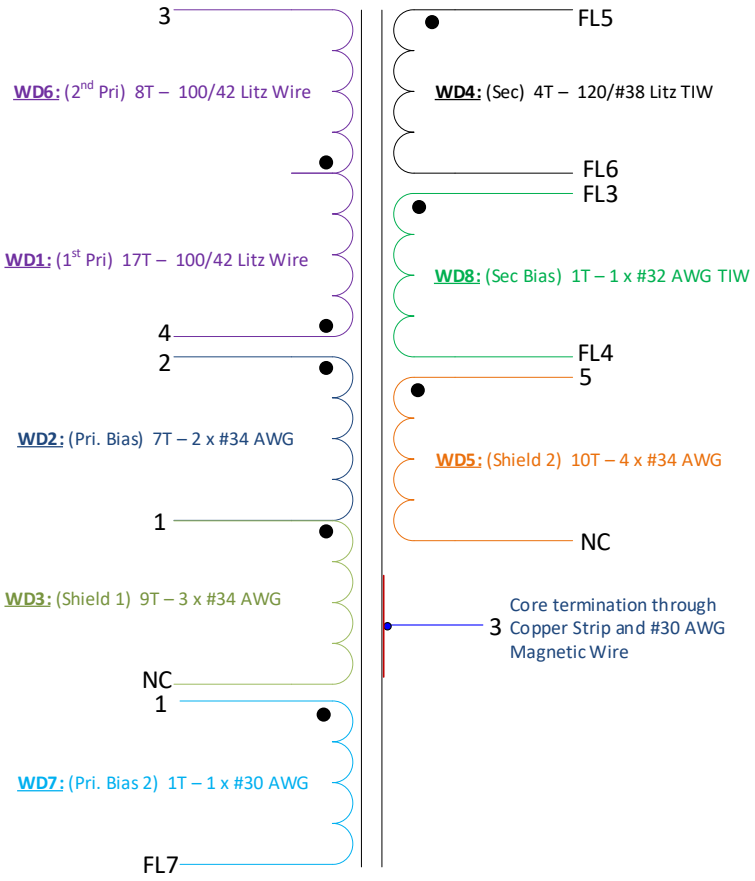


Figure 17 – Flyback Transformer (T7) Electrical Diagram.

7.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 3 and 4, with all other windings open.	320 μH ±5%
Resonant Frequency	Between pin 3 and 4, other windings open.	100 kHz (Min.)
Primary Leakage Inductance	Between pin 3 and 4, with pins: FL5-FL6 shorted.	4.5 μH (Max.)

7.3 *Material List*

Item	Description
[1]	Core: ATQ28/18 P/N: 99-00071-00.
[2]	Bobbin: Bobbin, ATQ28/18, Vertical, 5 pins. P/N: 25-01170-00.
[3]	Magnet Wire: Served Litz 100/#42
[4]	Magnet Wire: #30 AWG, Double Coated.
[5]	Magnet Wire: #34 AWG, Double Coated.
[6]	Magnet Wire: #35 AWG, Double Coated.
[7]	TIW Litz Wire: 120/#38, Triple Insulated Wire.
[8]	TIW Magnet Wire: #32 AWG, Triple Insulated Wire.
[9]	Bus Wire: #26 AWG, Alpha Wire, Tinned Copper.
[10]	3M Copper Foil (13 mm).
[12]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 9 mm Width.
[13]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 24 mm Width.
[14]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 36 mm Width.
[15]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 14 mm Width.
[16]	Varnish: Dolph BC-359.

7.4 *Transformer Build Diagram*

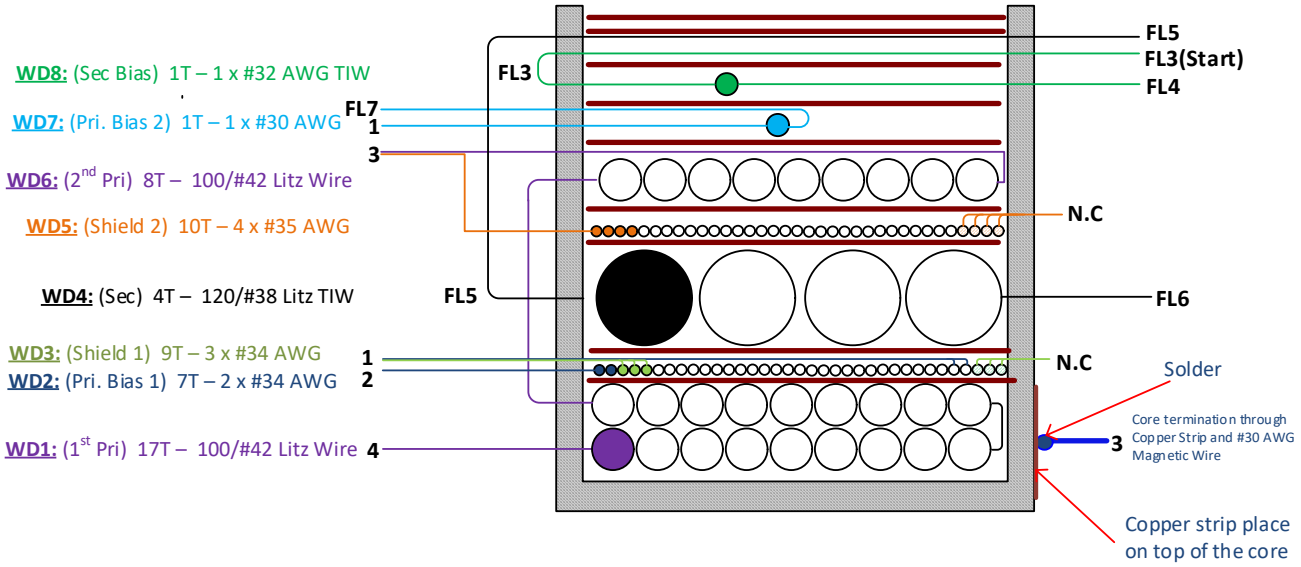
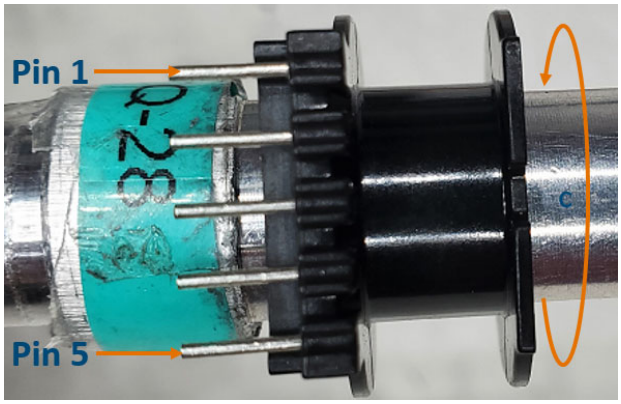
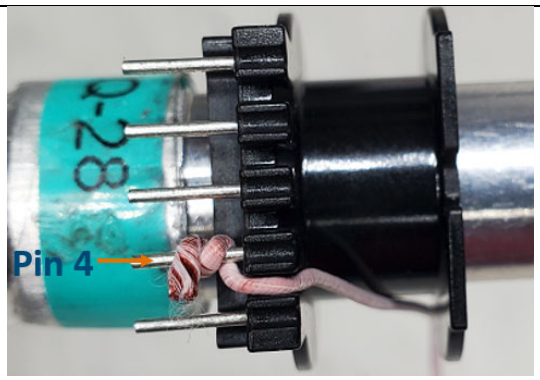


Figure 18 – Flyback Transformer (T7) Build Diagram.

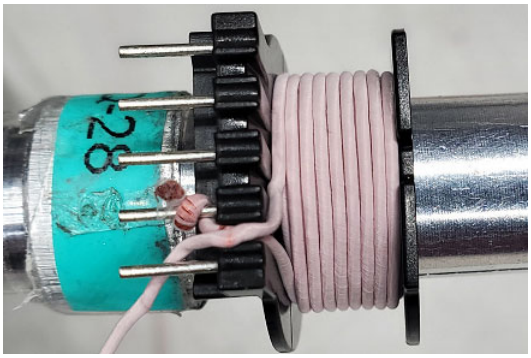
Note: Please follow below transformer build illustration to prevent shorting of wires from 2 adjacent terminals.

7.5 *Transformer Winding Instruction*

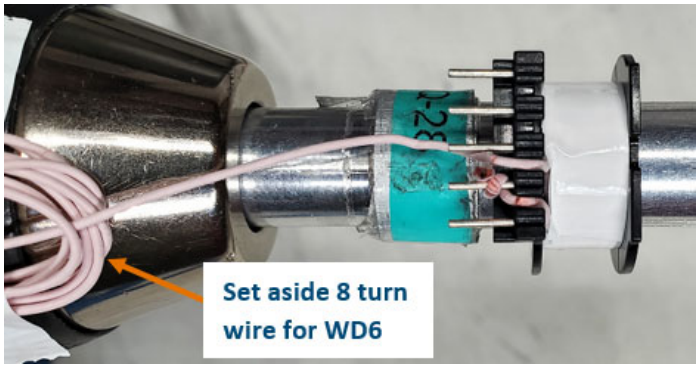
Winding Direction Use AT28/18 Bobbin (Item 2). Position the bobbin on the winding jig such that the primary side of the bobbin is on the left side with the primary terminal pins facing upward. The winding direction is clock-wise.	
Winding 1 (1st Primary) Use 100/#42 Litz magnet wire (Item 3) long enough for WD1 and WD6. Start at Pin 4 and wind 17 turns evenly for 2 layers.	



Set aside the remaining wires on the left side and fix it with tape as shown in the figure

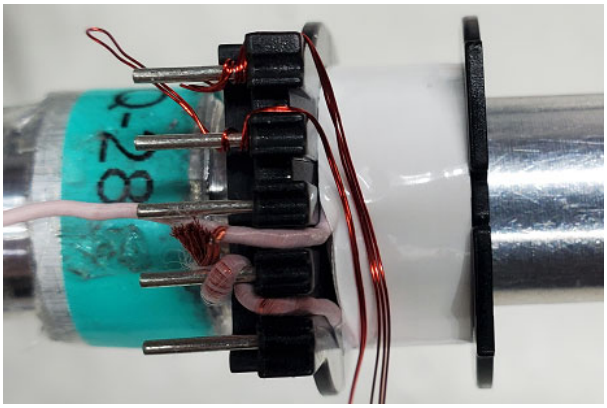


Tape Insulation
Apply 9 mm 1-layer polyester tape (Item 12) for insulation.

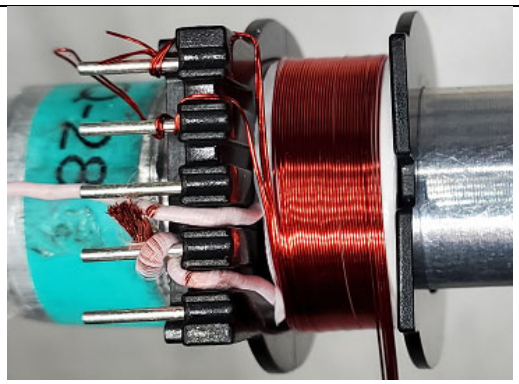


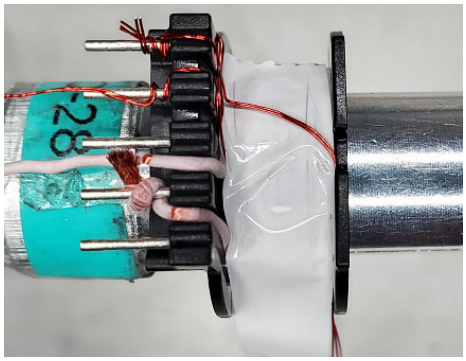
WD2: (Primary Bias) and WD:3 (Shield 1)
Use AWG#34 magnetic wire (Item 4). Prepare a bifilar wire for WD2 and trifilar wire for WD3.

WD3 will start at Pin 1 and WD2 at Pin 2.



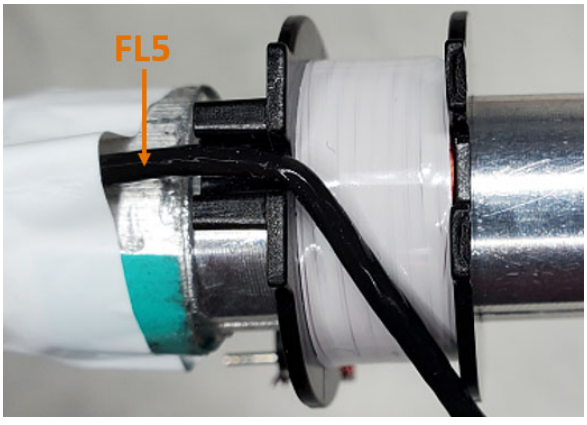
Wind WD2 and WD3 together for 7 turns. Continue to wind WD3 up to 9 turns and cut the wire at the end. Finish WD2 on Pin 1.





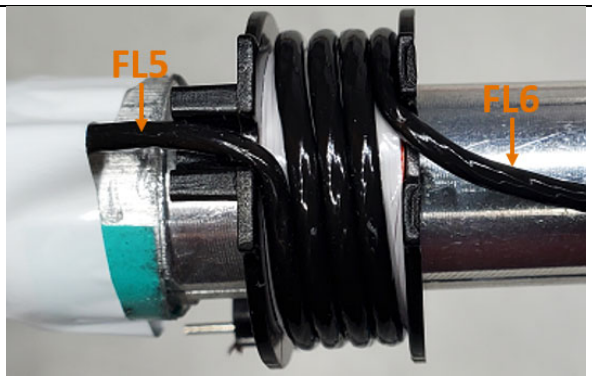
Tape Insulation
Apply 9 mm 1-layer polyester tape (Item 12) for insulation.

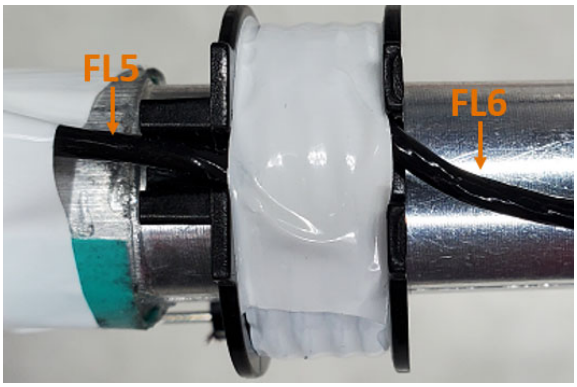
WD4: Secondary Winding
Use 120/#38 TIW Litz wire (Item 7). Position the bobbin such that the secondary wire slot is facing upward. Use tape to hold the wire on the slot. Start at FL5 and wind 4 turns evenly from left to right.



Finish the winding on the right side slot (FL6) and fix the wire with tape.

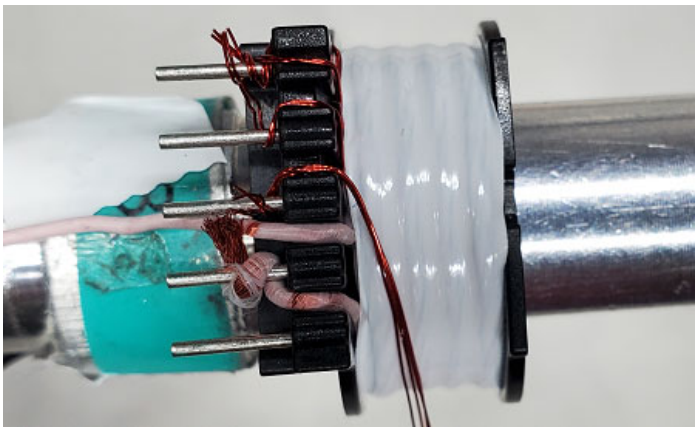
Tape Insulation
Apply 9 mm 1-layer polyester tape (Item 12) for insulation.



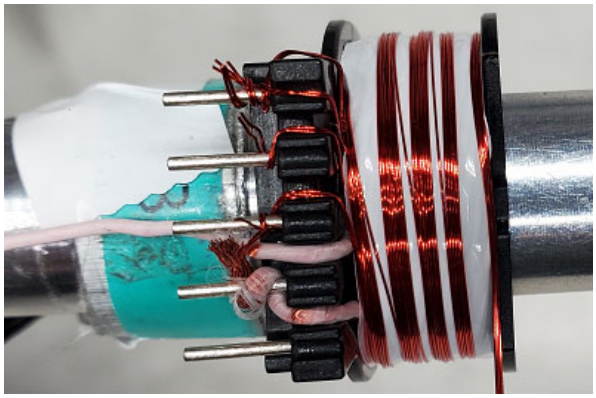


Winding 5 (Shield 2)

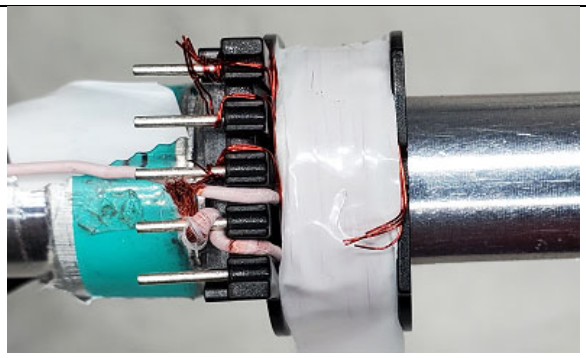
Use AWG#35 magnetic wire (Item 6). Prepare four-filar wire. Start at Pin 3 and wind 10 turns evenly from left to right in one layer.



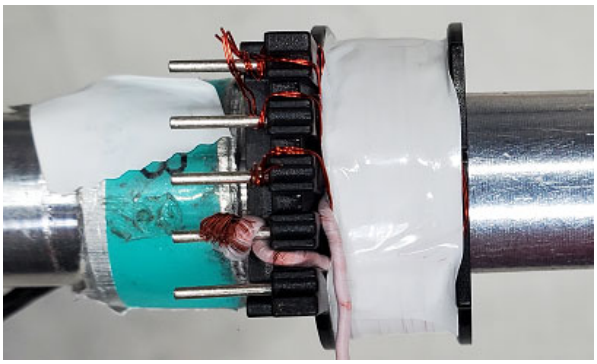
Cut the wire at the end of 10 turns on the right side.



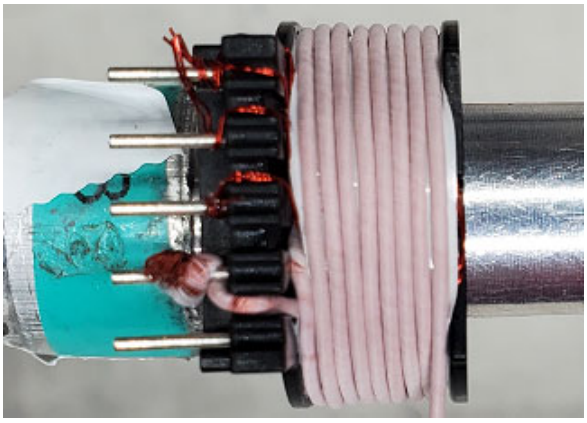
Tape Insulation
Apply 9 mm 1-layer polyester tape (Item 12) for insulation.



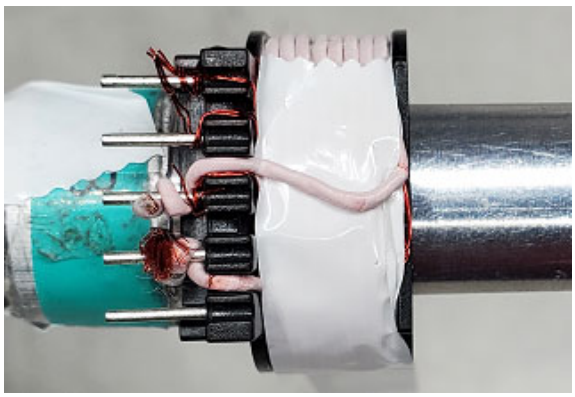
Winding 6. (2nd Primary)
Use the 100/#42 Litz magnetic wire (Item 3) that was set aside on the left from WD1. Start the winding on the left side of the bobbin and wind 8 turns evenly from left to right.



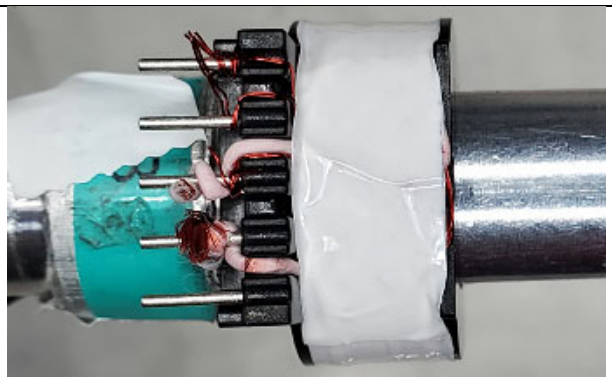
Finish the winding on Pin 3.

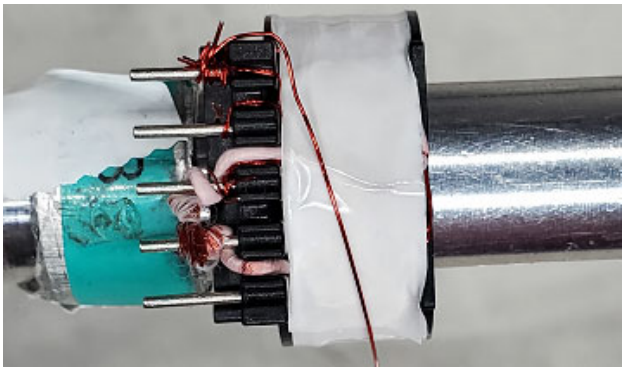


Tape Insulation
Apply 9 mm 1-layer polyester tape (Item 10) for insulation.

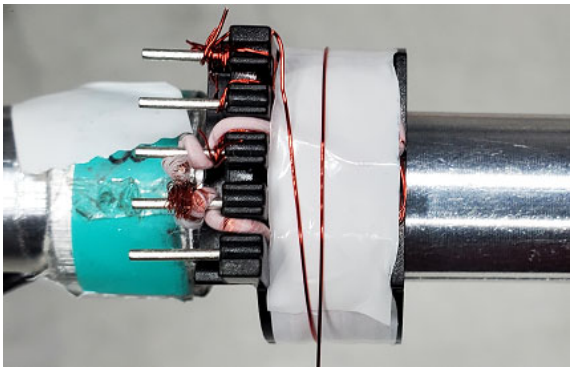


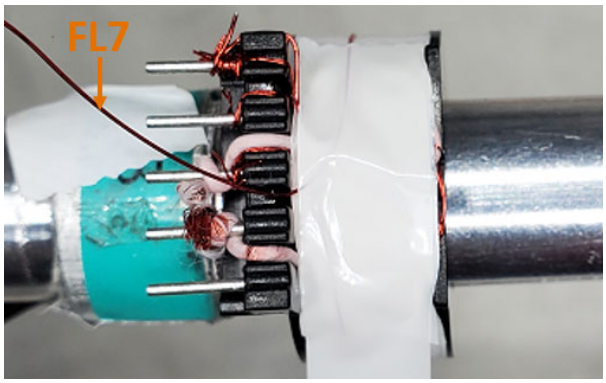
Winding 7 (Primary Bias 2)
Use AWG#30 magnetic wire. Start at Pin 1 and wind 1 turn. Finish terminal will be a fly lead wire FL7.



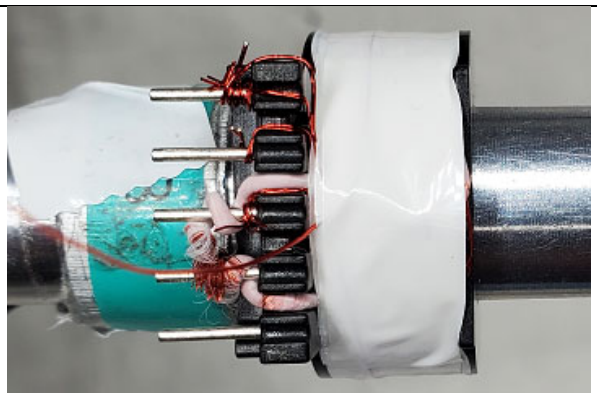


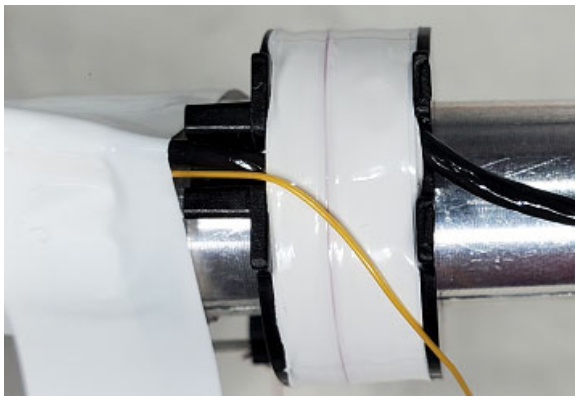
Tape Insulation
Apply 9 mm 1-layer polyester tape (Item 12) for insulation.



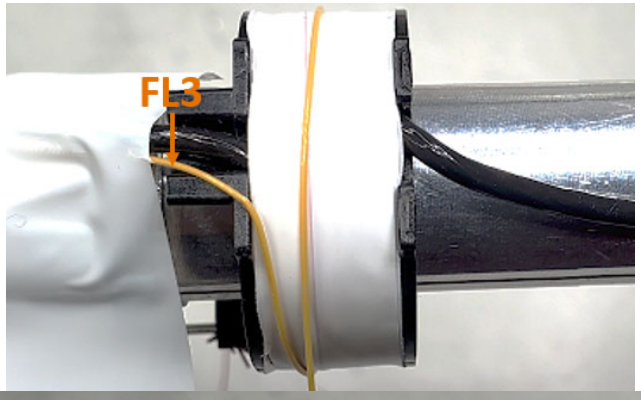


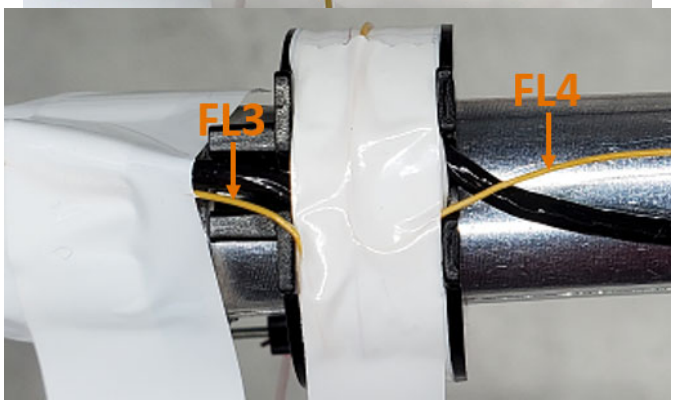
Winding 8 (Secondary Bias)
Use TIW AWG#32 (Item 8). Position the bobbin with the secondary side slot is facing upward. Start the winding (FL3) at the left side slot and wind 1 turn. Finish the winding at the right side slot with s fly lead wire (FL4).



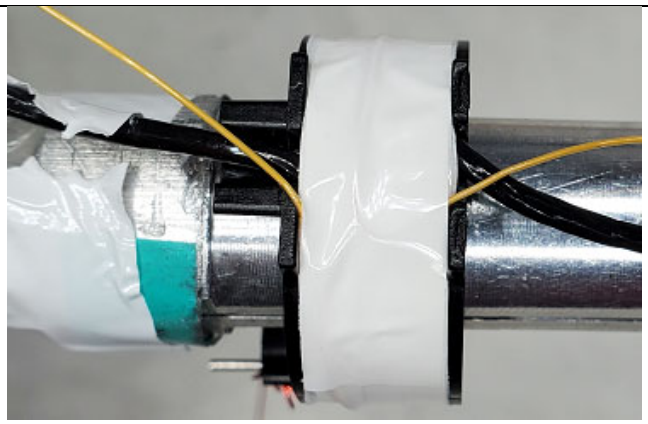


Tape Insulation
Apply 9 mm 1-layer polyester tape (Item 12) for insulation.

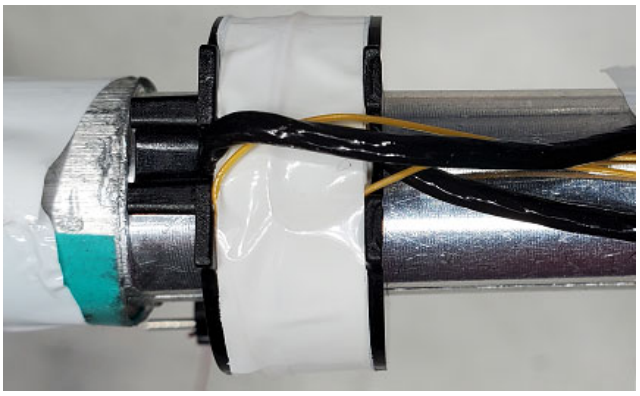




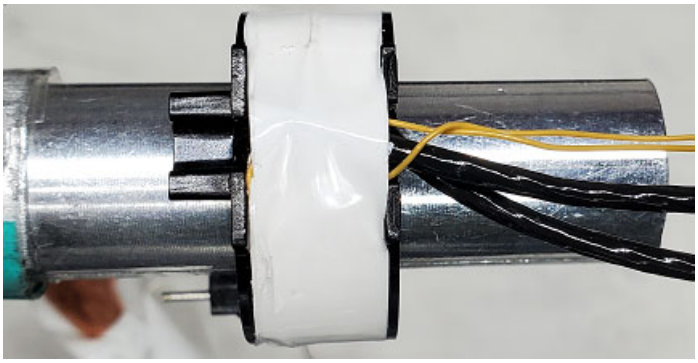
Fly Lead Wire Fixing
Fold or bend FL3 and FL5 from left side slot to the slot on the right side.



Apply 1 turn tape to fix the fly lead wires together on the right side slot.

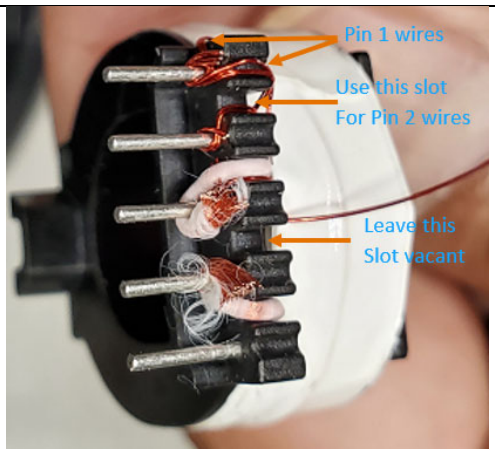


Primary Wire Soldering
Arrange the wire on the primary as shown in the figure to prevent shorting during soldering.



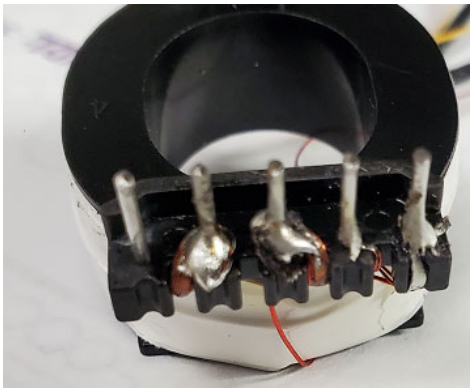
Solder the wire using solder bath.

Make sure solder accumulation is not higher than the level of the bottom ferrite core. This is to make sure the transformer is flash mounted in PCB assembly

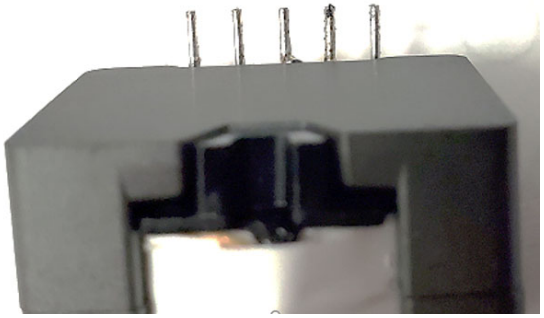


Core Inductance
Grind the center leg of the ferrite core evenly to meet the required inductance

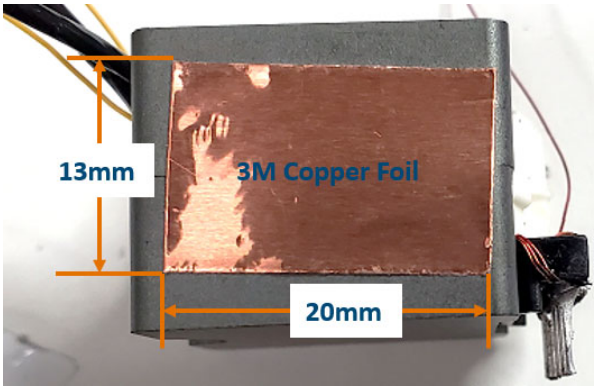
Core Fixing and Termination
Before fixing the top and bottom ferrite core with tape, Add 3M copper foil tape on the left side as shown in the figure.



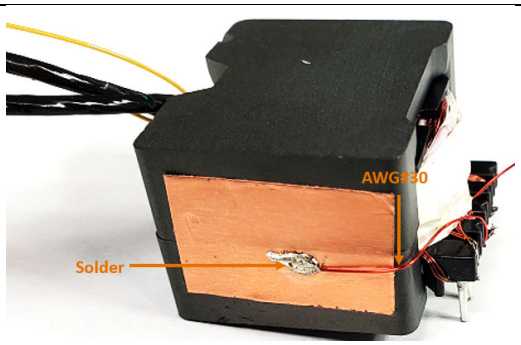
Solder a AWG#30 magnetic wire at the middle and terminate it on Pin 3.



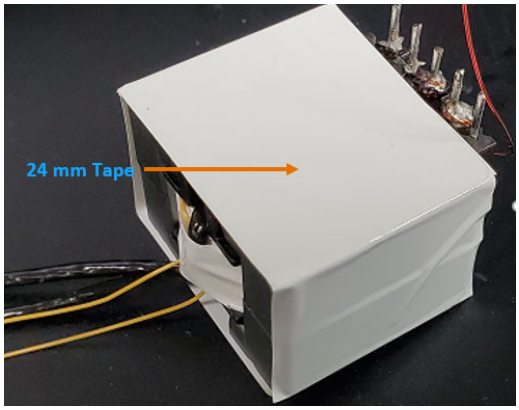
Use 24 mm polyester tape (Item 13) to fix the 2 cores. Make sure the bottom core is fully covered with tape.



Add 2 layer 36 mm polyester tape (Item 14) for reinforce safety insulation between core and secondary.

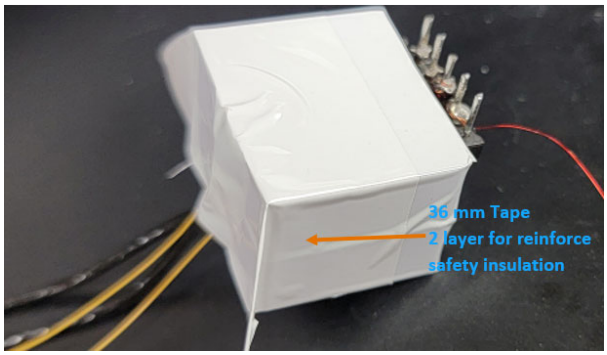


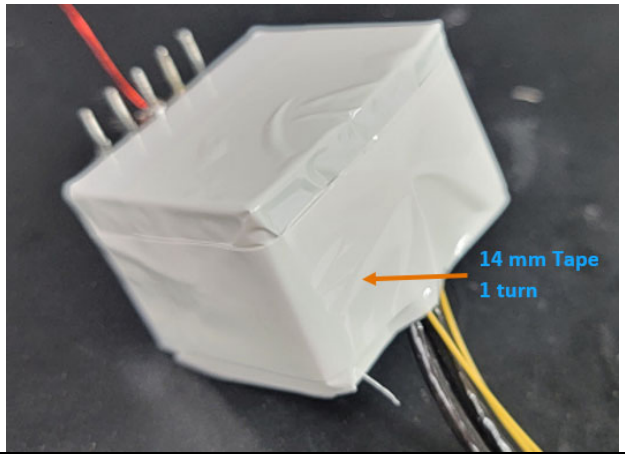
Apply 1 turn 14 mm polyester tape (Item 15) around the perimeter of the transformer to fix the safety insulation tape.



Transformer Varnishing

Dip the whole transformer in a pure varnish solution (Item 16) for 10 minutes. Cure the varnished transformer in hot(100^{0}C) oven for 30 minutes.





8 Common Mode Choke (L5) Specification

8.1 *Electrical Diagram*

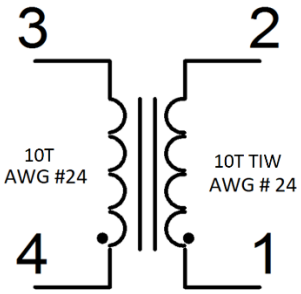


Figure 19 – CMC Electrical Diagram.

8.2 *Electrical Specifications*

Winding Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 1 and pin 2 or pin 3 and pin 4 with all other windings open.	300 µH ±20%

8.3 *Material List*

Item	Description
[1]	Toroid Core: 32-00315-00 (Green Color).
[2]	Magnet Wire: #24 AWG.
[3]	TIW Wire: #24 AWG.

8.4 *Assembled Picture*

Figure 20 – CMC Assembled Photo.

8.5 *Inductor Construction*

1. Winding 1 - Wind 10 turns of item 2 and 3 in bifilar wound as shown in above figure.

9 Boost Inductor (T8) Specification

9.1 *Electrical Diagram*

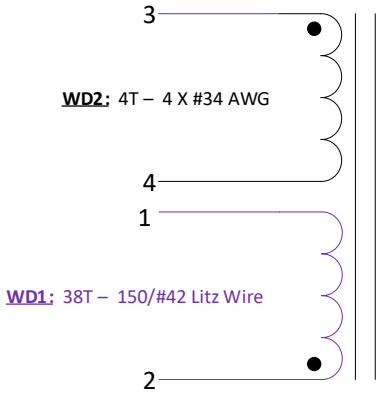


Figure 21 – Boost Inductor (T8) Electrical Diagram.

9.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 1 and 2, with all other windings open.	225 µH ±5%
Resonant Frequency	Between pin 1 and 2, other windings open	100 kHz (Min.)

9.3 *Material List*

Item	Description
[1]	Core: ATQ2718 (P/N: 99-00070-00).
[2]	Bobbin: ATQ27/18, Horizontal, 4; P/N: 25-01169-00.
[3]	Magnet Wire: Served Litz 150/42.
[4]	Magnet Wire: #34 AWG, Double Coated.
[5]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 10.5 mm Width.
[6]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 7.00 mm Width.
[7]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 20.9 mm Width
[8]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 17.6 mm Width
[9]	Varnish: Dolph BC-359.

9.4 *Boost Inductor Build Diagram*

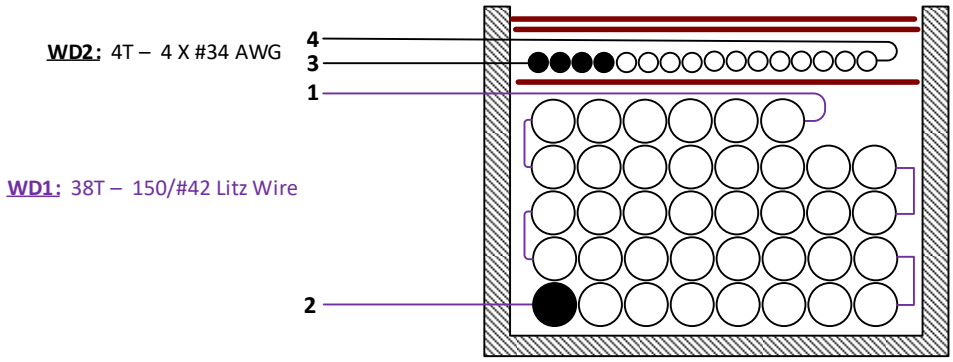
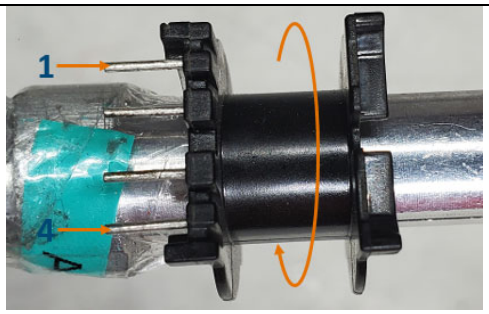


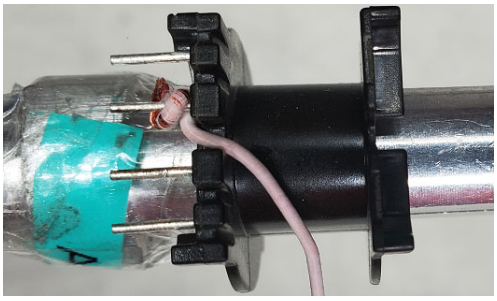
Figure 22 – Boost Inductor Build Diagram.

Note: Please follow the following transformer build illustrations to prevent shorting of wires from 2 adjacent terminals. There is also need to add polyester tape at the bottom ferrite core to prevent shorting from the primary windings.

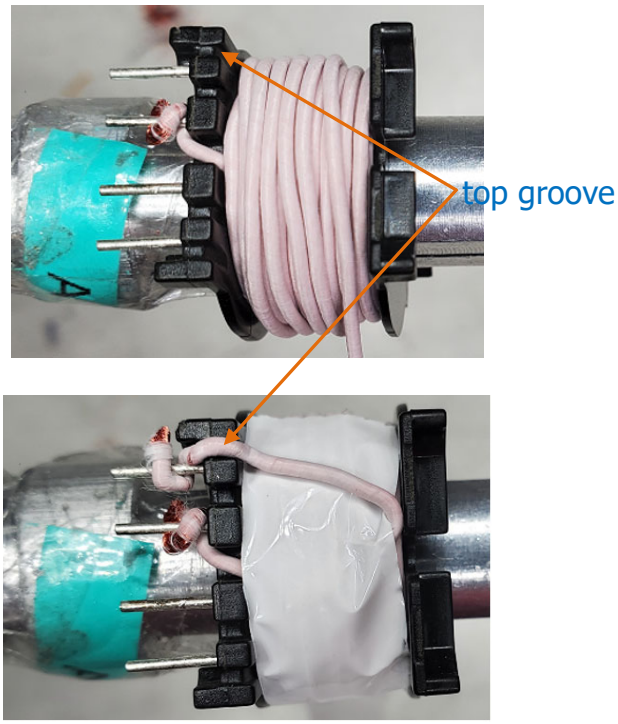
9.5 *Boost Inductor Winding Instructions*

Winding Directions
Bobbin is positioned on winder jig such that terminal Pin 1- 4 are in the left side facing upward. The inductor winding direction is clockwise.



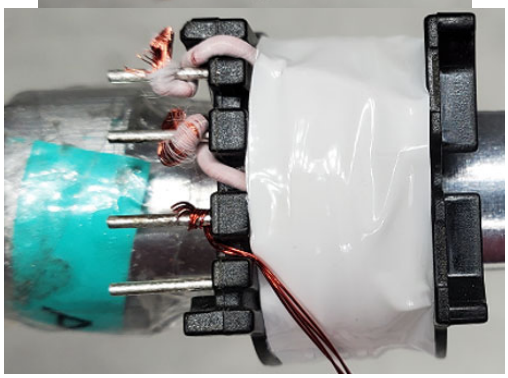


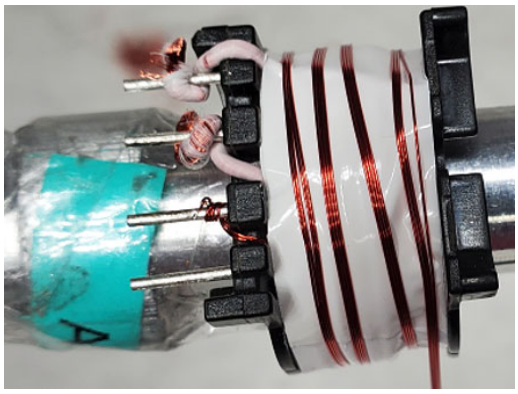
Winding 1
Use Litz wire 150/#42 (Item no. 3). Start at Pin 2 and wind 34 turns evenly.



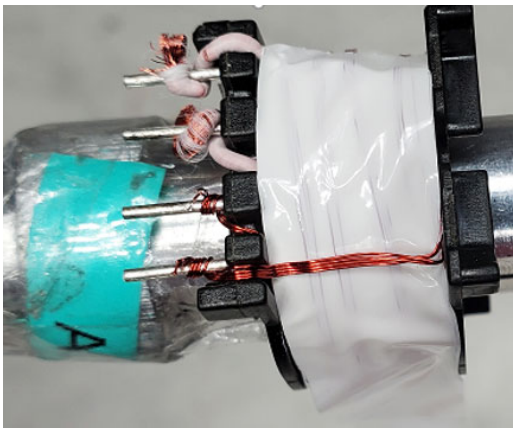
Apply 10.5 mm polyester tape (Item 5) as shown in the figure and then terminate the finish terminal to Pin 1 with the wire place on the top groove to prevent wire shorting during soldering. Continue to wind the tape for 1 layer.

Winding 2
Use four filar AWG No. 34 Magnetic Wires (Item 4). Start at Pin 3 and wind the wire from left spreading out the winding to right as shown in the figure.

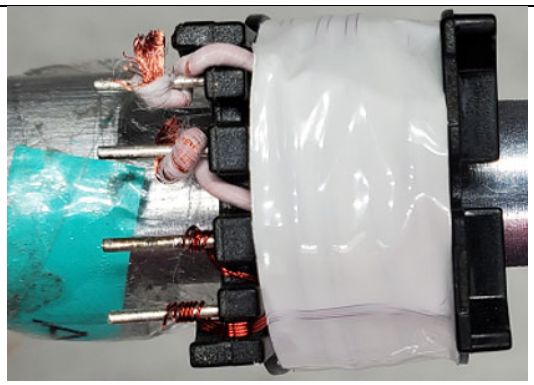




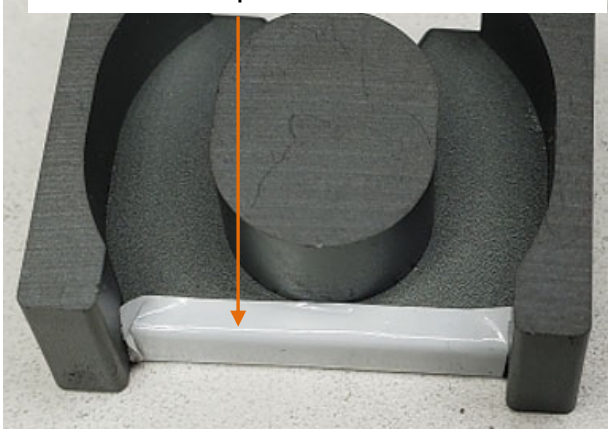
Apply 10.5 mm polyester tape (Item 5) as shown in the figure and then terminate the finish terminal to Pin 4. Continue to wind the tape for 1 layer.



Transformer Core Tape
To prevent short between the magnetic wires and transformer bottom ferrite core, Apply 7mm polyester tape (Item 6) for insulation. See figure on the right side



Bottom Ferrite Core
- Add tape on the terminal side



Core Fixing and Varnishing

Since the inductor will be flush-mounted into the board, solder the magnetic wires evenly with solder accumulation not higher than the bottom ferrite core.

Grind the center leg of the top ferrite core evenly until it matches the required inductance

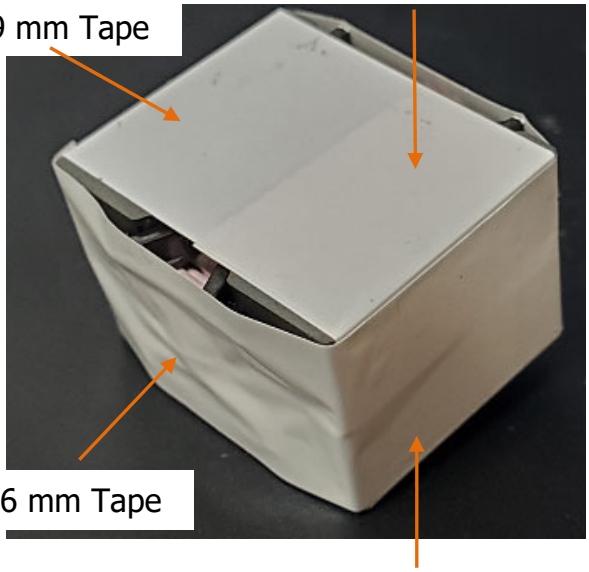
Apply 20.9 mm polyester tape (Item 7) to fix the top and bottom core.

Apply 17.6 mm polyester tape (Item 8) around the inductor as shown in the figure. This is for insulation from nearby heatsink and heat spreader

Dip varnish the transformer using Item 9. Cure the varnish inductor into 100 ^{0}C hot oven for 30 mins

Top Ferrite Core

20.9 mm Tape



17.6 mm Tape

Bottom Ferrite Core

10 InnoSwitch4-CZ Design Spreadsheet

1	ACDC_InnoSwitch4-CZ_Flyback_021722; Rev.2.1; Copyright Power Integrations 2022	INPUT	INFO	OUTPUT	UNITS	InnoSwitch4 CZ Single/Multi Output Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	INPUT_TYPE	DC		DC		Input Type
4	VIN_MIN	390		390	V	Minimum DC input voltage
5	VIN_MAX	405		405	V	Maximum DC input voltage
6	VIN_RANGE			PFC INPUT		Range of AC input voltage
7	LINEFREQ				Hz	AC Input voltage frequency
8	CAP_INPUT	82.0			uF	Input capacitor
9	VOUT	28.00	Warning	28.00	V	The output voltage exceeds the VOUT Pin voltage rating. Reduce the output voltage
10	CDC			0	mV	Cable drop compensation desired at full load
11	IOUT	5.000		5.000	A	Output current
12	POUT			140.00	W	Output power
13	EFFICIENCY	0.96		0.96		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
14	FACTOR_Z			0.60		Z-factor estimate
15	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
19	**PRIMARY CONTROLLER SELECTION**					
20	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
21	DEVICE_GENERIC	INN4077		INN4077		Generic device code
22	DEVICE_CODE			INN4077C		Actual device code
23	POUT_MAX			145	W	Power capability of the device based on thermal performance
24	RDSON_100DEG			0.25	Ω	Primary switch on time drain resistance at 100 degC
25	ILIMIT_MIN			3.162	A	Minimum current limit of the primary switch
26	ILIMIT_TYP			3.400	A	Typical current limit of the primary switch
27	ILIMIT_MAX			3.638	A	Maximum current limit of the primary switch
28	VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
29	VDRAIN_ON_PRSW			0.09	V	Primary switch on time drain voltage
30	VDRAIN_OFF_PRSW			625.0	V	Peak drain voltage on the primary switch during turn-off
34	**WORST CASE ELECTRICAL PARAMETERS**					
35	FSWITCHING_MAX	95000		95000	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
36	VOR	170.0		170.0	V	Secondary voltage reflected to the primary when the primary switch turns off
37	VMIN			390.00	V	Valley of the minimum input AC voltage at full load
38	KP			1.41		Measure of continuous/discontinuous mode of operation
39	MODE_OPERATION			DCM		Mode of operation
40	DUTYCYCLE			0.236		Primary switch duty cycle
41	TIME_ON			3.02	us	Primary switch on-time
42	TIME_OFF			7.56	us	Primary switch off-time
43	LPRIMARY_MIN			305.0	uH	Minimum primary inductance
44	LPRIMARY_TYP			321.1	uH	Typical primary inductance
45	LPRIMARY_TOL			5.0	%	Primary inductance tolerance

46	LPRIMARY_MAX			337.1	uH	Maximum primary inductance
48	**PRIMARY CURRENT**					
49	IPEAK_PRIMARY			3.527	A	Primary switch peak current
50	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
51	IAVG_PRIMARY			0.368	A	Primary switch average current
52	IRIPPLE_PRIMARY			3.527	A	Primary switch ripple current
53	IRMS_PRIMARY			0.930	A	Primary switch RMS current
55	**SECONDARY CURRENT**					
56	IPEAK_SECONDARY			22.044	A	Secondary winding peak current
57	IPEDESTAL_SECONDARY			0.000	A	Secondary winding current pedestal
58	IRMS_SECONDARY			8.805	A	Secondary winding RMS current
62	**TRANSFORMER CONSTRUCTION PARAMETERS**					
63	**CORE SELECTION**					
64	CORE	ATQ28/18.1B		ATQ28/18.1B		Core selection. Refer to the 'Transformer Construction' tab to see the detailed report
65	CORE CODE			ATQ28/18.1B		Core code
66	AE			153.00	mm^2	Core cross sectional area
67	LE			47.70	mm	Core magnetic path length
68	AL			9800	nH/turns^2	Ungapped core effective inductance
69	VE			7298.0	mm^3	Core volume
70	BOBBIN			TBI-238-07271.17XX		Bobbin
71	AW			37.40	mm^2	Window area of the bobbin
72	BW			8.50	mm	Bobbin width
73	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
75	**PRIMARY WINDING**					
76	NPRIMARY			25		Primary turns
77	BPEAK			3282	Gauss	Peak flux density
78	BMAX			3076	Gauss	Maximum flux density
79	BAC			1538	Gauss	AC flux density (0.5 x Peak to Peak)
80	ALG			514	nH/turns^2	Typical gapped core effective inductance
81	LG			0.355	mm	Core gap length
83	**PRIMARY BIAS WINDING**					
84	NBIAS_PRIMARY			7		Primary bias winding number of turns
86	**SECONDARY WINDING**					
87	NSECONDARY			4		Secondary winding number of turns
89	**SECONDARY BIAS WINDING**					
90	NBIAS_SECONDARY			1		Secondary bias winding number of turns
94	**PRIMARY COMPONENTS SELECTION**					
95	**CLAMPZERO**					
96	LLEAK			3.21	uH	Primary winding leakage inductance
97	CCLAMP			100.0	nF	Primary clamp capacitor
98	RD_CLAMPZERO	30		30	kΩ	HSD resistor
99	TLLDL/THLDL			430.0	ns	HSD resistor programmed delay
100	TIME_CLAMPZERO_OFF_TO_PRIMARY_ON			375.0	ns	Time between the ClampZero FET turn off and the primary FET turns on based on the HSD resistor selection
101	TIME_VDS_VALLEY			36.9	ns	Time taken by the VDS ring to reach its first valley
102	IPEAK_CLAMPZERO			3.475	A	Active clamp peak current
104	**LINE UNDERVOLTAGE**					
105	BROWN-IN REQURED			97.5	V	Required AC RMS/DC line voltage brown-in threshold
106	RLS			3.48	MΩ	Connect two 1.74 MOhm resistors to the V-pin for the required UV/OV threshold
107	BROWN-IN ACTUAL			98.7	V	Actual AC RMS/DC brown-in threshold

108	BROWN-OUT ACTUAL			89.3	V	Actual AC RMS/DC brown-out threshold
110	**LINE OVERVOLTAGE**					
111	OVERVOLTAGE_LINE			411.3	V	Actual AC RMS/DC line over-voltage threshold
113	**PRIMARY BIAS DIODE**					
114	VBIAS_PRIMARY	45.0		45.0	V	Rectified primary bias voltage
115	VF_BIAS_PRIMARY			0.70	V	Bias winding diode forward drop
116	VREVERSE_BIASDIODE_PRIMARY			158.40	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
117	CBIAS_PRIMARY			22	uF	Bias winding rectification capacitor
118	CBPP			0.47	uF	BPP pin capacitor
122	**SECONDARY COMPONENTS**					
123	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
124	RFB_LOWER			4.75	kΩ	Lower feedback resistor
125	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
127	**SECONDARY BIAS DIODE**					
128	USE_SECONDARY_BIAS	AUTO		YES		Use secondary bias winding for the design
129	VBIAS_SECONDARY			5.0	V	Rectified secondary bias voltage
130	VF_BIAS_SECONDARY			0.70	V	Bias winding diode forward drop
131	VREVERSE_BIASDIODE_SECONDARY			21.20	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
132	CBIAS_SECONDARY			10	uF	Bias winding rectification capacitor
133	CBPS			2.20	uF	BPP pin capacitor
136	**MULTIPLE OUTPUT PARAMETERS**					
137	**OUTPUT 1**					
138	VOUT1			28.00	V	Output 1 voltage
139	IOUT1			5.00	A	Output 1 current
140	POUT1			140.00	W	Output 1 power
141	IRMS_SECONDARY1			8.805	A	Root mean squared value of the secondary current for output 1
142	IRIPPLE_CAP_OUTPUT1			7.248	A	Current ripple on the secondary waveform for output 1
143	NSECONDARY1			4		Number of turns for output 1
144	VREVERSE_RECTIFIER1			92.80	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
145	SRFET1	Auto		AON7254		Secondary rectifier (Logic MOSFET) for output 1
146	VF_SRFET1			0.330	V	SRFET on-time drain voltage for output 1
147	VBREAKDOWN_SRFET1			150	V	SRFET breakdown voltage for output 1
148	RDSON_SRFET1			66.0	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1

11 HiperPFS-5 Design Spreadsheet

1	Hiper_PFS-5_Boost_031722; Rev.1.0; Copyright Power Integrations 2022	INPUT	INFO	OUTPUT	UNITS	Discontinuous Mode Boost Converter Design Spreadsheet
2	**Enter Application Variables**					
3	Input Voltage Range	Universal		Universal		Input voltage range
4	VACMIN			90	VAC	Minimum AC input voltage. Spreadsheet simulation is performed at this voltage. To examine operation at other votlages, enter here, but enter fixed value for LPFC_ACTUAL.
5	VACMAX			265	VAC	Maximum AC input voltage
6	VBROWNIN			82	VAC	Expected Typical Brown-in Voltage per IC specifications; Line impedance not accounted for.
7	VBROWNOUT			71	VAC	Expected Typical Brown-out voltage per IC specifications; Line impedance not accounted for.
8	VO			400	VDC	Nominal load voltage
9	PO	145		145	W	Nominal Output power
10	fL			50	Hz	Line frequency
11	TA Max			40	°C	Maximum ambient temperature
12	Efficiency Estimate	0.9600		0.9600		Enter the efficiency estimate for the boost converter at VACMIN. Should approximately match calculated efficiency in Loss Budget section
13	VO_MIN			380	VDC	Minimum Output voltage
14	VO_RIPPLE_MAX			20	VDC	Maximum Output voltage ripple
15	T_HOLDUP		Warning	20	ms	Expected holdup time is smaller than specified value. Please use larger Output capacitance
16	VHOLDUP_MIN			320	VDC	Minimum Voltage Output can drop to during holdup
17	I_INRUSH			40	A	Maximum allowable inrush current
18	Forced Air Cooling	No		No		Enter "Yes" for Forced air cooling. Otherwise enter "No". Forced air reduces acceptable choke current density and core autopick core size
20	**KP and INDUCTANCE**					
21	LPFC_MIN (0 bias)			216	uH	Minimum PFC inductance value
22	LPFC_TYP (0 bias)	225		225	uH	LPFC value used for calculations. Enter value to hold constant (also enter core selection) while changing VACMIN to examine brownout operation.
23	LPFC_MAX (0 bias)		Warning	234	uH	LPFC_MAX exceeds the maximum required inductance (231 uH) for power delivery
24	LP_TOL	4.0		4.0	%	Tolerance of PFC Inductor Value (ferrite only)
25	LPFC_PEAK			225	uH	Inductance at VACMIN and maximum bias current. For Ferrite, same as LPFC_DESIRED (0 bias)
26	KP_ACTUAL			1.15		Actual KP calculated from LPFC_DESIRED
28	Basic Current Parameters					
29	IAC_RMS			1.68	A	AC input RMS current at VACMIN and Full Power load
30	IL_RMS			2.00	A	Inductor RMS current (calculated at VACMIN and Full Power Load)
31	IO_DC			0.36	A	Output average current/Average diode current
34	**PFS Parameters**					
35	PFS Package			F		HiperPFS package selection
36	PFS Part Number	PFS5177F		PFS5177F		If examining brownout operation, over-ride autopick with desired device size

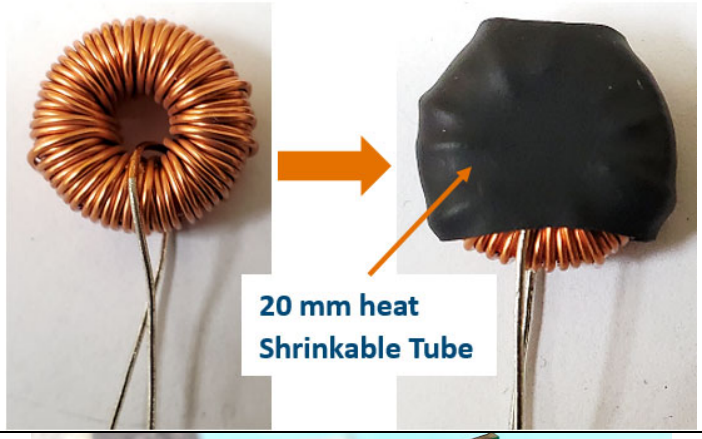
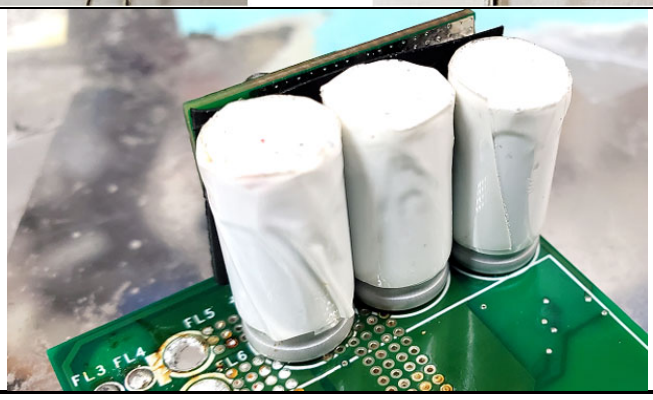
37	Self-Supply Feature	Yes		Yes		Device self-supply feature. Select "Yes" to select device with self-supply feature or "No" for device without self-supply
38	PS_FACTOR	0.8		0.8		Programmable output power selection factor
39	PO_MAX_DEV			148	W	Maximum output power of the device
40	IOCP min			4.60	A	Minimum Current limit
41	IOCP typ			6.00	A	Typical current limit
42	IOCP max			7.20	A	Maximum current limit
43	IP			4.52	A	MOSFET peak current
44	IRMS			1.74	A	PFS MOSFET RMS current
45	RDSON			0.23	Ohms	Typical RDSon at 100 'C
46	FS_PK			80.8	kHz	Estimated frequency of operation at crest of input voltage (at VACMIN)
47	FS_AVG			71.1	kHz	Estimated average frequency of operation over line cycle (at VACMIN)
48	PCOND_LOSS_PFS			0.695	W	Estimated PFS Switch conduction losses
49	PSW_LOSS_PFS			0.019	W	Estimated PFS Switch switching losses
50	PFS_TOTAL			0.714	W	Total Estimated PFS Switch losses
51	TJ Max			100	deg C	Maximum steady-state junction temperature
52	Rth-JS			2.80	°C/W	Maximum thermal resistance (Junction to heatsink)
53	HEATSINK Theta-CA			81.21	°C/W	Maximum thermal resistance of heatsink
56	**INDUCTOR DESIGN**					
57	**Material and Dimensions**					
58	Core Type	Ferrite		Ferrite		Enter "Sendust", "Iron Powder" or "Ferrite"
59	Core Material	Auto		PC44/PC95		Select from 60u, 75u, 90u or 125 u for Sendust cores. Fixed at PC44/PC95 for Ferrite cores. Fixed at -52 material for Pow Iron cores.
60	Core Geometry	ATQ		ATQ		Toroid only for Sendust and Powdered Iron; EE or PQ for Ferrite cores.
61	Core	ATQ27/18		ATQ27/18		Core part number
62	Ae			131.00	mm^2	Core cross sectional area
63	Le			50.80	mm	Core mean path length
64	AL			7350.00	nH/t^2	Core AL value
65	Ve			6.66	cm^3	Core volume
66	HT (EE/PQ/EQ/RM/POT) / ID (toroid)			4.90	mm	Core height/Height of window; ID if toroid
67	MLT			56.4	mm	Mean length per turn
68	BW			10.40	mm	Bobbin width
69	LG			0.95	mm	Gap length (Ferrite cores only)
70	**Flux and MMF Calculations**					
71	BP_TARGET (ferrite only)	3500		3500	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
72	B_OCP (or BP)			3476	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
73	B_MAX			2099	Gauss	Peak flux density at AC peak, VACMIN and Full Power Load, nominal inductance,minimum IOCP
74	µ_TARGET (powder only)			N/A	%	target µ at peak current divided by µ at zero current, at VACMIN, full load (powder only) - drives auto core selection
75	µ_MAX (powder only)			N/A	%	actual µ at peak current divided by µ at zero current, at VACMIN, full load (powder only)
76	µ_OCP (powder only)			N/A	%	µ at IOCPtyp divided by µ at zero current
77	I_TEST			6.0	A	Current at which B_TEST and H_TEST are calculated, for checking flux at a current other than IOCP or IP; if blank IOCP_typ is used.
78	B_TEST			2897	Gauss	Flux density at I_TEST and maximum tolerance inductance
79	µ_TEST (powder only)			N/A	%	µ at IOCP divided by µ at zero current, at IOCPtyp
80	**Wire**					

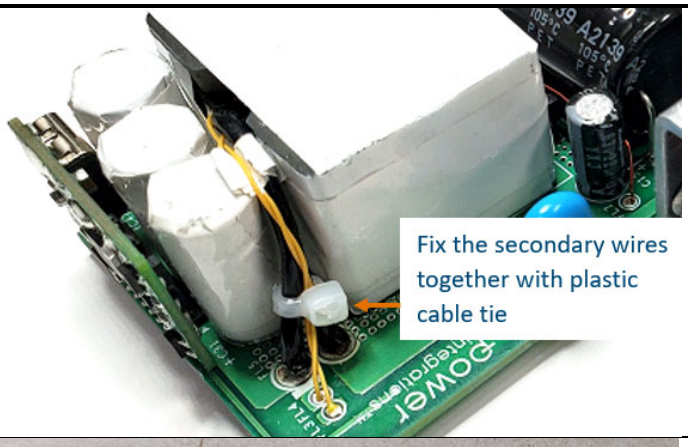
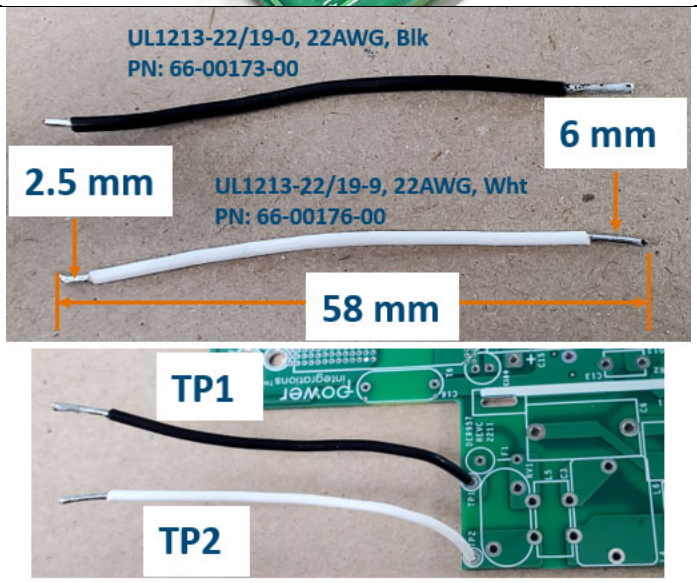
81	TURNS			37		Inductor turns. To adjust turns, change BP_TARGET (ferrite) or µ_TARGET (powder)
82	ILRMS			2.00	A	Inductor RMS current
83	Wire type	Litz		Litz		Select between "Litz" or "Magnet" for double coated magnet wire
84	AWG	42		42	AWG	Inductor wire gauge
85	Filar	100		100		Inductor wire number of parallel strands. Leave blank to auto-calc for Litz
86	OD (per strand)			0.064	mm	Outer diameter of single strand of wire
87	OD bundle (Litz only)			0.89	mm	Will be different than OD if Litz
88	DCR			0.147	ohm	Choke DC Resistance
89	P AC Resistance Ratio			0.32		Ratio of total copper loss, including HF AC, to the DC component of the loss
90	J		Warning	6.33	A/mm^2	Current density is high, if copper loss is high use thicker wire, more strands, or larger core
91	Layers			3.33		Estimated layers in winding
92	**Auxiliary Winding**					
93	N_AUX			4		Recommended auxiliary winding number of turns to ensure the supply to the VS pin
94	V_VS_MAX			1.24	V	Maximum voltage across the auxiliary winding
95	V_VS_MIN			-30.39	V	Minimum voltage across the auxiliary winding
96	RVS			10.00	kohm	Recommended series resistor to the VS pin. Place as close as possible to the VS pin of Hiper-PFS5
97	**Loss Calculations**					
98	BAC-p-p			2051	Gauss	Core AC peak-peak flux excursion at VACMIN, peak of sine wave
99	LPFC_CORE_LOSS			0.193	W	Estimated Inductor core Loss
100	LPFC_COPPER_LOSS			0.604	W	Estimated Inductor copper losses
101	LPFC_TOTAL_LOSS			0.797	W	Total estimated Inductor Losses
104	**PFC Diode**					
105	PFC Diode Part Number	Auto		LXA03T600		PFS Diode Part Number
106	Type / Part Number			Qspeed		PFC Diode Type / Part Number
107	Manufacturer			PI		Diode Manufacturer
108	VRRM			600.0	V	Diode rated reverse voltage
109	IF			3.00	A	Diode rated forward current
110	Qrr			43.0	nC	Qrr at High Temperature
111	VF			2.10	V	Diode rated forward voltage drop
112	PCOND_DIODE			0.772	W	Estimated Diode conduction losses
113	PSW_DIODE			0.000	W	Estimated Diode switching losses
114	P_DIODE			0.772	W	Total estimated Diode losses
115	TJ Max			100.0	deg C	Maximum steady-state operating temperature
116	Rth-JS			3.30	degC/W	Maximum thermal resistance (Junction to heatsink)
117	HEATSINK Theta-CA			73.87	degC/W	Maximum thermal resistance of heatsink
118	IFSM			23.0	A	Non-repetitive peak surge current rating. Consider larger size diode if inrush or thermal limited.
121	**Output Capacitor**					
122	COUT	82		82	uF	Minimum value of Output capacitance
123	VO_RIPPLE_EXPECTED			14.7	V	Expected ripple voltage on Output with selected Output capacitor
124	T_HOLDUP_EXPECTED			16.3	ms	Expected holdup time with selected Output capacitor
125	ESR_LF			1.38	ohms	Low Frequency Capacitor ESR
126	ESR_HF			0.55	ohms	High Frequency Capacitor ESR
127	IC_RMS_LF			0.23	A	Low Frequency Capacitor RMS current
128	IC_RMS_HF			0.90	A	High Frequency Capacitor RMS current
129	CO_LF_LOSS			0.074	W	Estimated Low Frequency ESR loss in Output capacitor
130	CO_HF_LOSS			0.448	W	Estimated High frequency ESR loss in Output capacitor
131	Total CO LOSS			0.522	W	Total estimated losses in Output Capacitor

134	**Input Bridge (BR1) and Fuse (F1)**					
135	I^2t Rating			5.76	A^2*s	Minimum I^2t rating for fuse
136	Fuse Current rating			2.60	A	Minimum Current rating of fuse
137	VF			0.90	V	Input bridge Diode forward Diode drop
138	IAVG			1.62	A	Input average current at VBROWNOUT.
139	PIV_INPUT BRIDGE			375	V	Peak inverse voltage of input bridge
140	PCOND_LOSS_BRIDGE			2.720	W	Estimated Bridge Diode conduction loss
141	CIN			0.47	uF	Input capacitor. Use metallized polypropylene or film foil type with high ripple current rating
142	CIN_DF			0.001		Input Capacitor Dissipation Factor (tan Delta)
143	CIN_PLOSS			0.008	W	Input Capacitor Loss
144	RT1			9.37	ohms	Input Thermistor value
145	D_Precharge			1N5407		Recommended precharge Diode
148	**PFS5 Small Signal Components**					
149	RVS			10.0	kOhms	VS pin resistor for valley sensing. This resistor should be optimized such that proper delay is introduced from the instant the voltage on the sense winding goes below the Vvs2 threshold to the instant when the cascode turns-on (valley sensing). Must be tested on the bench
150	RPS			25 - 50	kOhms	Power programmability resistor
151	RV1			4.0	MOhms	Line sense resistor 1
152	RV2			6.0	MOhms	Line sense resistor 2
153	RV3			6.0	MOhms	Typical value of the lower resistor connected to the V-PIN. Use 1% resistor only!
154	RV4			155.5	kOhms	Description pending, could be modified based on feedback chain R1-R4
155	C_V			0.514	nF	V pin decoupling capacitor (RV4 and C_V should have a time constant of 80us) Pick the closest available capacitance.
156	C_VCC			1.0	uF	Supply decoupling capacitor
157	C_C			100	nF	Feedback C pin decoupling capacitor
158	Power good Vo lower threshold VPG(L)			333	V	Vo lower threshold voltage at which power good signal will trigger
159	PGT set resistor			320.5	kohm	Power good threshold setting resistor
162	**Feedback Components**					
163	RFB_1			4.00	Mohms	Feedback network, first high voltage divider resistor
164	RFB_2			6.00	Mohms	Feedback network, second high voltage divider resistor
165	RFB_3			6.00	Mohms	Feedback network, third high voltage divider resistor
166	RFB_4			155.5	kohms	Feedback network, lower divider resistor
167	CFB_1			0.514	nF	Feedback network, loop speedup capacitor. (R4 and C1 should have a time constant of 80us) Pick the closest available capacitance.
168	RFB_5			23.7	kohms	Feedback network: zero setting resistor
169	CFB_2			1000	nF	Feedback component- noise suppression capacitor
172	**Loss Budget (Estimated at VACMIN)**					
173	PFS Losses			0.714	W	Total estimated losses in PFS
174	Boost diode Losses			0.772	W	Total estimated losses in Output Diode
175	Input Bridge losses			2.720	W	Total estimated losses in input bridge module
176	Input Capacitor Losses			0.008	W	Total estimated losses in input capacitor
177	Inductor losses			0.797	W	Total estimated losses in PFC choke
178	Output Capacitor Loss			0.522	W	Total estimated losses in Output capacitor
179	EMI choke copper loss			0.282	W	Total estimated losses in EMI choke copper
180	Total losses			5.815	W	Overall loss estimate
181	Efficiency			96.14	%	Estimated efficiency at VACMIN, full load.
184	**HiperPFS-5 Integrated CAPZero Function**					
185	Total Series Resistance (Rcapzero1+Rcapzero2)			0.730	MOhms	Maximum total series resistor value to discharge X-capacitors with time constant of 1 second. Resistors must be connected to D1 and D2 pins

						of the HiperPFS-5 part for integrated CAPZero function
188	**EMI Filter Components Recommendation**					
189	CX2			470	nF	X-capacitor after differencial mode choke and before bridge, ratio with Po
190	LDM_calc			270	uH	Estimated minimum differential inductance to avoid <10kHz resonance in input current
191	CX1			470	nF	X-capacitor before common mode choke, ratio with Po
192	LCM			10.0	mH	Typical common mode choke value
193	LCM_leakage			30	uH	Estimated leakage inductance of CM choke, typical from 30~60uH
194	CY1 (and CY2)			220	pF	typical Y capacitance for common mode noise suppression
195	LDM_Actual			240	uH	cal_LDM minus LCM_leakage, utilizing CM leakage inductance as DM choke.
196	DCR_LCM			0.070	Ohms	Total DCR of CM choke for estimating copper loss
197	DCR_LDM			0.030	Ohms	Total DCR of DM choke(or CM #2) for estimating copper loss
199	Note: CX2 can be placed between CM choke and DM choke depending on EMI design requirement.					

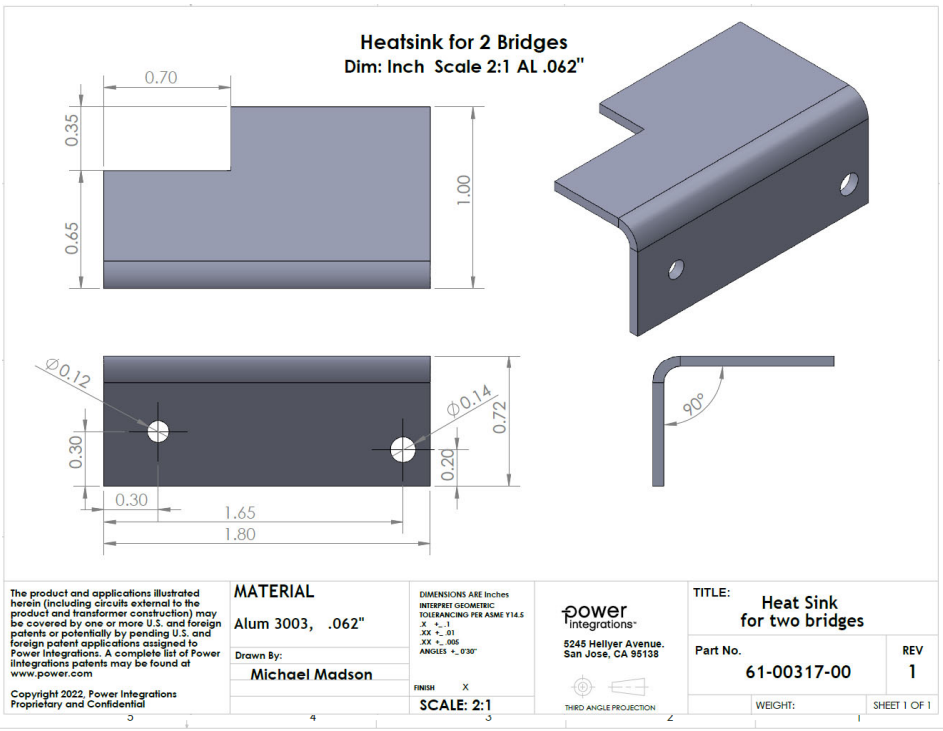
12 Special Assembly Instructions

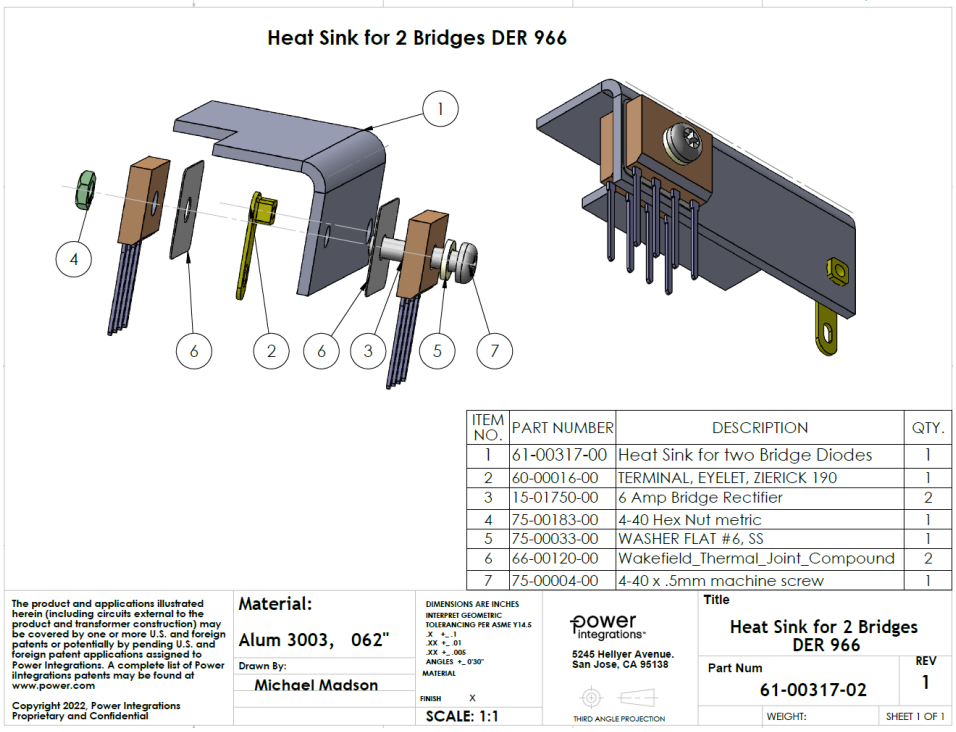
L6 – Differential Input Choke Add 20 mm heat shrinkable tube for insulation	
C26, C31 and C47 – Output Capacitors Apply 2 layer tape as shown in the figure	

T6 – Flyback Transformer Use plastic cable tie to fix the secondary wires together. This will shorten the noisy secondary wire loop.	
TP1/TP2 – Input Line Terminals Use 58 mm AWG #22 cable wires for TP1 and TP2.	

13 Heat Sink Assembly

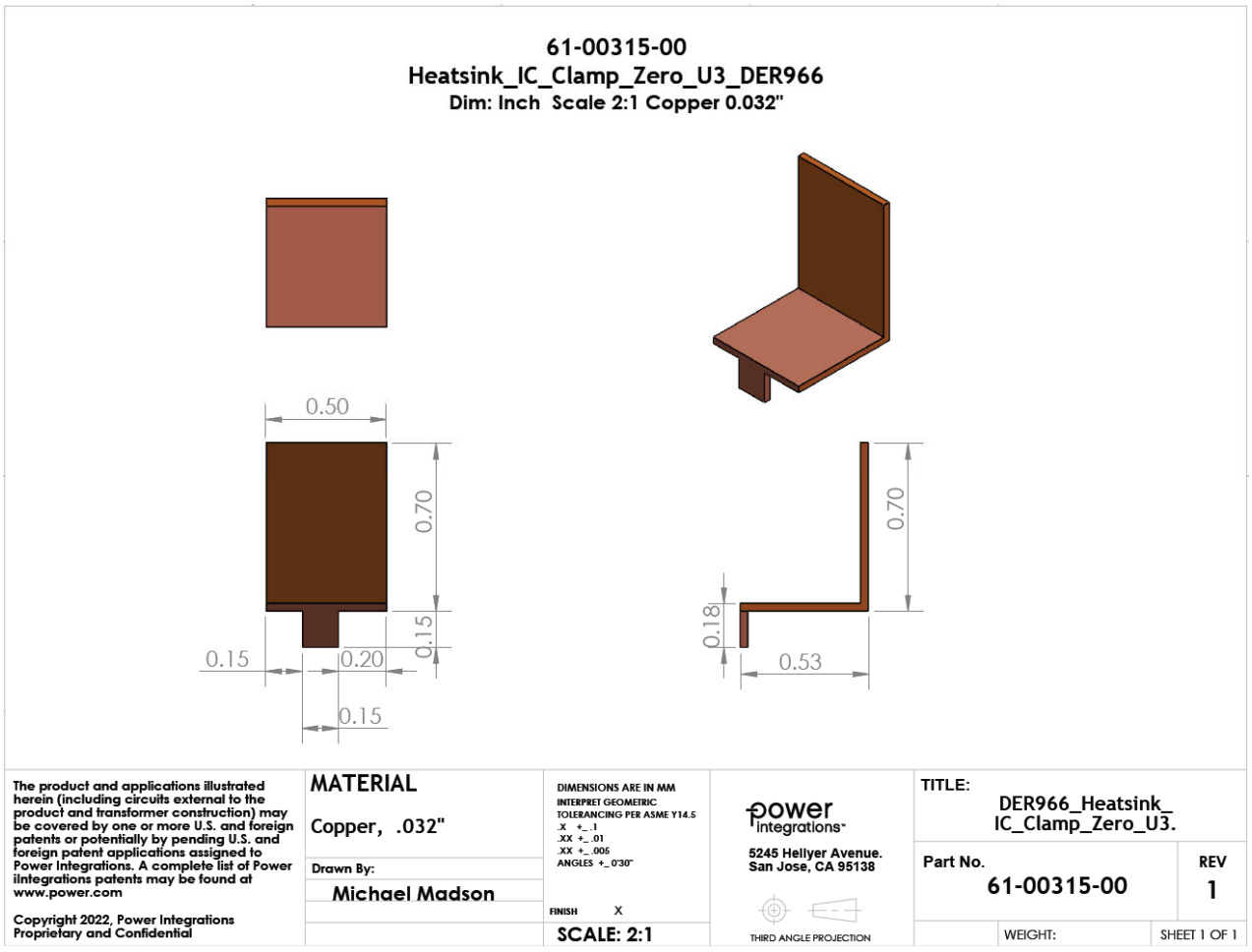
13.1 *Bridge Diode (BR1 / BR2) Heat Sink Assembly*



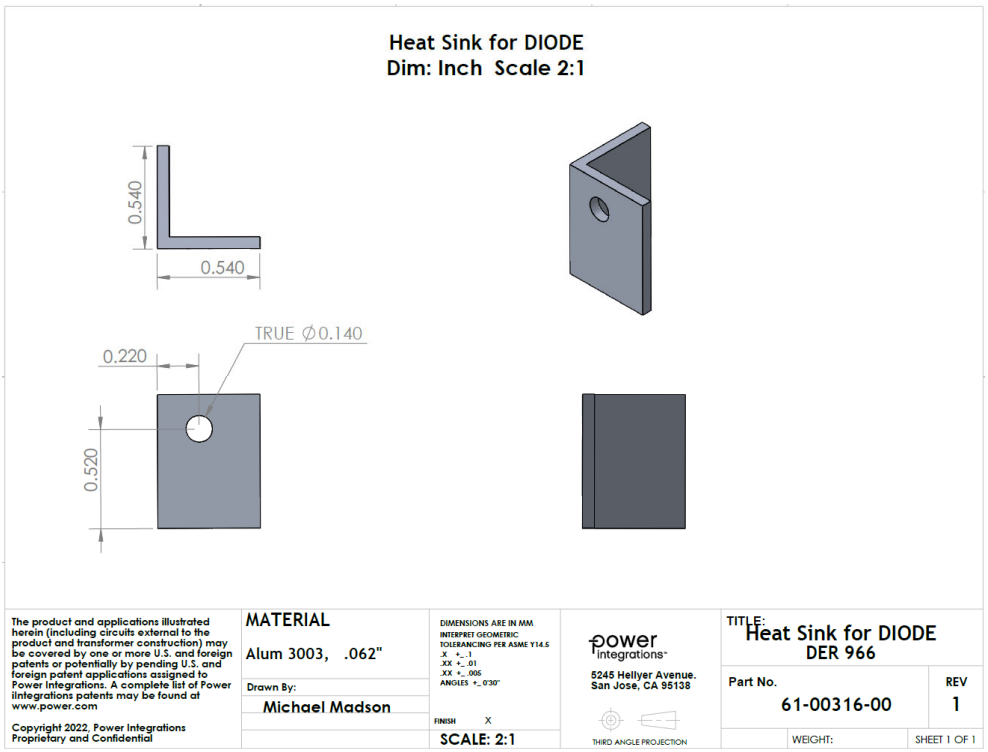


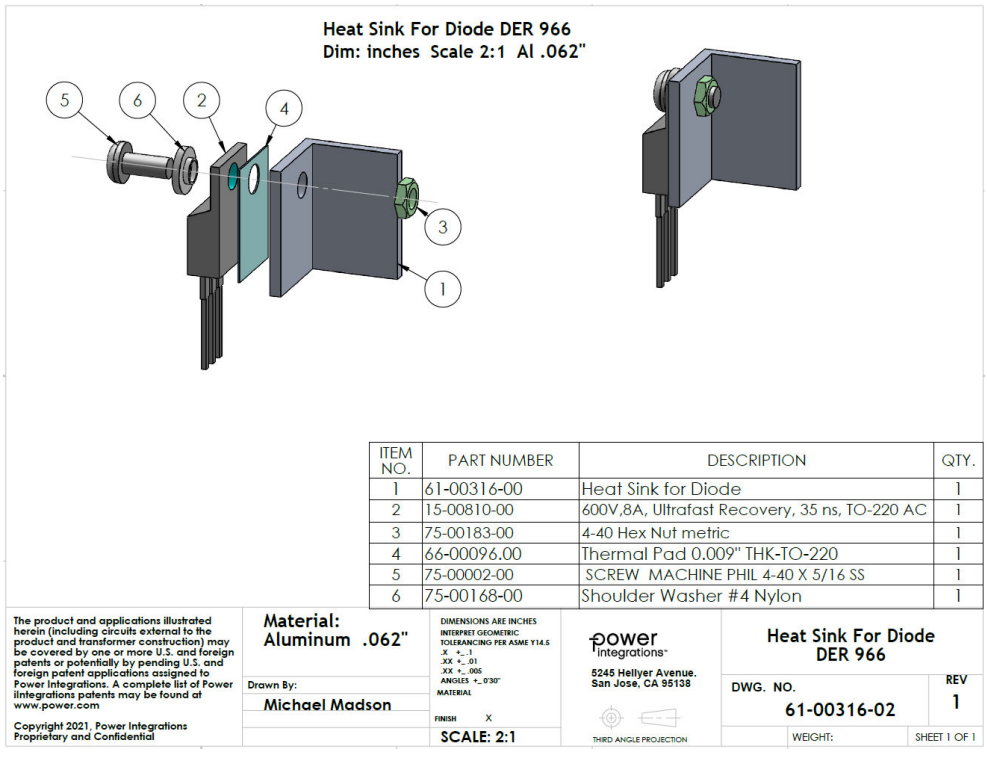
ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00317-00	Heat Sink for two Bridge Diodes	1
2	60-00016-00	TERMINAL, EYELET, ZIERICK 190	1
3	15-01750-00	6 Amp Bridge Rectifier	2
4	75-00183-00	4-40 Hex Nut metric	1
5	75-00033-00	WASHER FLAT #6, SS	1
6	66-00120-00	Wakefield_Thermal_Joint_Compound	2
7	75-00004-00	4-40 x .5mm machine screw	1

13.2 *U3 Heat Sink*



13.3 *D13 Heat Sink Assembly*

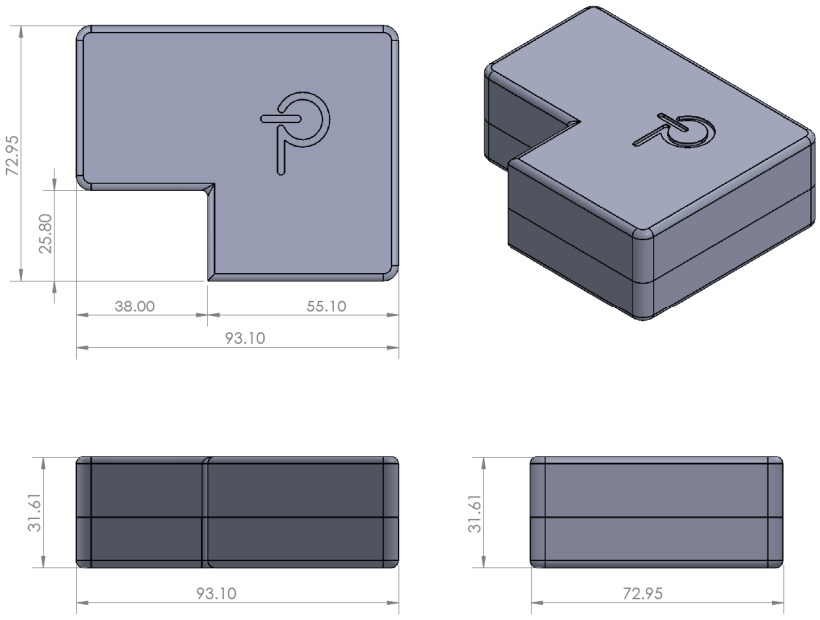




ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00316-00	Heat Sink for Diode	1
2	15-00810-00	600V,8A, Ultrafast Recovery, 35 ns, TO-220 AC	1
3	75-00183-00	4-40 Hex Nut metric	1
4	66-00096.00	Thermal Pad 0.009" THK-TO-220	1
5	75-00002-00	SCREW MACHINE PHIL 4-40 X 5/16 SS	1
6	75-00168-00	Shoulder Washer #4 Nylon	1

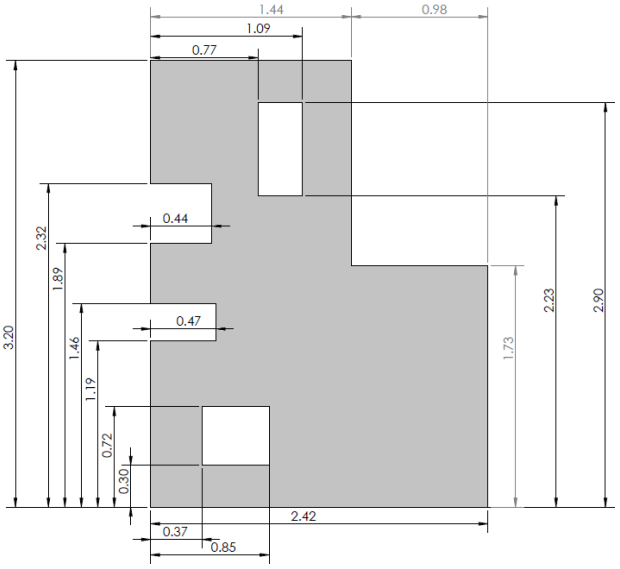
14 Enclosure Assembly

14.1 *Plastic Enclosure*



14.2 *Heat Spreader*

14.3 *Heat Spreader Bottom Side Insulator*



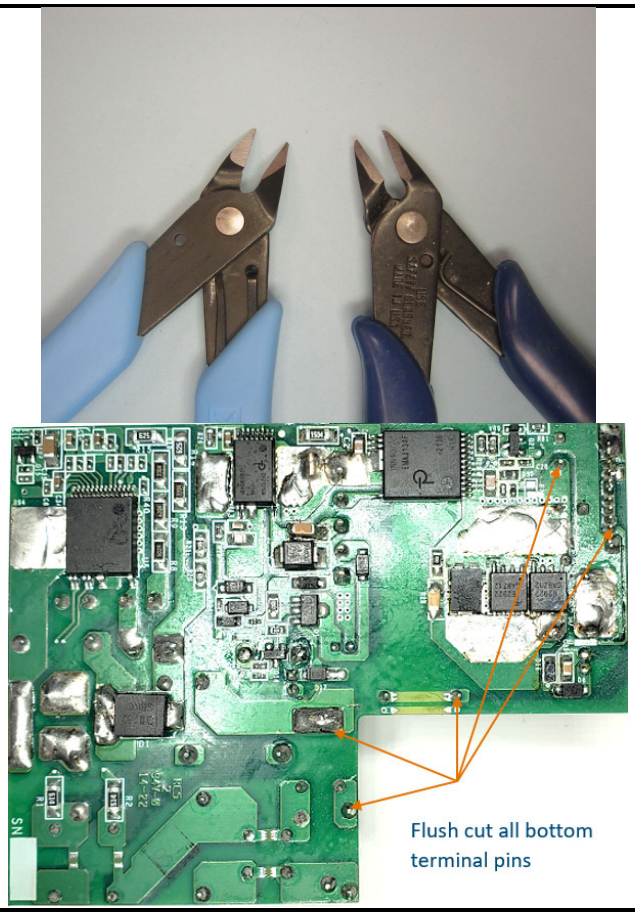
Material: MYLAR301 - MYLAR SHEET,WC, 0.003" thick
P/N: 66-00230-00

14.4 *Heat Spreader Assembly Instruction*

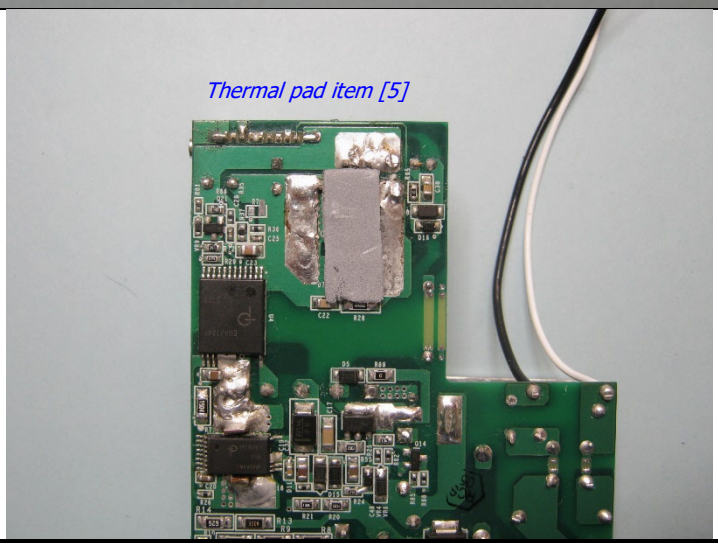
14.4.1 Material List

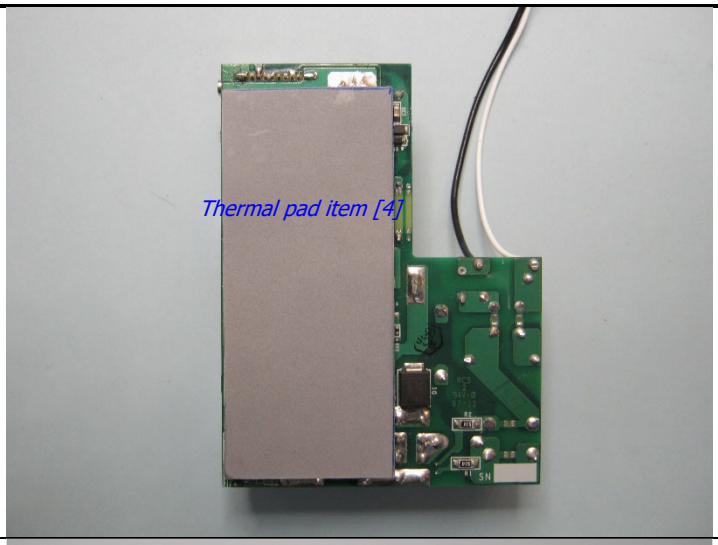
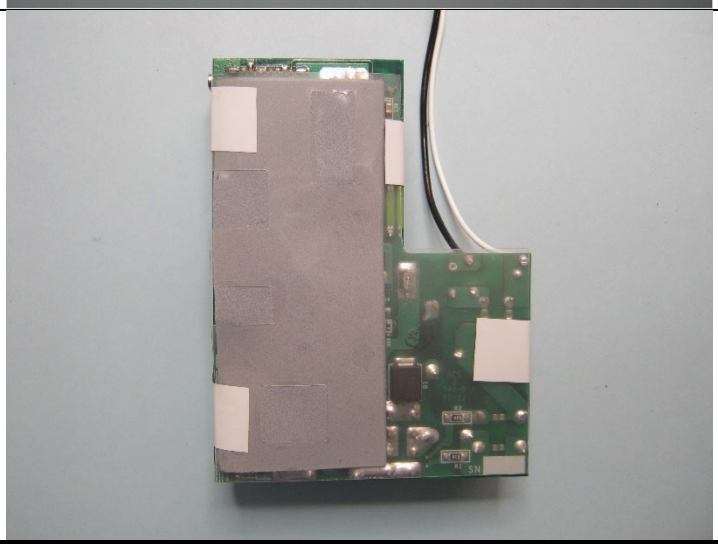
Item	Description
[1]	Aluminum Metal Sheet; 0.016”.
[2]	Copper Metal Sheet; 0.015”.
[3]	Clear, Mylar Teijin, 3 mil Thick, PI#:61-00312-00.
[4]	Thermal Pad, at Bottom of PCB, Material: 3M, 1.0 mm Thick, 66-00382-00, dim: 2.9” x 1.3”.
[5]	Thermal Pad, for FETs, Material: 3M, 0.5 mm Thick, 66-00383-00, dim: 0.75” x 0.27”.
[6]	Thermal Pad, for Daughter Board, Material: 3M, 1.0 mm Thick, 66-00382-00, dim: 0.90” x 0.64”.
[7]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 7.0 mm Width; or Equivalent.

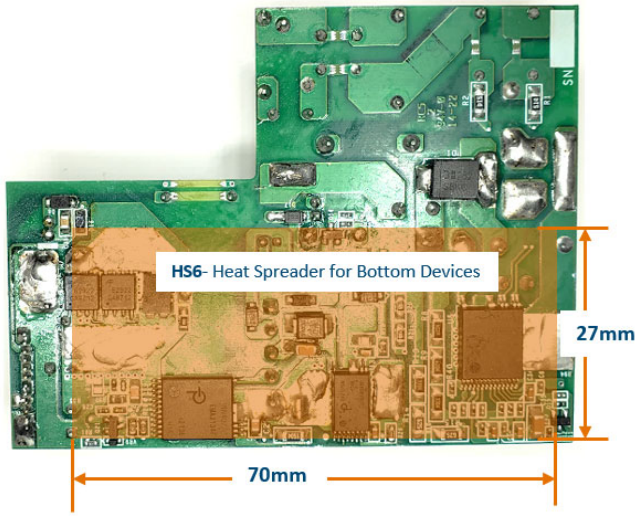
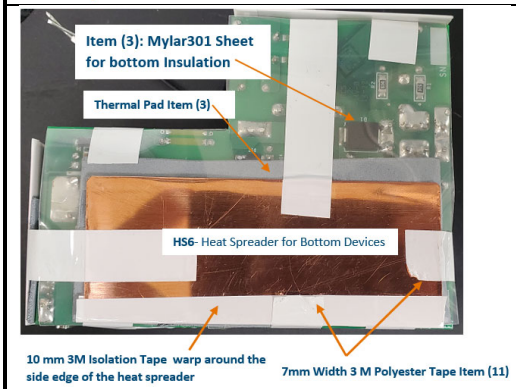
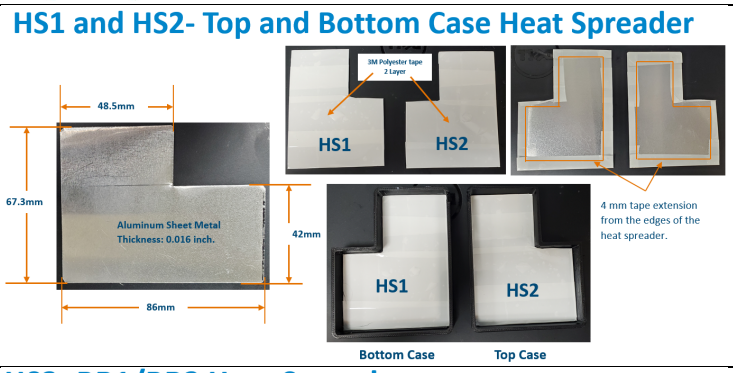
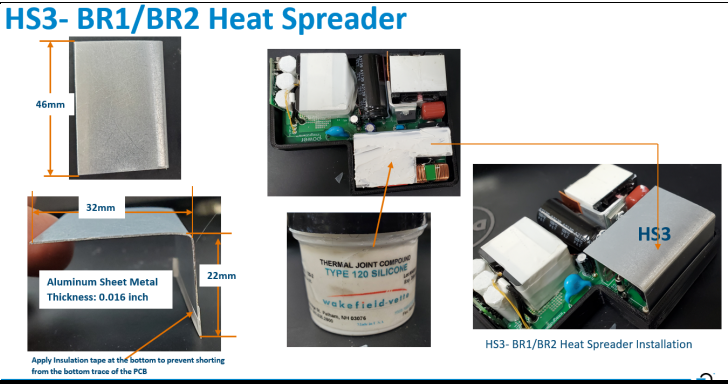
14.4.2 Assembly Illustration

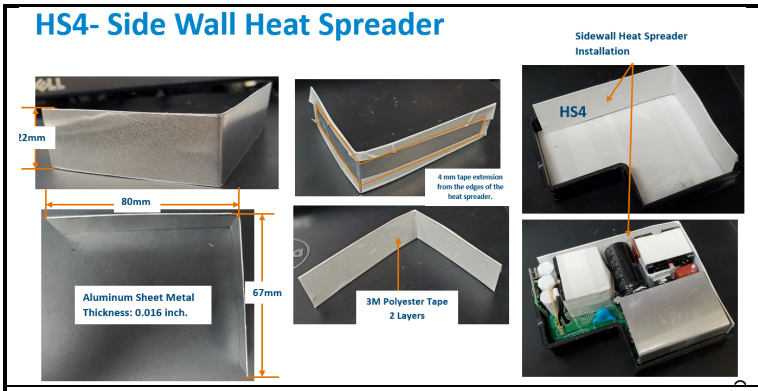
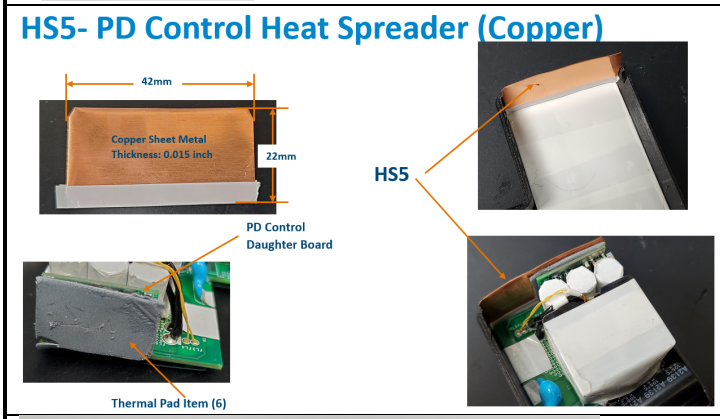
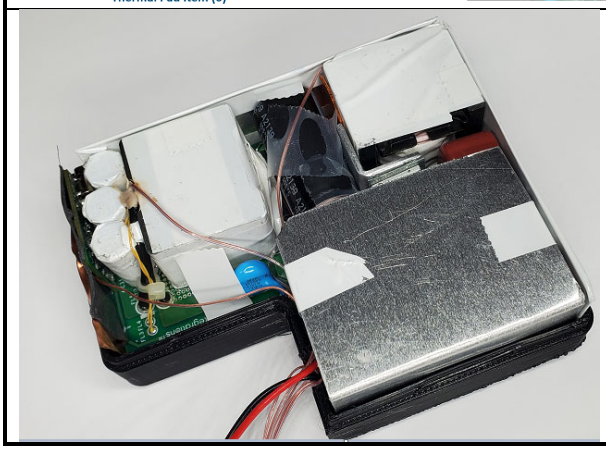


Use proper flush cutters such as shown in this picture to have all terminal pins of PCB to be flush cut to avoid any pins poking into the thermal pads. *(see illustration beside for reference).*

	Prepare thermal pads item [4]
	Prepare thermal pads item [5]
	Place thermal pad item [5] on top of D7, Q4 and Q12 at the bottom of PCB.

	Place thermal pad item [4] at the bottom of PCB as shown in the figure
	Prepare insulator item [3].
	Place the mylar sheet insulator item (3) on top of thermal pad. Add tape (Item 7) to fix the mylar sheet and the thermal pad into the PCB.

	Prepare **HS6 Heat Spreader** using 0.015-inch copper metal sheet. HS6 rectangular dimension is 27mm x 70mm.
	Place the HS6 heat spreader as shown in the figure and apply 7 mm width polyester tape (Item 7) to fix it tightly on top of the thermal pad.
	HS1 and HS2 Heat Spreader Outline and Installation
	HS3-BR1/BR2 Heat Spreader Outline and Installation

	HS4 – Side Wall Heat Spreader Outline and Installation
	HS5 – PD control board Heat Spreader Outline and Installation. Before inserting the PCB assembly inside the bottom case, place item 6 (thermal pad) at the bottom of the PD control board. Please the HS5 (PD control heat spreader) on the side of case and insert the PCB assembly with the thermal pad item (6) attached. See the figure on the left side.
	Case Installation – Insert the PSU with the heat spreader intact as shown in the figure

15 Performance Data

Output voltages are measured at the PCB end and all the measurements are taken at room temperature unless otherwise specified.

15.1 *No-Load Input Power at 5 V_{OUT}*

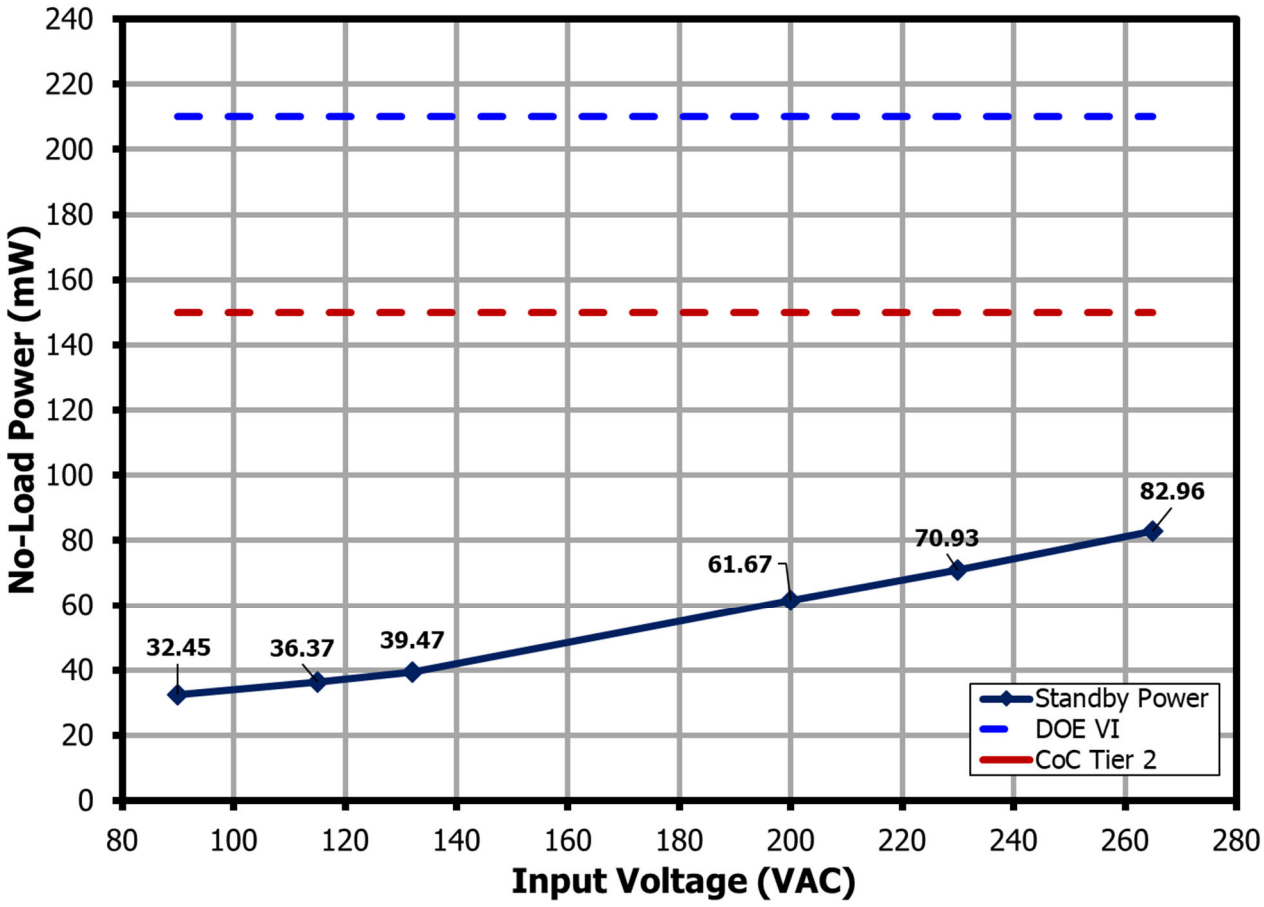


Figure 23 – No-Load Input Power vs. Input Line Voltage.

15.2 *Average and 10% Load Efficiency*

Note: Output voltage measured at the USB-PD connector on the board. Efficiency measured at room temperature after warming up the unit for 15 min @ full load.

15.2.1 Efficiency Requirements

		Test	Average	Average	10% Load
		Effective	2016	Jan-16	Jan-16
V_{OUT} (V)	Model (V)	Power (W)	New EISA2007	CoC v5 Tier 2	CoC v5 Tier 2
5	<6	15	81.4%	81.8%	72.5%
9	>6	27	86.6%	87.3%	77.3%
15	>6	45	87.7%	88.9%	78.9%
20	>6	100	88.0%	89.0%	79.0%
28	>6	130	88.0%	89.0%	79.0%

15.2.2 Efficiency Performance Summary (On Board)

V_{OUT} (V)	Power (W)	Average Efficiency (%)		10% Load Efficiency (%)	
		115 VAC	230 VAC	115 VAC	230 VAC
5	15	91.66	89.66	88.19	79.04
9	27	92.10	92.34	86.42	84.52
15	45	90.38	93.48	79.08	86.23
20	100	92.83	93.80	89.16	90.41
28	140	93.43	94.38	88.71	88.17

15.2.3 Average and 10% Load Efficiency at 115 VAC

15.2.3.1 Average Efficiency Chart at 115 VAC

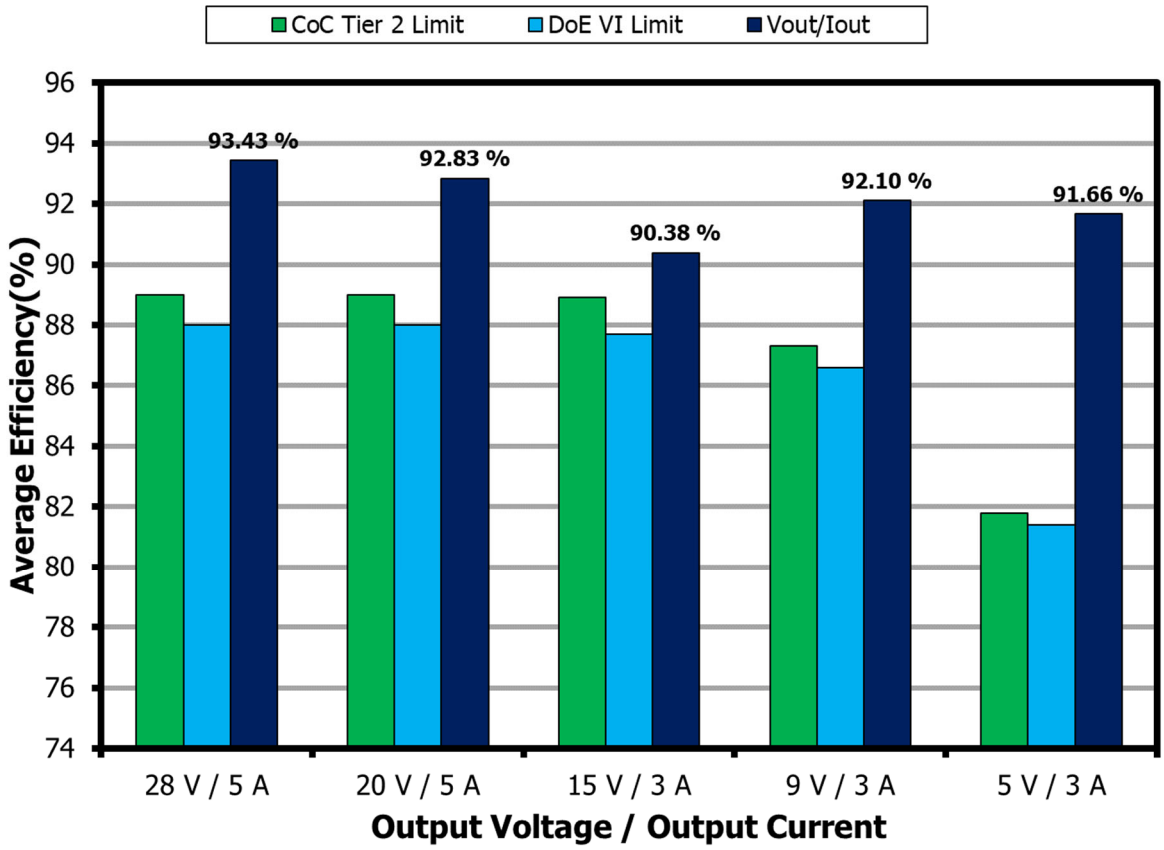


Figure 24 – Average Efficiency at 115 VAC, 60 Hz.

15.2.3.2 10% Efficiency Chart at 115 VAC

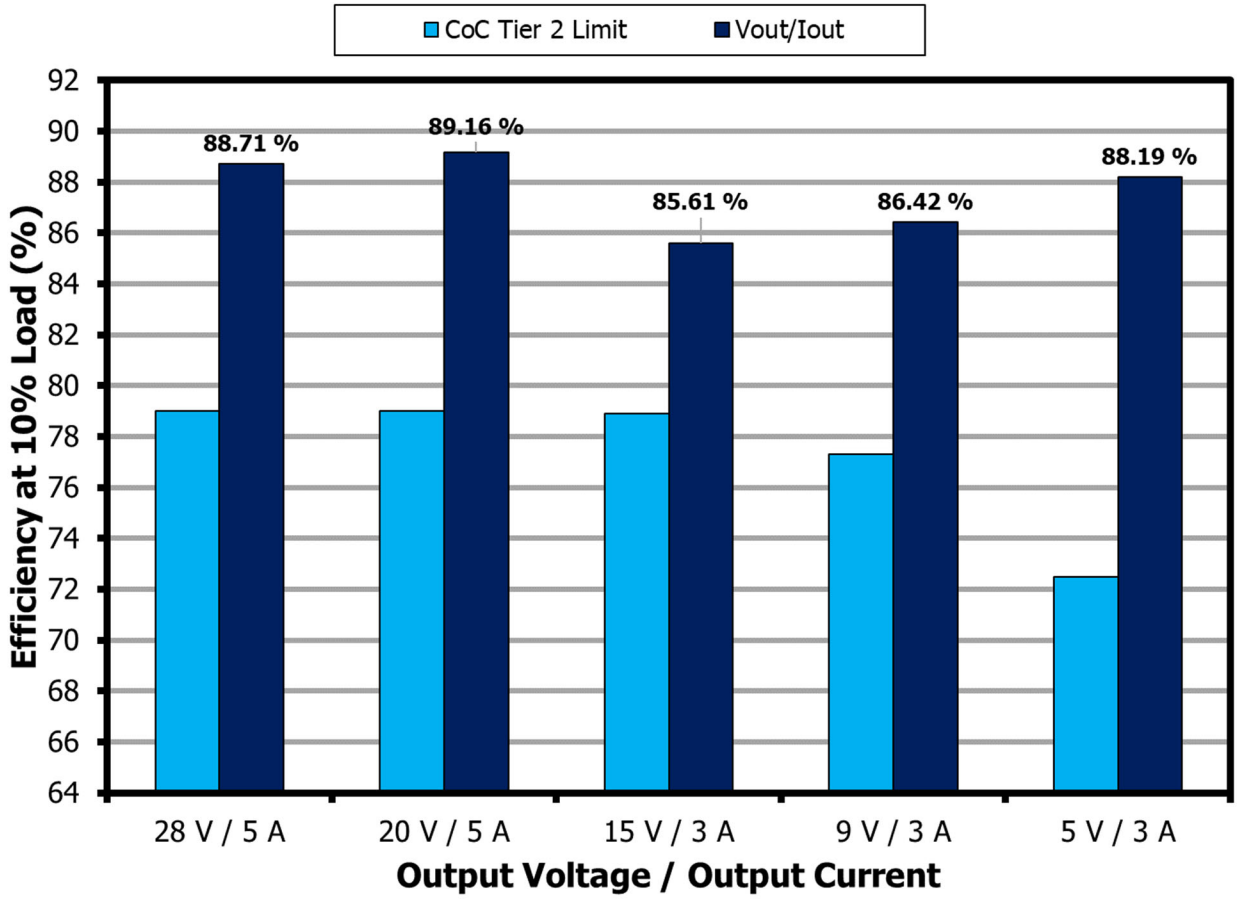


Figure 25 – Efficiency at 10% load, 115 VAC, 60 Hz.

15.2.3.3 Output: 5 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	15.15	91.97	**91.66**
75	11.33	92.11	
50	7.52	91.84	
25	3.75	90.71	
10	1.50	88.19	

15.2.3.4 Output: 9 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	26.90	92.65	**92.10**
75	20.14	92.66	
50	13.40	92.44	
25	6.69	90.65	
10	2.67	86.42	

15.2.3.5 Output: 15 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	44.94	92.98	**92.30**
75	33.74	92.91	
50	22.51	92.52	
25	11.26	90.81	
10	4.51	85.61	

15.2.3.6 Output: 20 V / 5 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	100.78	93.50	**92.83**
75	75.68	93.45	
50	50.48	93.24	
25	25.25	91.14	
10	10.11	89.16	

15.2.3.7 Output: 28 V / 5 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	142.10	93.89	**93.43**
75	106.67	93.79	
50	71.16	93.51	
25	35.59	92.52	
10	14.26	88.71	

15.2.4 Average and 10% Load Efficiency at 230 VAC

15.2.4.1 Average Efficiency Chart at 230 VAC

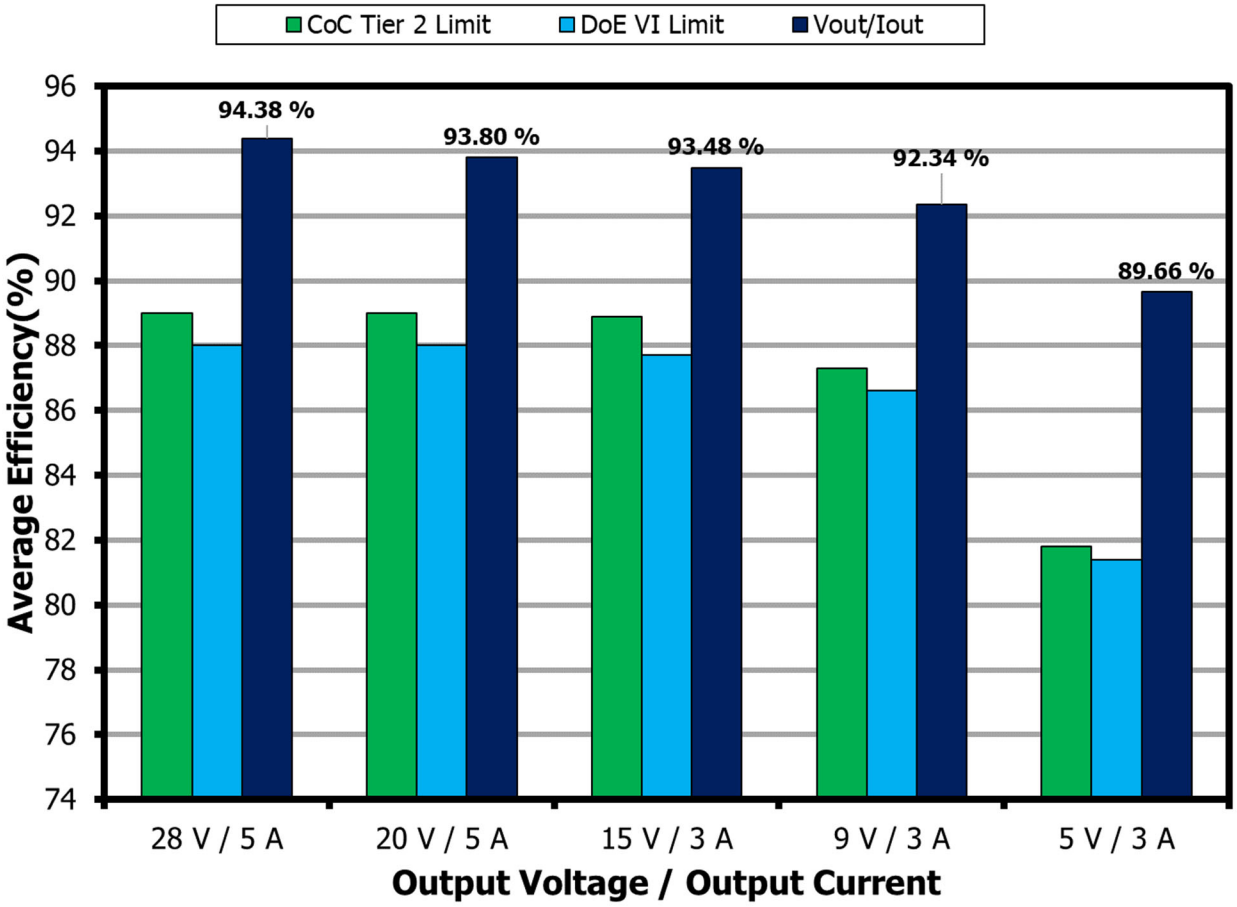


Figure 26 – Average Efficiency at 230 VAC, 50 Hz.

15.2.4.2 10% Efficiency Chart at 230 VAC

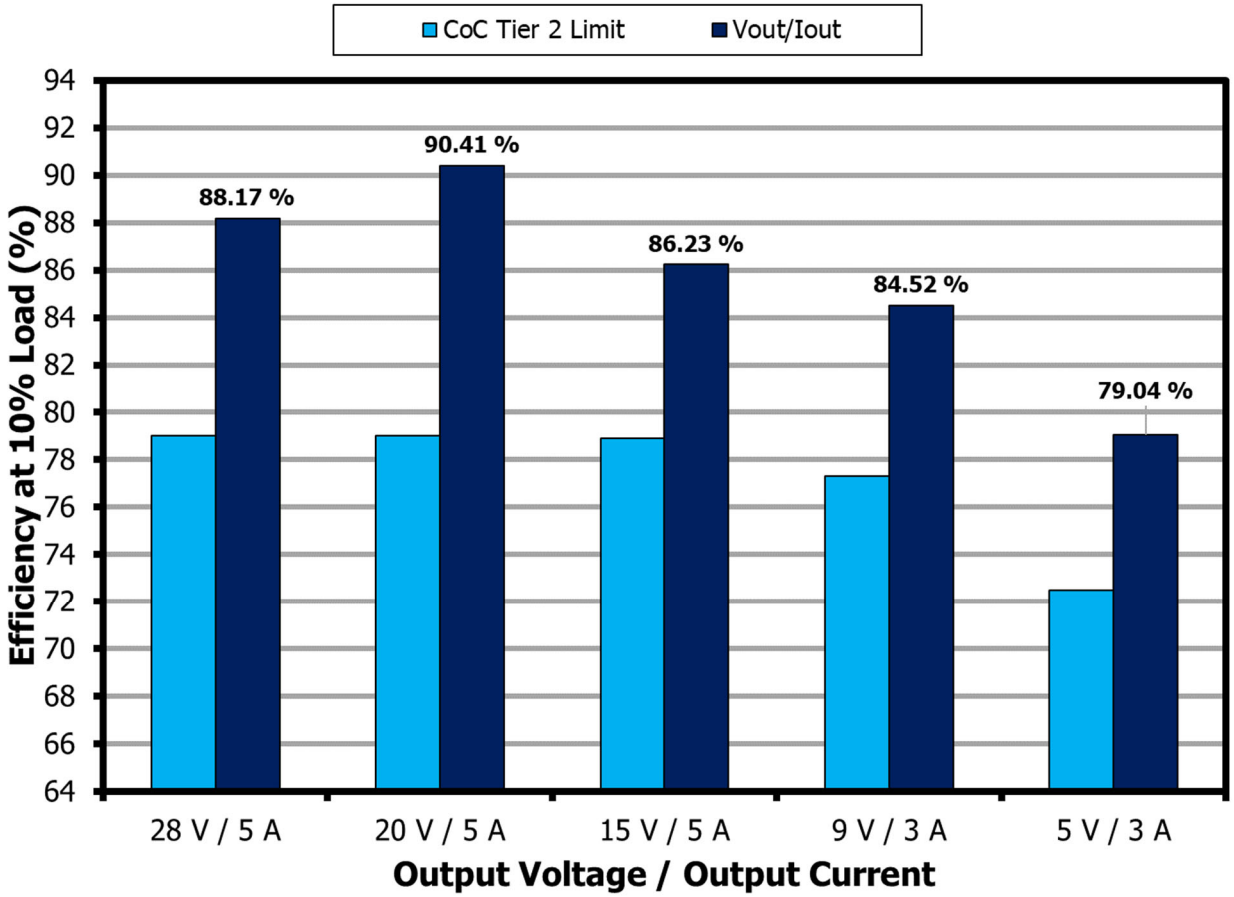


Figure 27 – Efficiency at 10 % load, 230 VAC, 50 Hz.

15.2.4.3 Output: 5 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	15.18	91.39	**89.66**
75	11.34	90.88	
50	7.53	89.79	
25	3.76	86.57	
10	1.49	79.04	

15.2.4.4 Output: 9 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	26.93	93.46	**92.34**
75	20.17	93.28	
50	13.41	92.55	
25	6.69	90.08	
10	2.68	84.52	

15.2.4.5 Output: 15 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	45.00	94.32	**93.48**
75	33.77	94.23	
50	22.51	93.76	
25	11.26	91.61	
10	4.51	86.23	

15.2.4.6 Output: 20 V / 5 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	100.74	94.63	**93.80**
75	75.64	94.47	
50	50.48	94.02	
25	25.24	92.06	
10	10.11	90.41	

15.2.4.7 Output: 28 V / 5 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	142.05	95.07	**94.38**
75	106.65	94.90	
50	71.15	94.43	
25	35.59	93.13	
10	14.25	88.17	

15.3 *Electrical Test Data (On Board)*

	Input		Input Measurement					Output 1 Measurement				
	VAC (RMS)	Freq (Hz)	V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	PF	% THD	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	%V Reg	Efficiency (%)
28 V / 5 A	90	60	89.78	1719.00	152.96	0.99	11.48	28.43	5001.37	142.18	1.53	92.95
	115	60	114.86	1328.00	151.51	0.99	8.20	28.43	5001.74	142.18	1.52	93.84
	132	60	131.85	1155.20	150.96	0.99	7.92	28.43	5001.37	142.18	1.53	94.18
	200	50	199.87	757.50	149.88	0.99	11.85	28.43	5001.74	142.22	1.55	94.89
	230	50	229.89	660.00	149.64	0.99	13.85	28.43	5000.99	142.19	1.55	95.02
	265	50	264.89	594.10	149.42	0.95	20.64	28.44	5000.99	142.21	1.56	95.18
	Input		**Input Measurement**					**Output 1 Measurement**				
	VAC (RMS)	Freq (Hz)	V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	PF	% THD	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	%V Reg	Efficiency (%)
20 V / 5 A	90	60	89.86	1224.00	108.82	0.99	11.70	20.19	5001.37	100.97	0.95	92.79
	115	60	114.92	952.50	108.02	0.99	11.77	20.19	5000.99	100.96	0.94	93.46
	132	60	131.91	830.50	107.70	0.98	12.12	20.19	5001.37	100.97	0.94	93.75
	200	50	199.90	541.50	106.96	0.99	10.61	20.19	5001.37	100.99	0.96	94.42
	230	50	229.92	473.20	106.84	0.98	13.25	20.19	5001.74	100.97	0.94	94.51
	265	50	264.92	428.80	106.59	0.94	19.67	20.19	5001.37	100.96	0.93	94.72
	Input		**Input Measurement**					**Output 1 Measurement**				
	VAC (RMS)	Freq (Hz)	V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	PF	% THD	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	%V Reg	Efficiency (%)
15 V / 3 A	90	60	89.93	1076.00	48.78	0.50	144.08	14.99	3000.90	44.99	-0.06	92.22
	115	60	114.98	923.00	48.40	0.46	174.52	15.01	3000.52	45.03	0.06	93.05
	132	60	131.95	862.60	48.28	0.42	194.07	15.02	3000.90	45.06	0.11	93.34
	200	50	199.94	684.00	47.84	0.35	242.25	15.02	3000.90	45.08	0.15	94.23
	230	50	229.94	624.90	47.83	0.33	254.77	15.02	3000.90	45.09	0.17	94.27
	265	50	264.94	540.00	47.79	0.33	250.49	15.03	3000.90	45.09	0.18	94.36
	Input		**Input Measurement**					**Output 1 Measurement**				
	VAC (RMS)	Freq (Hz)	V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	PF	% THD	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	%V Reg	Efficiency (%)
9 V / 3 A	90	60	89.95	706.90	29.17	0.46	173.51	8.96	3000.52	26.89	-0.42	92.19
	115	60	114.99	641.60	29.04	0.39	211.97	8.97	3000.90	26.93	-0.30	92.73
	132	60	131.97	594.40	28.99	0.37	228.79	8.97	3000.90	26.93	-0.29	92.90
	200	50	199.94	426.20	28.83	0.34	246.79	8.98	3000.90	26.95	-0.22	93.48
	230	50	229.95	375.90	28.88	0.33	242.37	8.98	3000.52	26.96	-0.17	93.35
	265	50	264.95	332.60	28.97	0.33	232.86	8.99	3000.52	26.97	-0.13	93.09
	Input		**Input Measurement**					**Output 1 Measurement**				
	VAC (RMS)	Freq (Hz)	V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	PF	% THD	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	%V Reg	Efficiency (%)
5 V / 3 A	90	60	89.96	472.60	16.54	0.39	213.79	5.04	3000.15	15.13	0.83	91.45
	115	60	115.00	379.30	16.47	0.38	223.38	5.05	3000.90	15.15	0.98	91.99
	132	60	131.98	336.00	16.46	0.37	223.79	5.05	3000.52	15.16	1.04	92.10
	200	50	199.95	249.40	16.52	0.33	226.80	5.06	3000.52	15.17	1.15	91.86
	230	50	229.96	225.55	16.62	0.32	213.97	5.06	3000.52	15.18	1.21	91.36
	265	50	264.96	205.74	16.77	0.31	195.42	5.06	3000.52	15.19	1.26	90.58

15.4 *Efficiency Across Line (On Board)*

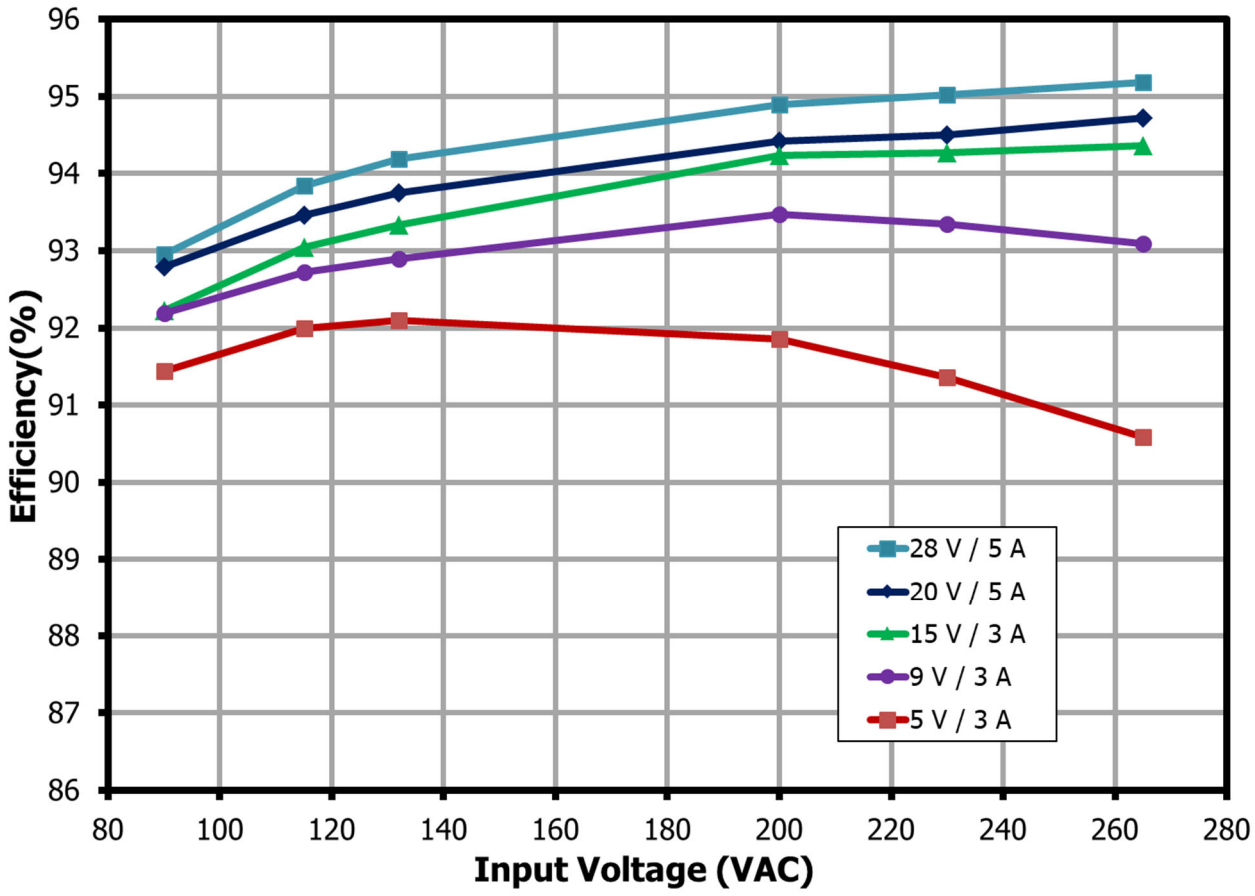


Figure 28 – Full Load Efficiency vs. Input Line for 5 V, 9 V, 15 V, 20 V and 28 V Output, Room Temperature.

15.5 *Power Factor*

PFC is disabled at 15 V, 9 V and 5 V Output.

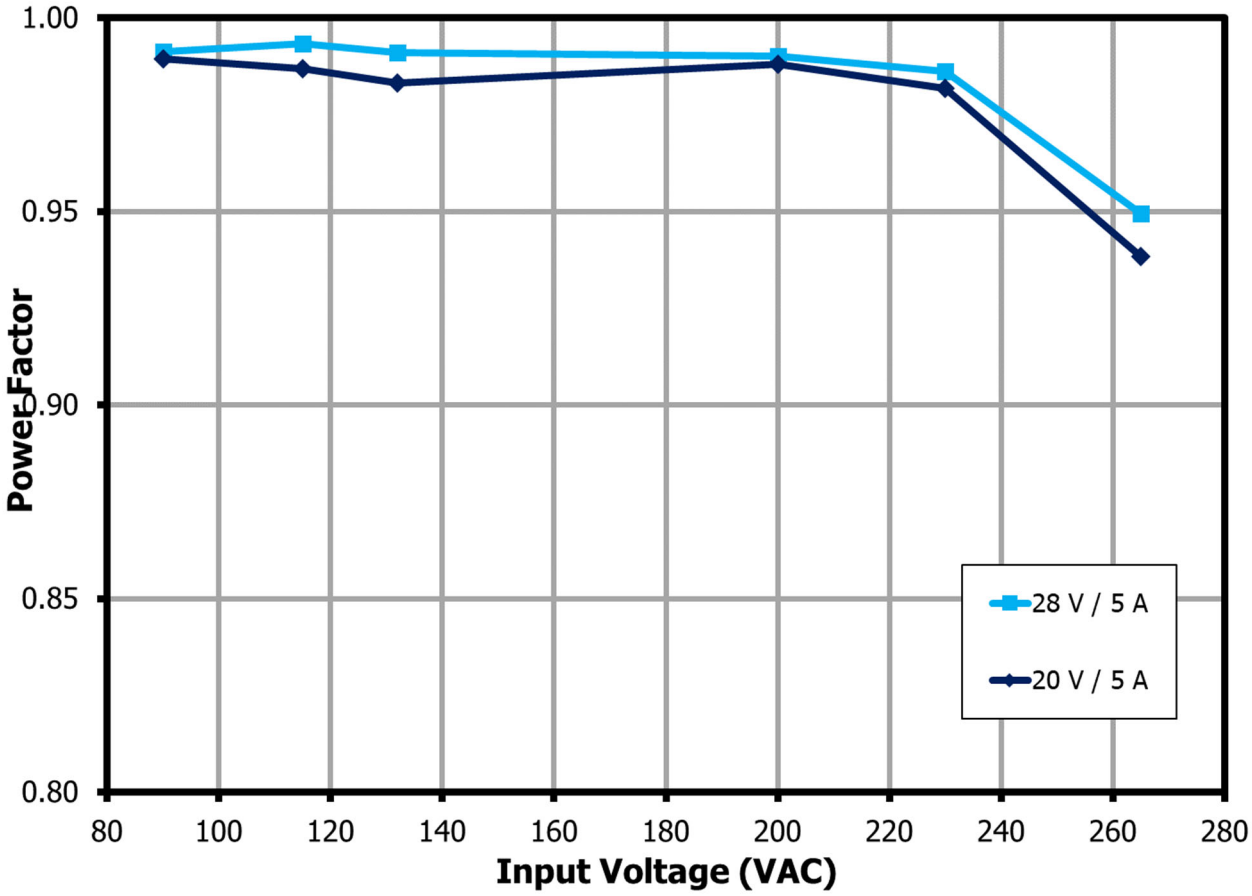


Figure 29 – Power Factor vs. Input Line Voltage, Room Temperature.

15.6 *A-THD*

PFC is disabled at 15 V, 9 V and 5 V Output.

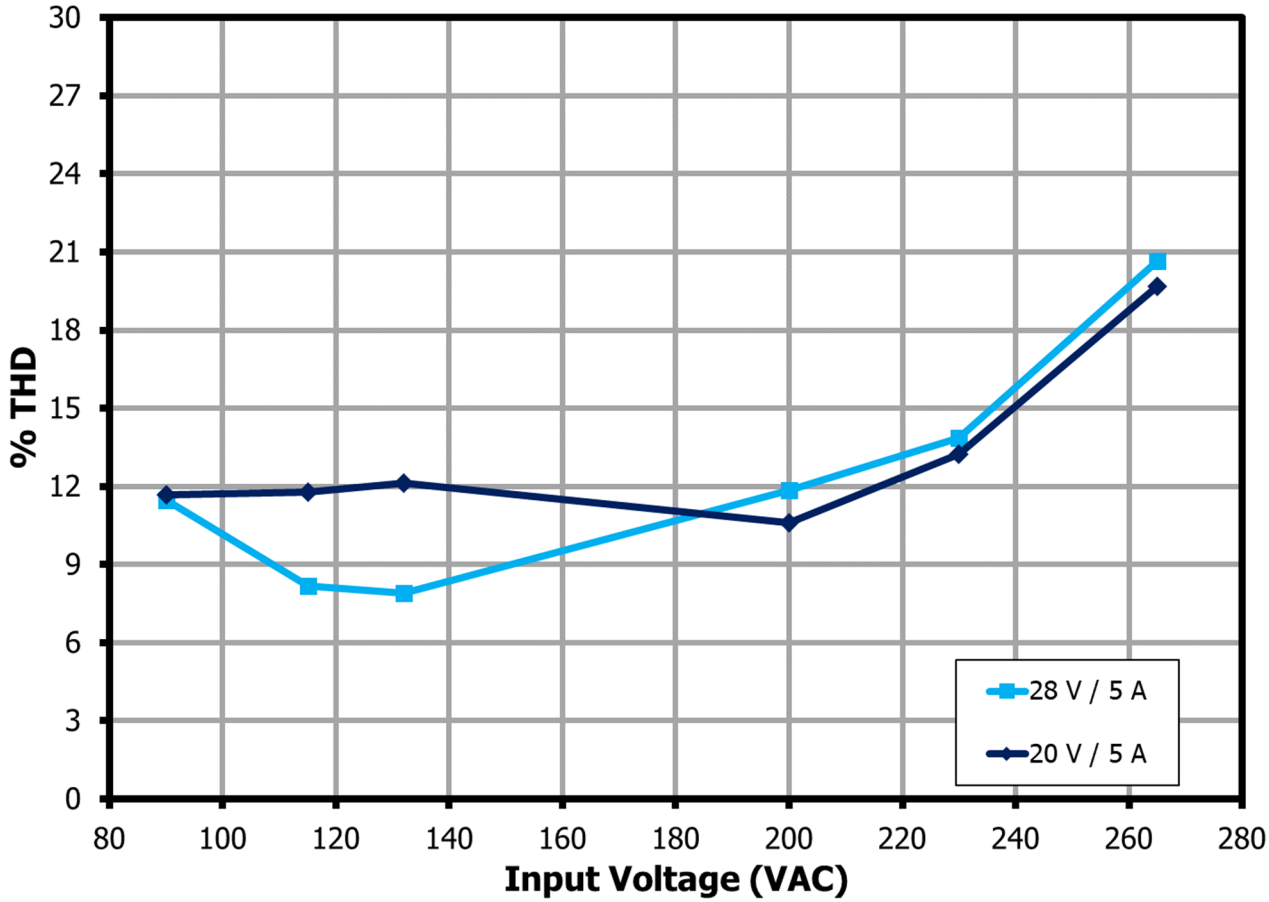


Figure 30 – THD (%) vs. Input Line Voltage, Room Temperature.

15.7 *Line Regulation (On Board)*

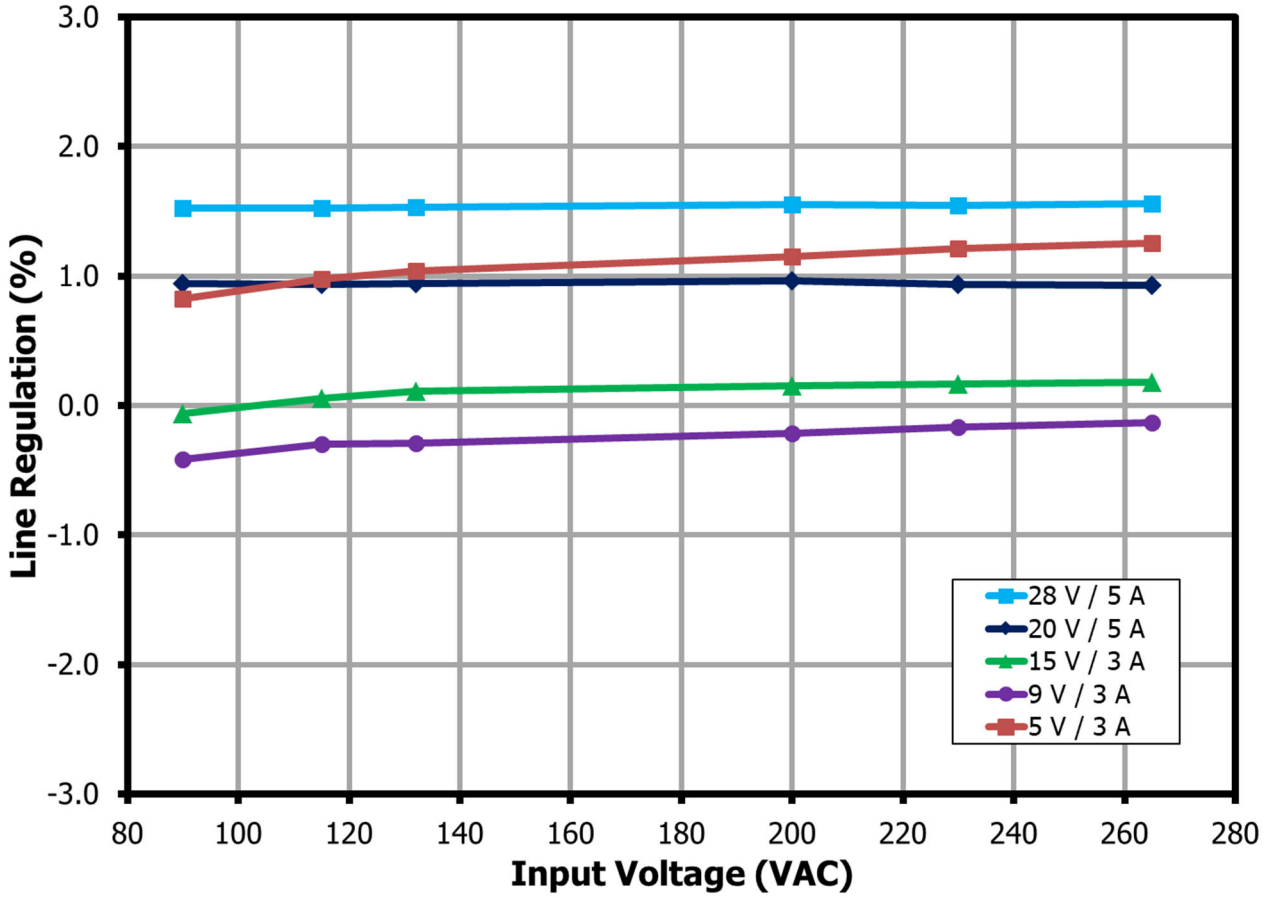


Figure 31 – Line Regulation (%) vs. Input Line Voltage, Room Temperature.

15.8 *Load Regulation (On Board)*

15.8.1 Output: 5 V / 3 A

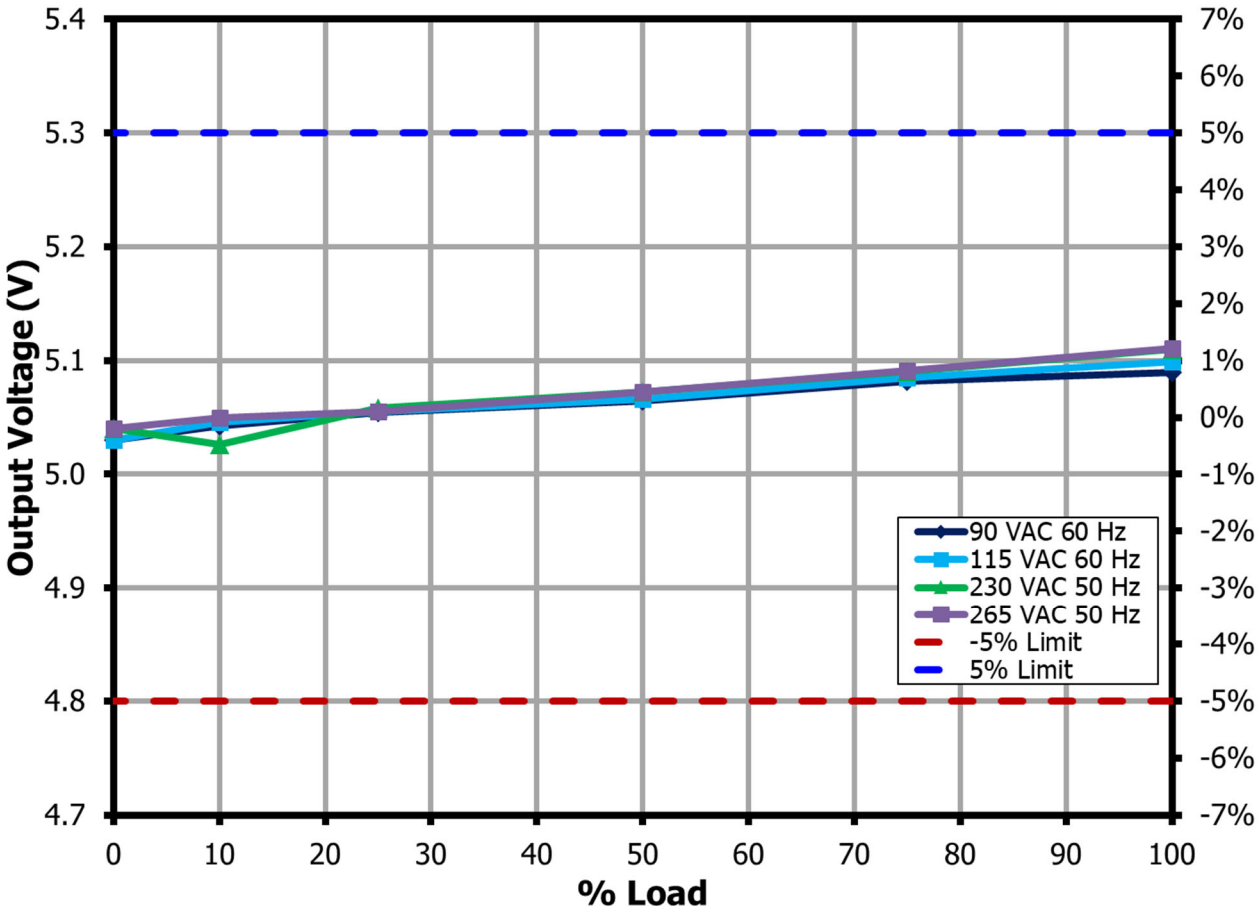


Figure 32 – Output Voltage vs. Output Load for 5 V Output, Room Temperature.

15.8.2 Output: 9 V / 3 A

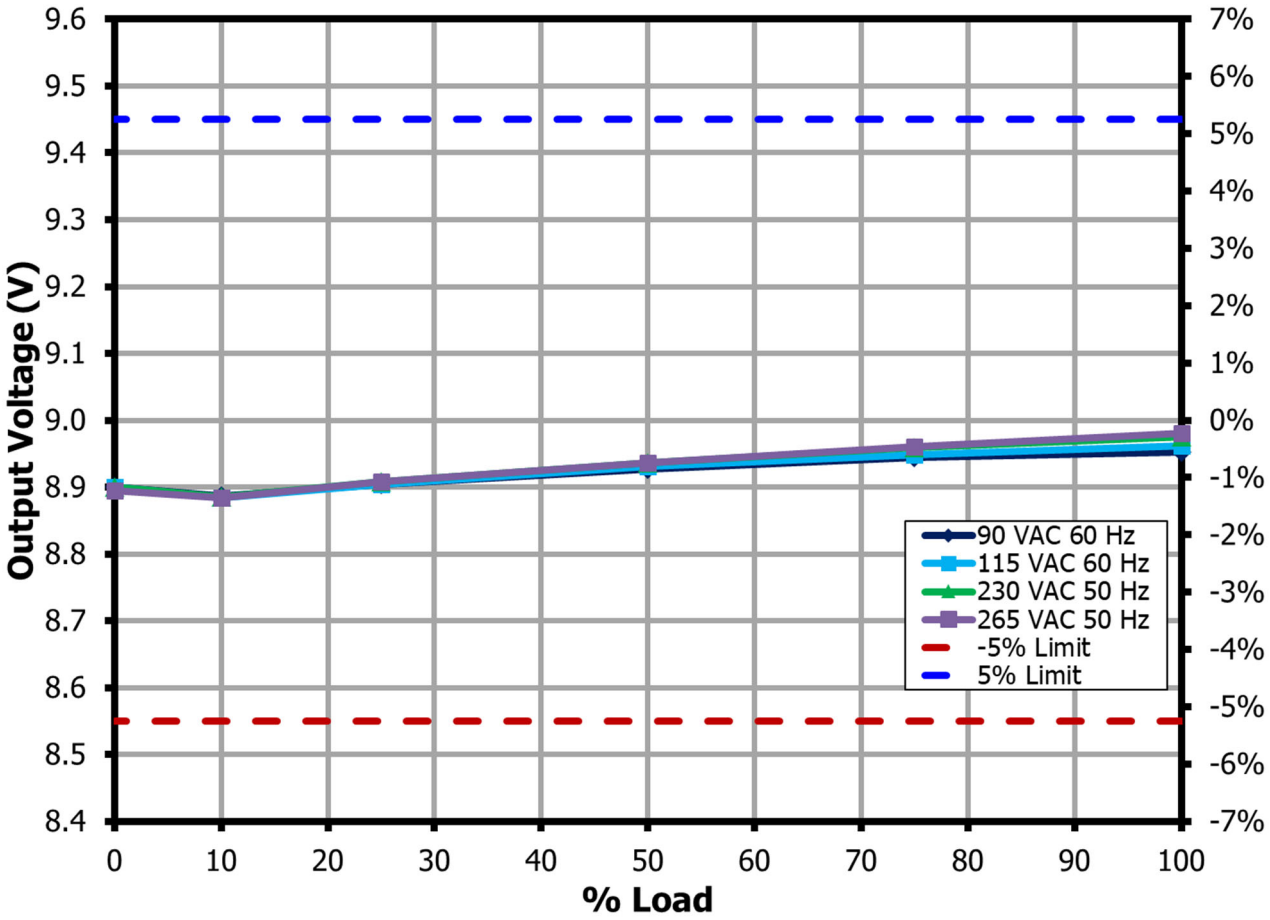


Figure 33 – Output Voltage vs. Output Load for 9 V Output, Room Temperature.

15.8.3 Output: 15 V / 3 A

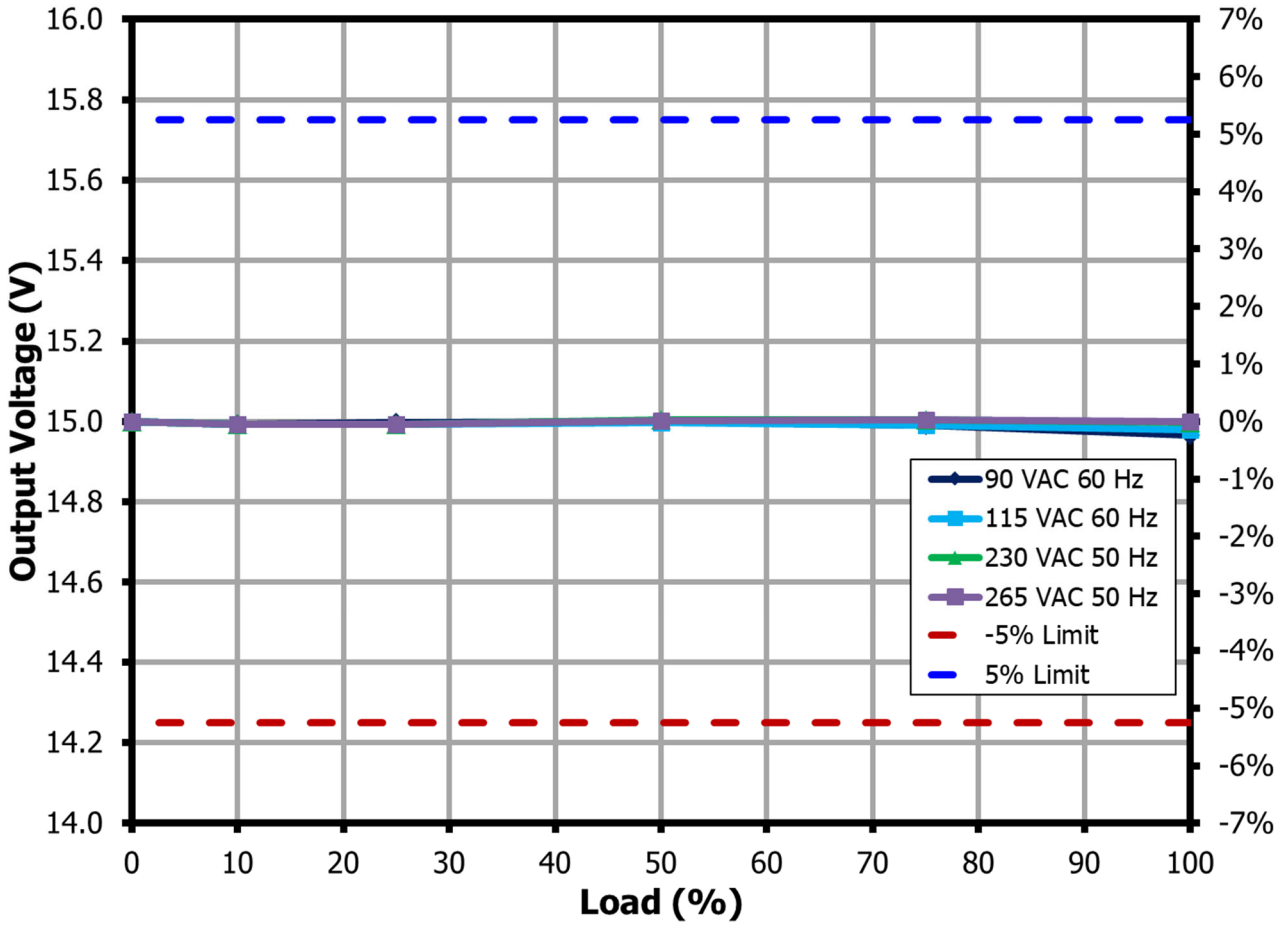


Figure 34 – Output Voltage vs. Output Load for 15 V Output, Room Temperature.

15.8.4 Output: 20 V / 5 A

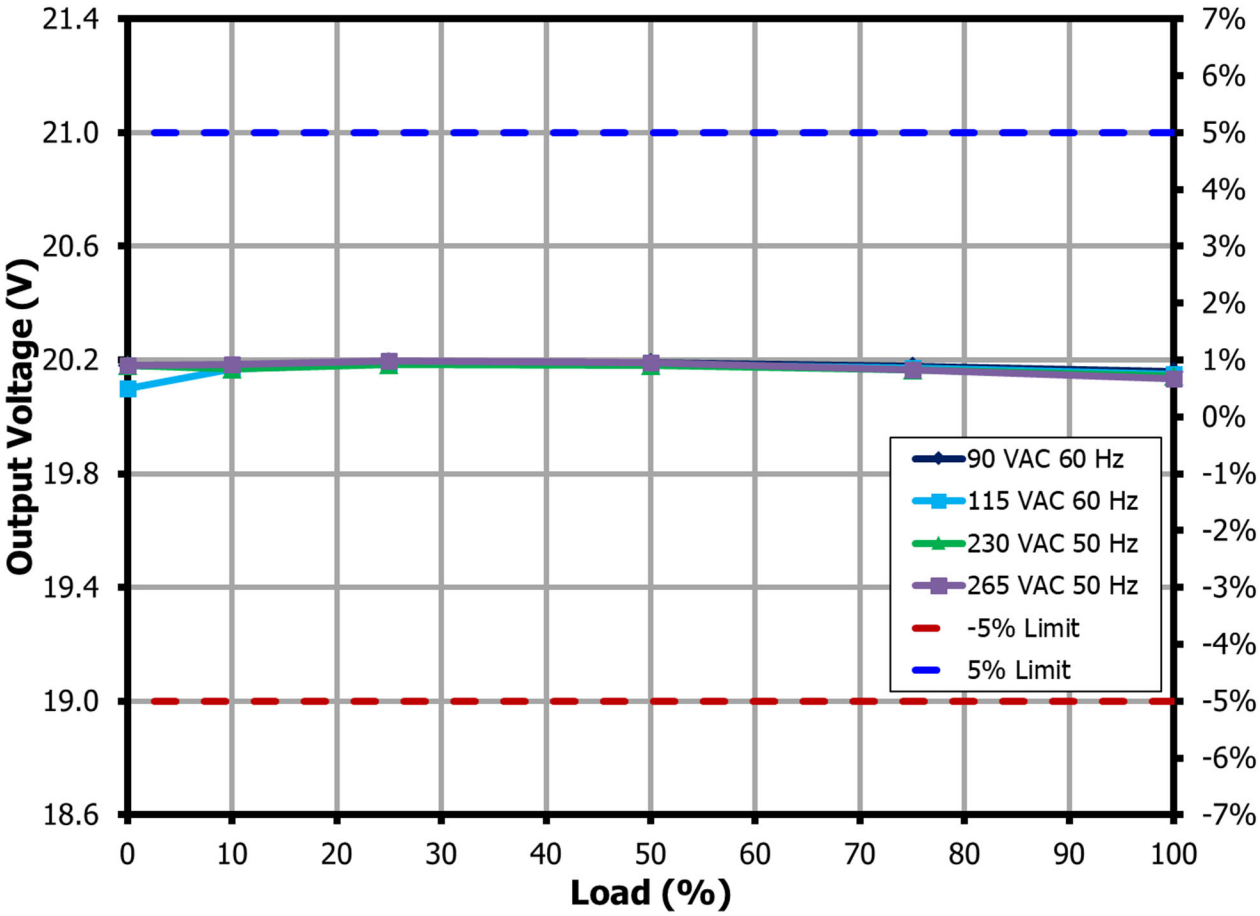


Figure 35 – Output Voltage vs. Output Load for 20 V Output, Room Temperature.

15.8.5 Output: 28 V / 5 A

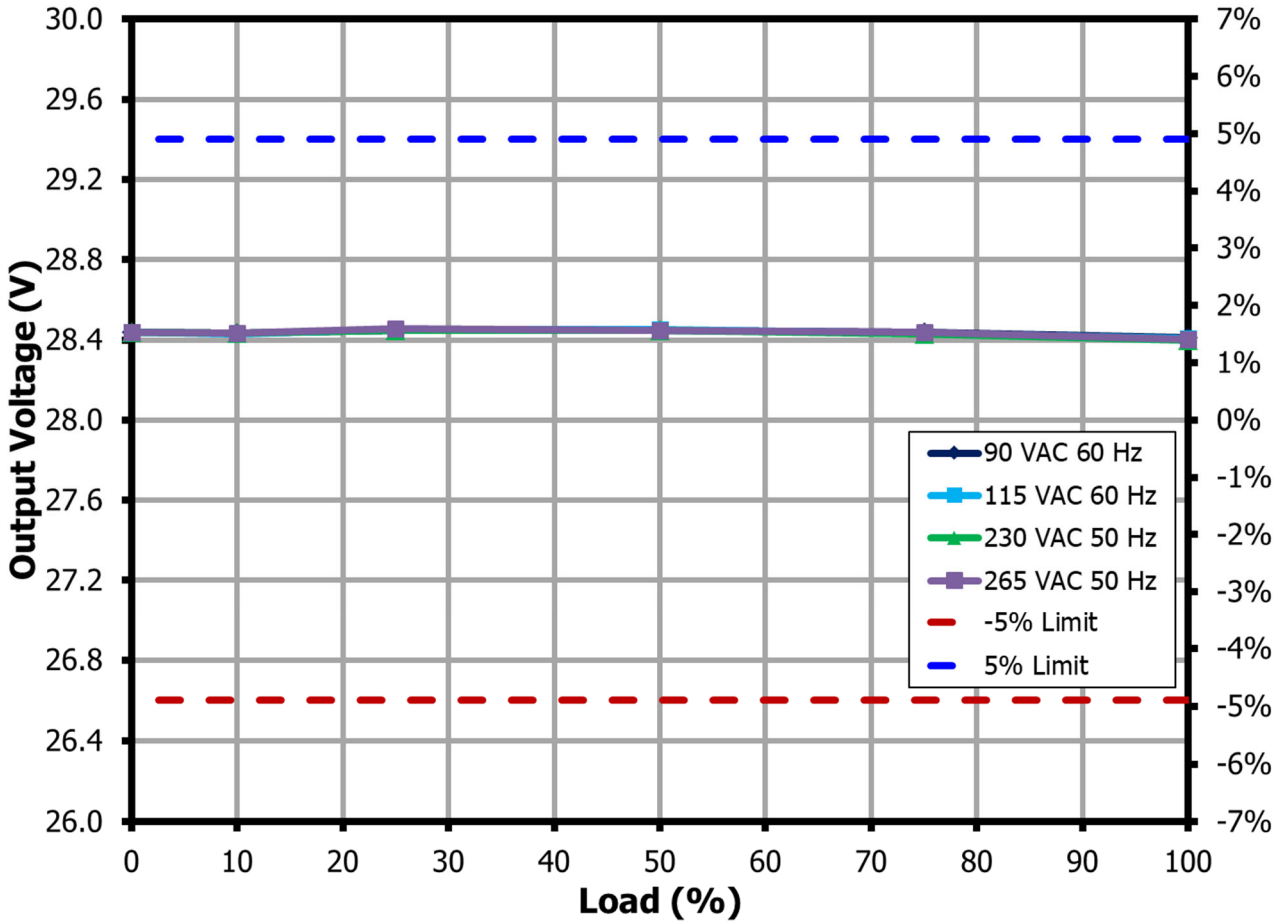


Figure 36 – Output Voltage vs. Output Load for 28 V Output, Room Temperature.

15.9 *Efficiency vs Load (On Board)*

15.9.1 Output: 5 V / 3 A

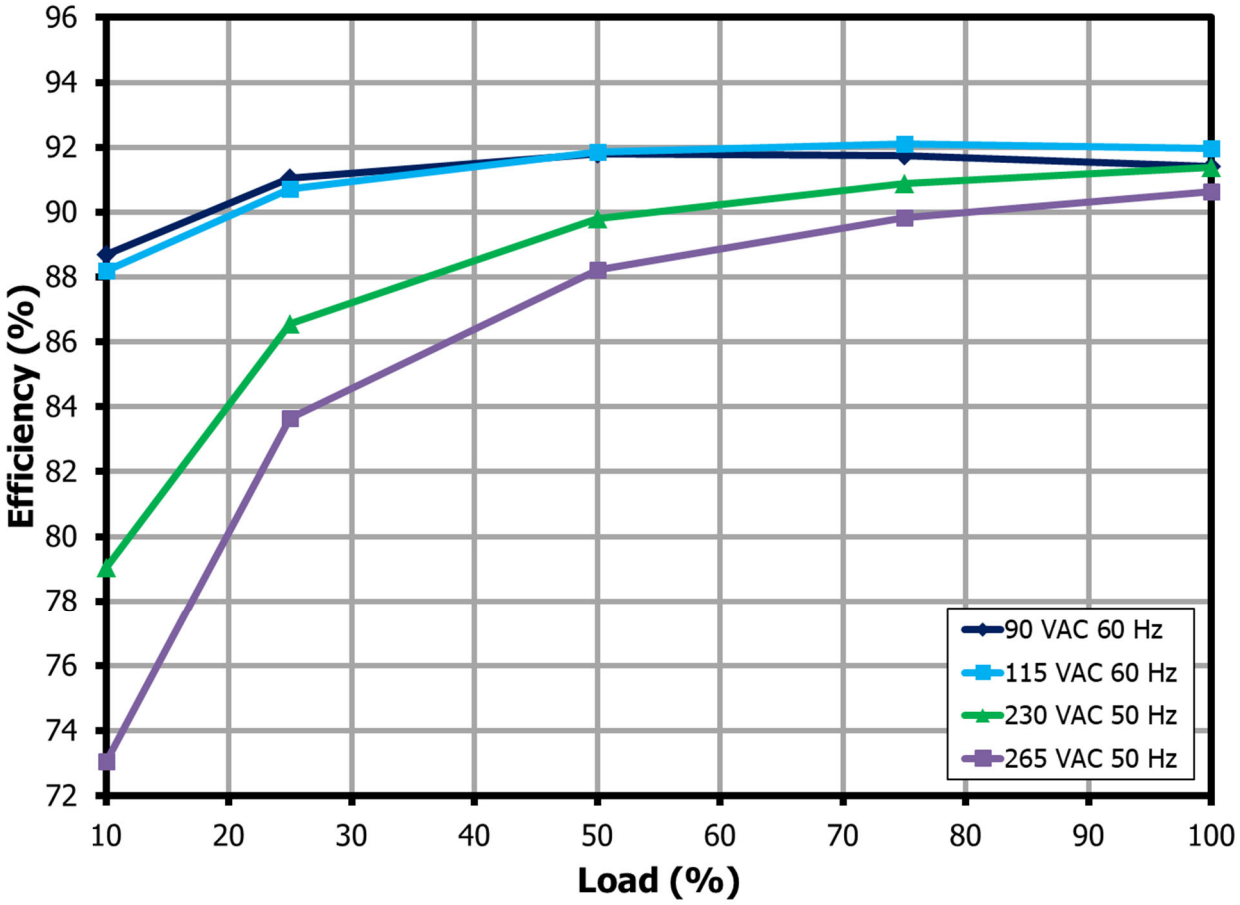


Figure 37 – Efficiency vs. Output Load for 5 V Output, Room Temperature.

15.9.2 Output: 9 V / 3 A

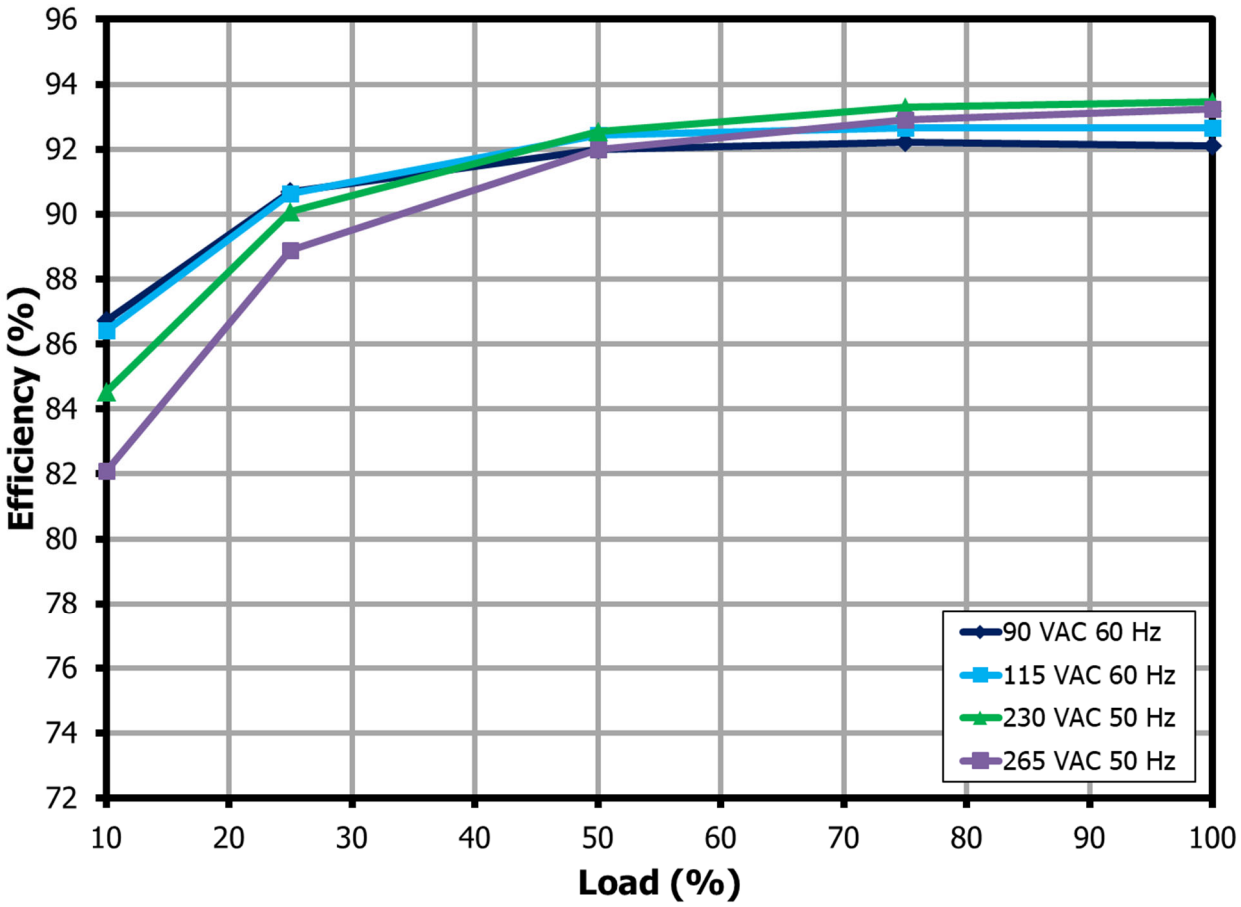


Figure 38 – Efficiency vs. Output Load for 9 V Output, Room Temperature.

15.9.3 Output: 15 V / 3 A

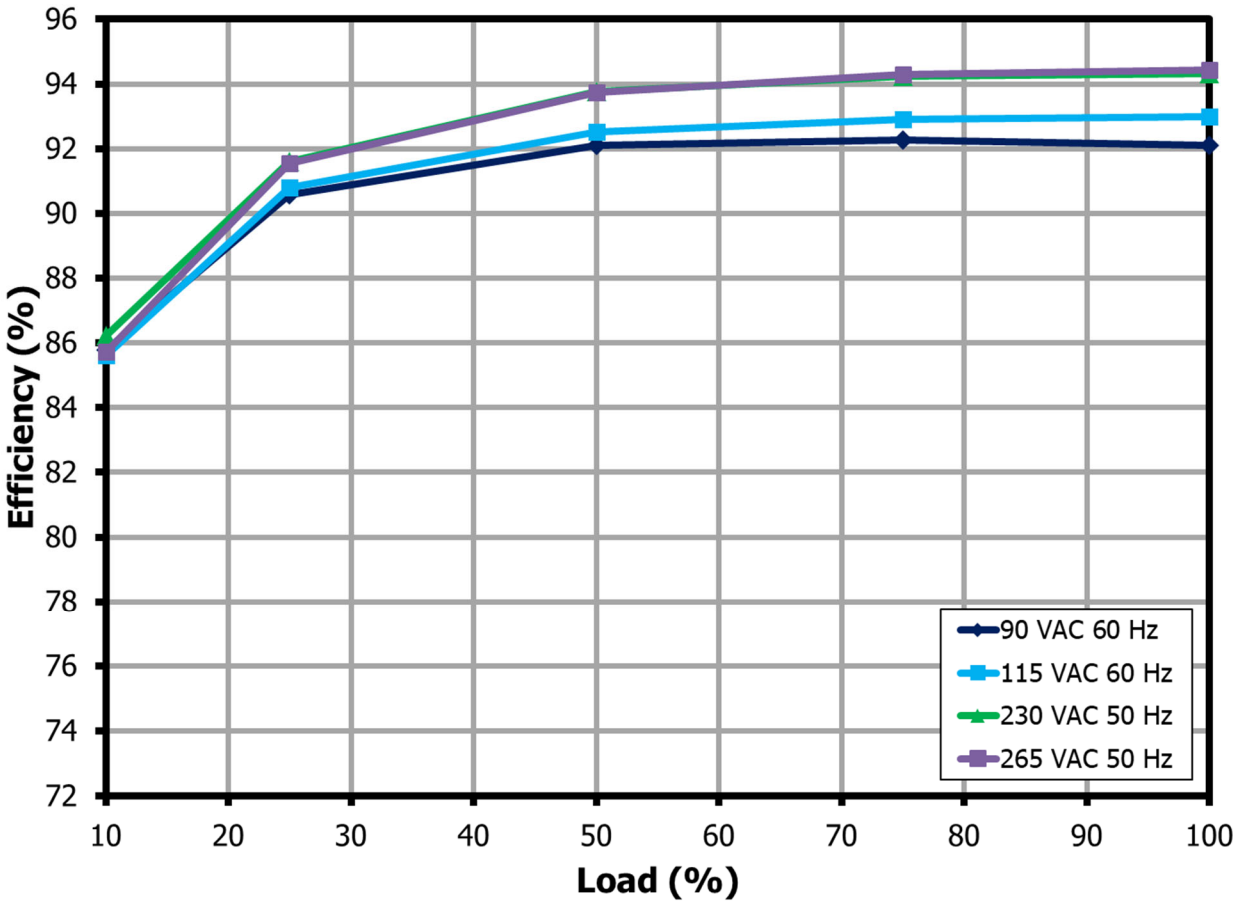


Figure 39 – Efficiency vs. Output Load for 15 V Output, Room Temperature.

15.9.4 Output: 20 V / 5 A

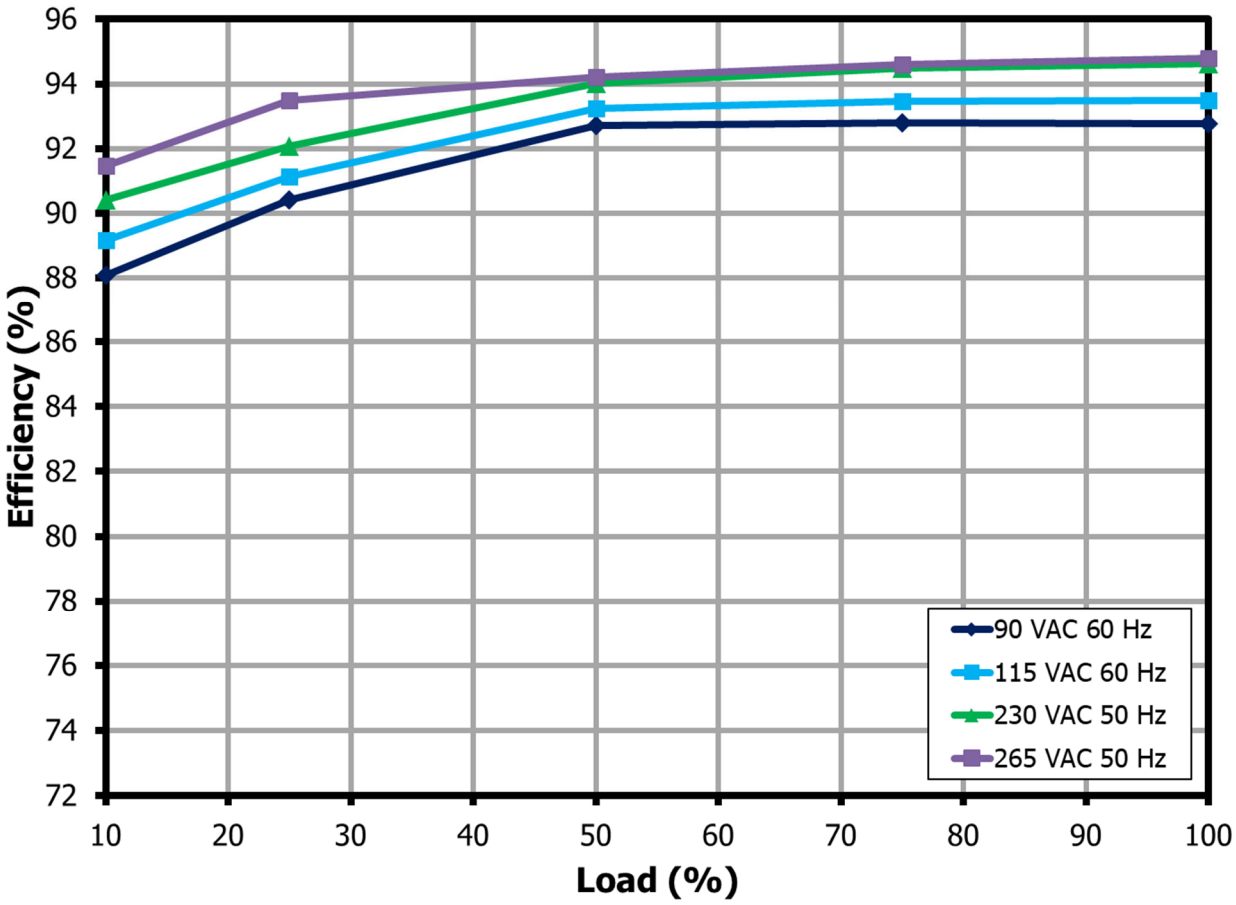


Figure 40 – Efficiency vs. Output Load for 20 V Output, Room Temperature.

15.9.5 Output: 28 V / 5 A

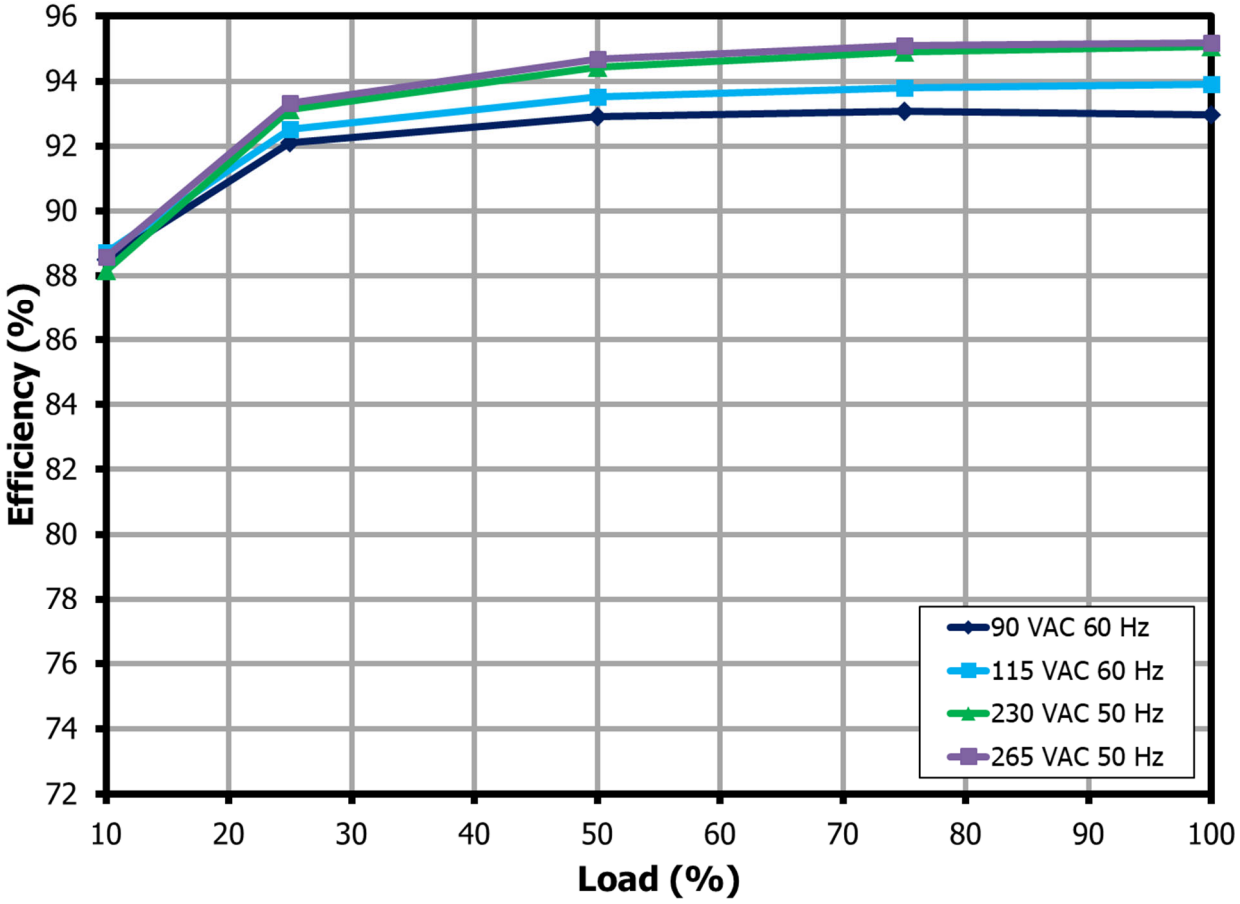


Figure 41 – Efficiency vs. Output Load for 28 V Output, Room Temperature.

16 Thermal Performance

Thermal performance is measured at ambient temperature. Thermal performance is tested inside an acrylic box with natural convection.

16.1 *Thermal Test Scan - Open Frame Unit*

DUT (open frame) is placed inside an acrylic housing to reduce the effect of airflow Component's case temperature is measured using an IR camera

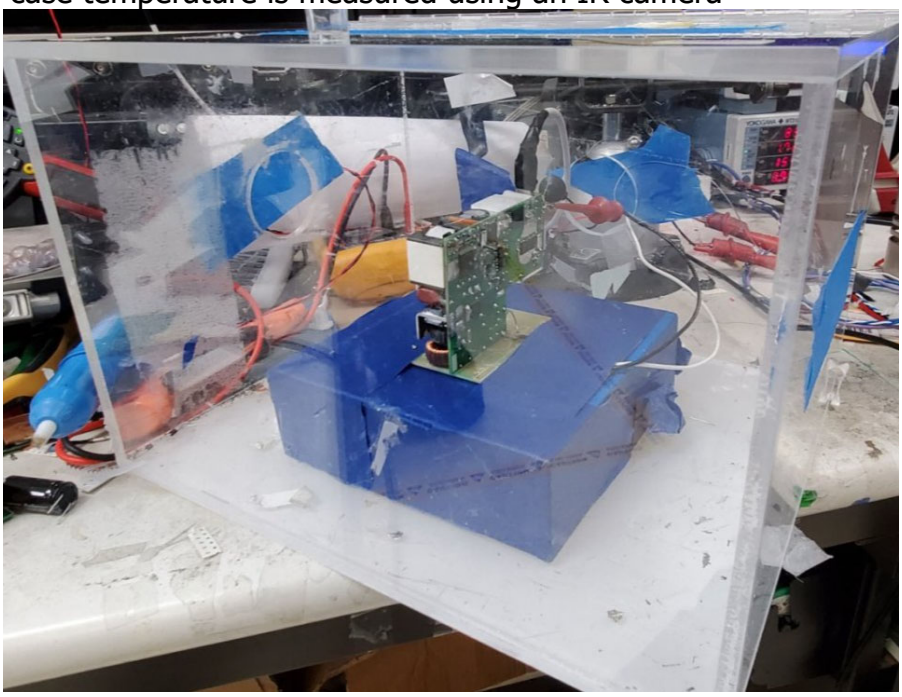


Figure 42 – Thermal Test Set-up.

Thermal Measurements (Open Frame)

Ref Des	Description	Temperature (°C)				
		90 VAC	100 VAC	115 VAC	230 VAC	265 VAC
U5	PFS5 (PFS5177F)	91.3	86.9	81.3	69.1	65.6
U3	Clamp Zero (CPZ1076M)	96.9	95.2	91.5	83	80.1
U4	INNO4-CZ (INN4077C)	97.8	96.5	92.9	87.1	84.7
Q4/Q12	SRFET (AONS62922)	94.7	95.6	92.5	88.9	87.3
BR1/BR2	Bridge Diode	97	91.8	84.7	65.5	61.7
D13	PFC Boost Diode	89.9	86.6	81.2	69.3	65.6
T8	PFC Boost Inductor	87.9	84.1	79	66.1	61.7
T7	Flyback Transformer	103.4	103.6	100.1	96.8	94.2
U6	PD Control IC	93	93	92.3	88.9	88.5
Amb	Ambient Temperature	28.5	28	28	28	28

16.2 *Thermal Test with Plastic Housing*

DUT with complete heat spreader and case assembly
Component's case temperature is measured through a thermocouple

16.2.1 Thermal Measurement at Room Ambient Temperature

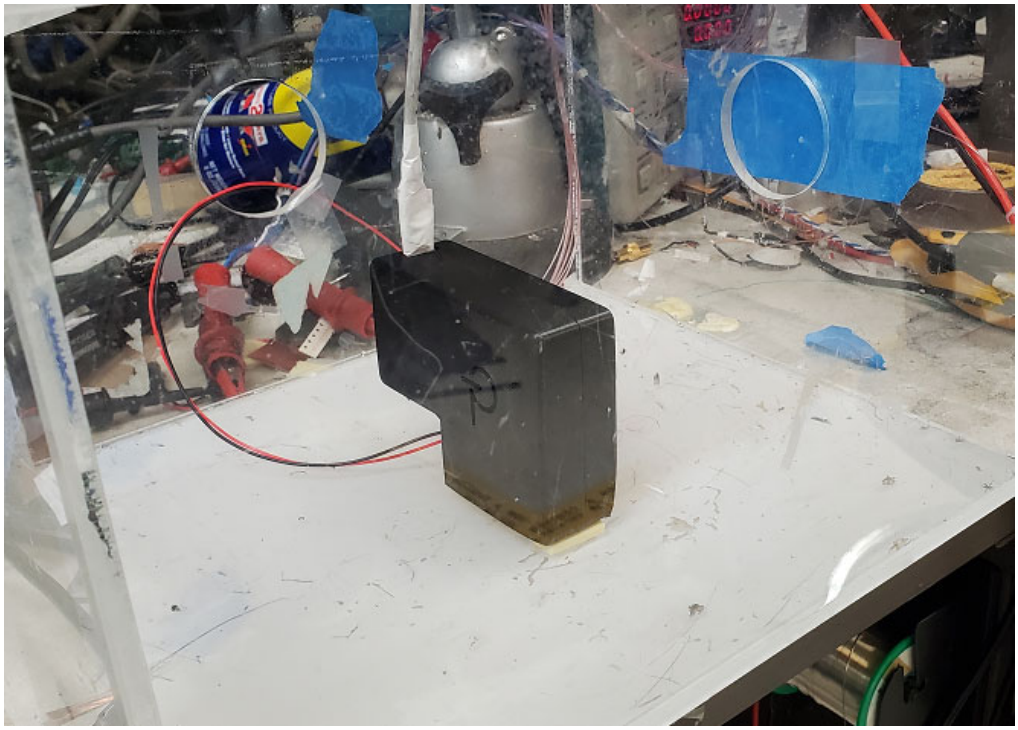


Figure 43 – Thermal Test Set-up.

Thermal Measurements (With Plastic Housing) at Room Ambient Temperature

Components		Temperature (°C)				
		90 VAC 60Hz	**100 VAC 60 Hz**	**115 VAC 60 Hz**	**230 VAC 50 Hz**	**265 VAC 50 Hz**
AMB	Ambient Temp	27.2	28.1	27.5	25.8	28.7
U6	PD Control IC	102.8	97.2	95.6	87	86.9
T8	Boost Inductor	101	95.4	89.4	74.2	72.1
T7	Flyback TRF	120.9	116	112	101.3	99.6
U5	HiperPFS-5	100.3	94.1	90.2	75.6	76.6
U3	ClampZero	101.3	94.8	91.2	78.9	76.7
U4	InnoSwitch4-CZ	101.8	95.6	91.1	79.3	77.1
D13	Boost Diode	113.3	105.7	100	85.1	84.8
BR1/BR2	Bridge Diode	109.8	98.8	95.8	74.9	71.8
Q4/Q12	SRFET	106.7	101.6	99.3	86.2	84.8

16.2.2 Thermal Measurement at 42 ºC Ambient Temperature

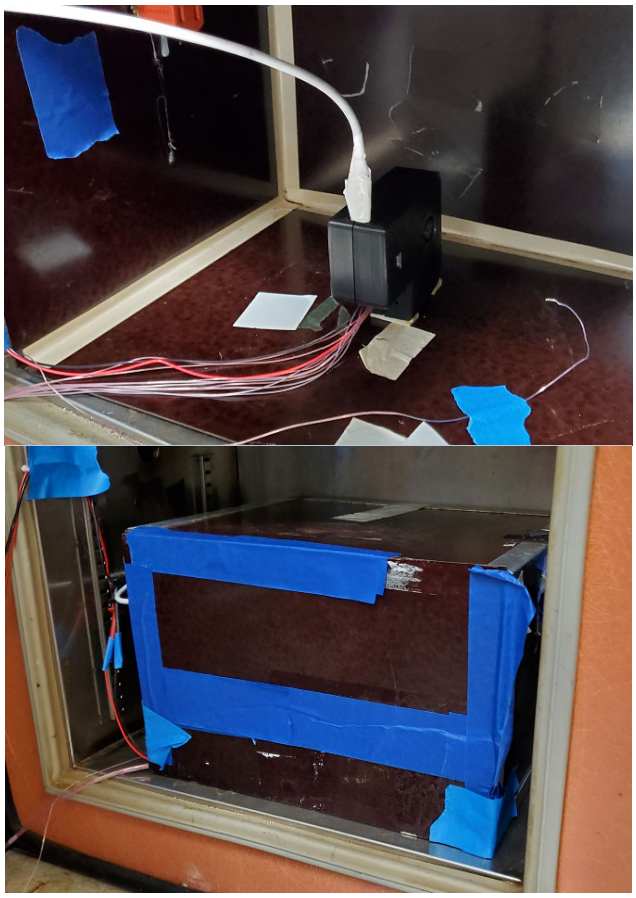


Figure 44 – Thermal Test Set-up.

Components		Temperature (°C)			
		90 VAC 60Hz	**115 VAC 60 Hz**	**230 VAC 50 Hz**	**265 VAC 50 Hz**
AMB	Ambient Temp	45.3	44.9	42.8	42.7
U6	PD Control IC	118.2	110	100.2	99
T8	Boost Inductor	113.8	100.4	84.4	82.7
T7	Flyback TRF	137.3	126.3	113.4	111.7
U5	HiperPFS-5	112.3	100.1	86.3	84.5
U3	ClampZero	114.3	102	89.8	87.1
U4	InnoSwitch4-CZ	114.7	102.4	89.1	88.1
D13	Boost Diode	126.5	111.5	95.6	93.5
BR1/BR2	Bridge Diode	124	106.4	85.8	82.9
Q4/Q12	SRFET	118.8	107.8	94.8	93.7

17 Waveforms

Note: Measurements taken at room temperature

17.1 *Start-up Waveforms*

17.1.1 Output Voltage and Current

Note: Output voltages captured on the board at output connector

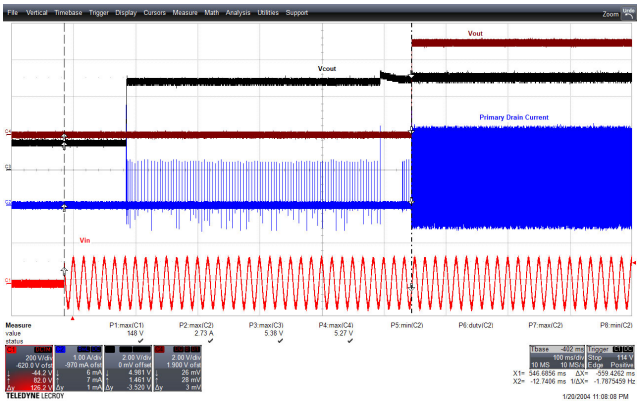


Figure 45 – Output Voltage at Start-up.
90 VAC, 5 V, 3 A Load.
C1: V_{IN}, 200 V / div.
C2: I_{DRAIN}, 1 A / div.
C3: V_{COUT}, 2 V / div.
C4: V_{OUT}, 2 V / div.
Time: 100 ms / div.

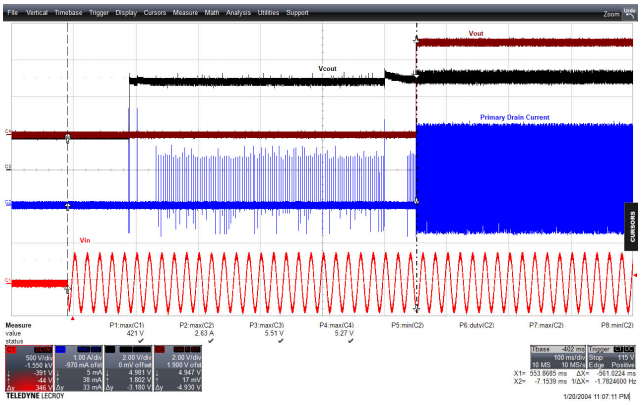


Figure 46 – Output Voltage at Start-up.
90 VAC, 5 V, 3 A Load.
C1: V_{IN}, 500 V / div.
C2: I_{DRAIN}, 1 A / div.
C3: V_{COUT}, 2 V / div.
C4: V_{OUT}, 2 V / div.
Time: 100 ms / div.

17.1.2 InnoSwitch4-CZ Drain Voltage and Current at Start-up

Figure 47 – InnoSwitch4-CZ Drain Voltage and Current.
90 VAC, 5 V, 3 A Load (191 V_{MAX}).
C1: V_{DRAIN}, 100 V / div.
C2: I_{DRAIN}, 1 A / div.
Time (Zoom): 19.4 µs / div.

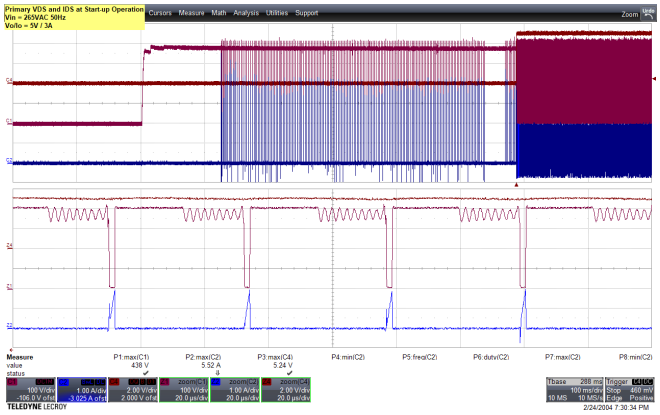


Figure 48 – InnoSwitch4-CZ Drain Voltage and Current.
265 VAC, 5 V, 3 A Load (438 V_{MAX}).
C1: V_{DRAIN}, 100 V / div.
C2: I_{DRAIN}, 0.5 A / div.
Time (Zoom): 13.6 µs / div.

17.1.3 Primary Clamp Drain Voltage and Current at Start-up

Figure 49 – Primary Clamp Drain Voltage and Current.
90 VAC, 5 V, 3 A Load (175 V_{MAX}).
C1: V_{DRAIN}, 50 V / div.
C2: I_{DRAIN}, 1 A / div.
Time (Zoom): 20 µs / div.

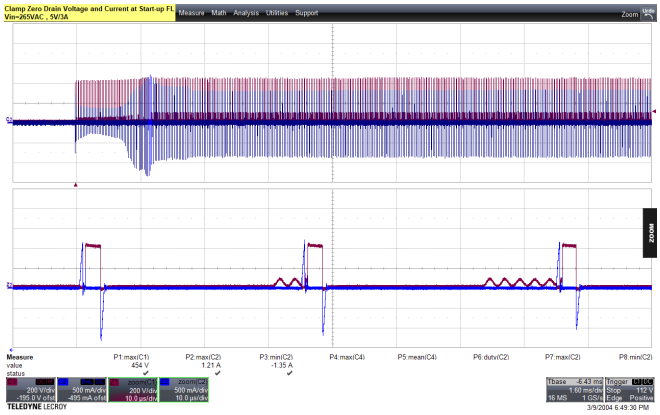


Figure 50 – Primary Clamp Drain Voltage and Current.
265 VAC, 5 V, 3 A Load (454 V_{MAX}).
C1: V_{DRAIN}, 200 V / div.
C2: I_{DRAIN}, 500 mA / div.
Time (Zoom): 20 µs / div.

17.1.4 HiperPFS-5 Drain Voltage and Current at Start-up

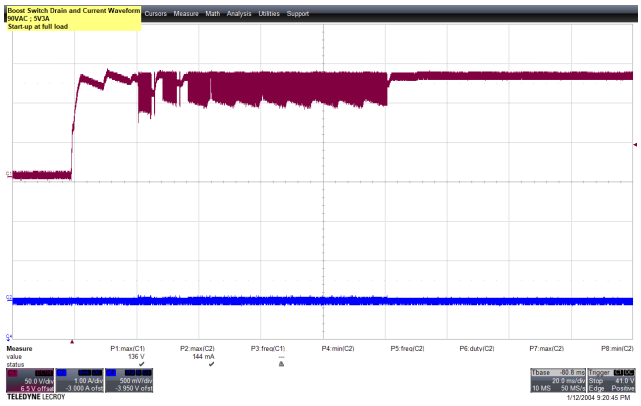


Figure 51 – HiperPFS-5 Drain Voltage and Current.
90 VAC, 5 V, 3 A Load (136 V_{MAX}).
C1: V_{DRAIN}, 50 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 20 ms / div.

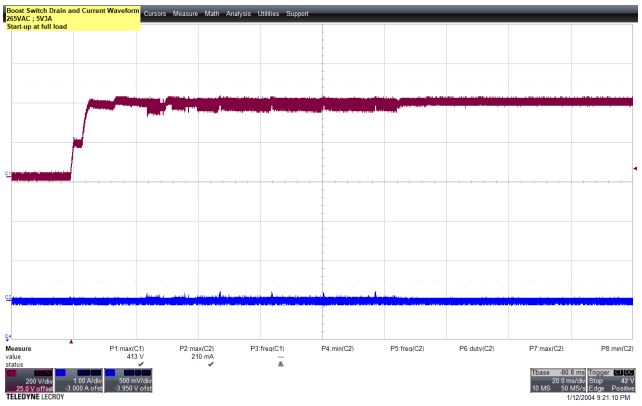


Figure 52 – HiperPFS-5 Drain Voltage and Current.
265 VAC, 5 V, 3 A Load (413 V_{MAX}).
C1: V_{DRAIN}, 200 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 20 ms / div.

17.2 *Load Transient Response*

Note: Output voltage waveforms are captured at the end of the PC board. Load setting is as follows: 10% - 100% load current step, 25 Hz, 50% duty cycle, slew rate of 150 mA / µs.

17.2.1 Output: 5 V / 3 A

Figure 53 – Transient Response.
90 VAC, 5 V, 10% – 100% Load Step.
V_{MIN}: 4.61 V, V_{MAX}: 5.13 V.
C1: V_{OUT}, 0.5 V / div.
C2: I_{LOAD}, 2 A / div.
Time: 10 ms / div.

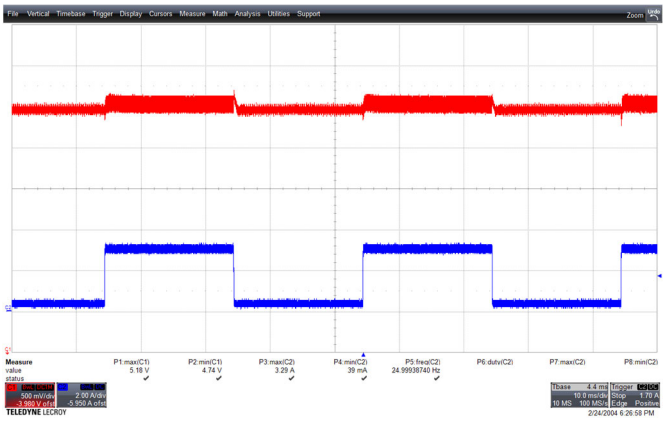


Figure 54 – Transient Response.
265 VAC, 5 V, 10% – 100% Load Step.
V_{MIN}: 4.74 V, V_{MAX}: 5.18 V.
C1: V_{OUT}, 0.5 V / div.
C2: I_{LOAD}, 2 A / div.
Time: 10 ms / div.

17.2.2 Output: 9 V / 3 A

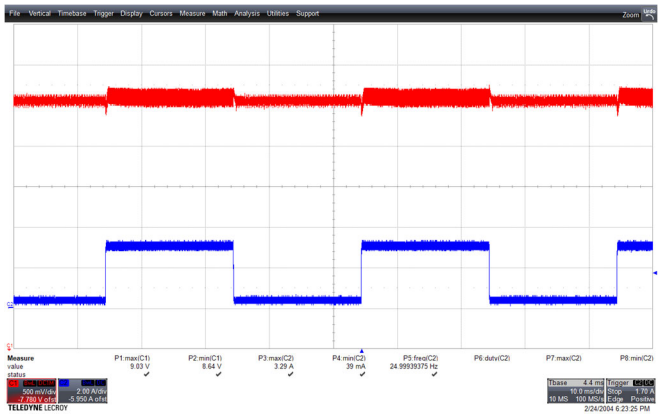


Figure 55 – Transient Response.
90 VAC, 9 V, 10% – 100% Load Step.
V_{MIN}: 8.64 V, V_{MAX}: 9.03 V.
C1: V_{OUT}, 0.5 V / div.
C2: I_{LOAD}, 2 A / div.
Time: 10 ms / div.

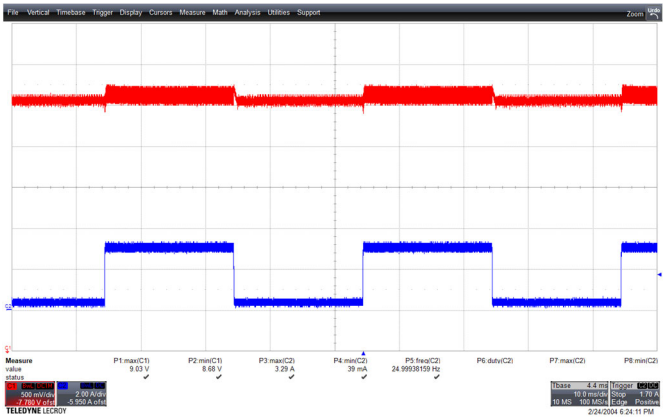


Figure 56 – Transient Response.
265 VAC, 9 V, 10% – 100% Load Step.
V_{MIN}: 8.68 V, V_{MAX}: 9.03 V.
C1: V_{OUT}, 0.5 V / div.
C2: I_{LOAD}, 2 A / div.
Time: 10 ms / div.

17.2.3 Output: 15 V / 3 A

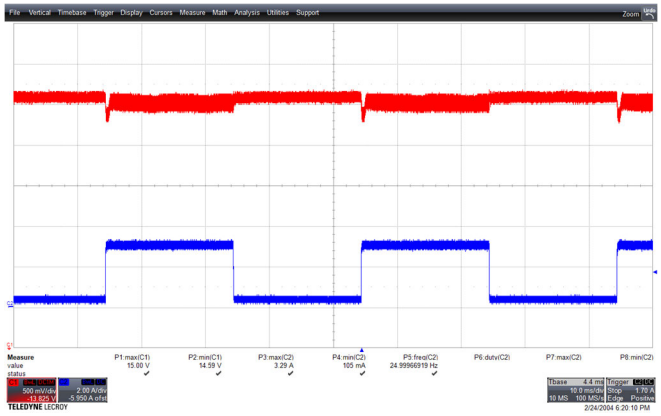


Figure 57 – Transient Response.
90 VAC, 15 V, 10% – 100% Load Step.
V_{MIN}: 14.59 V, V_{MAX}: 15 V.
C1: V_{OUT}, 0.5 V / div.
C2: I_{LOAD}, 2 A / div.
Time: 10 ms / div.

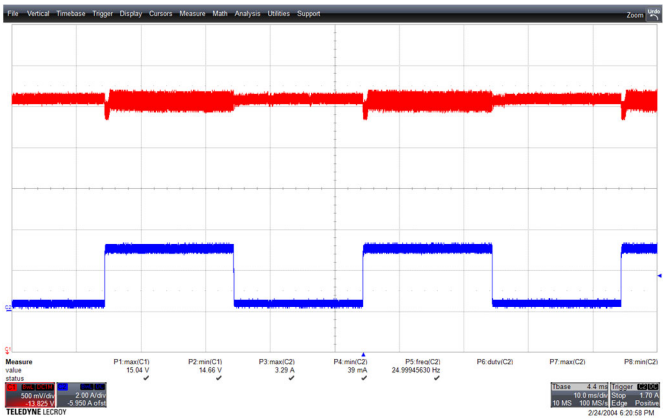


Figure 58 – Transient Response.
265 VAC, 15 V, 10% – 100% Load Step.
V_{MIN}: 14.66 V, V_{MAX}: 15.04 V.
C1: V_{OUT}, 0.5 V / div.
C2: I_{LOAD}, 2 A / div.
Time: 10 ms / div.

17.2.4 Output: 20 V / 5 A

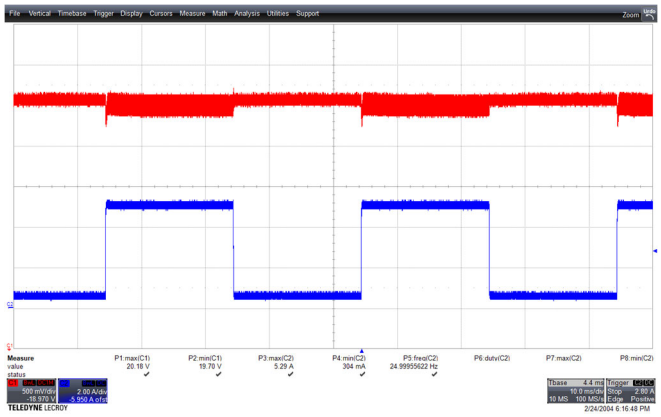


Figure 59 – Transient Response.
90 VAC, 20 V, 10% – 100% Load Step.
V_{MIN}: 19.7 V, V_{MAX}: 20.18 V.
C1: V_{OUT}, 0.5 V / div.
C2: I_{LOAD}, 2 A / div.
Time: 10 ms / div.

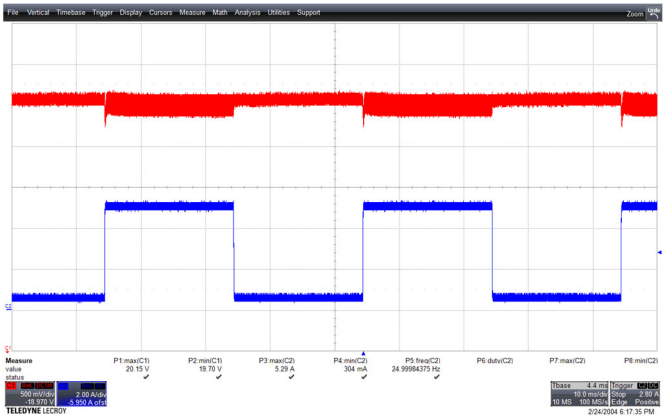


Figure 60 – Transient Response.
265 VAC, 20 V, 10% – 100% Load Step.
V_{MIN}: 19.70 V, V_{MAX}: 20.15 V.
C1: V_{OUT}, 0.5 V / div.
C2: I_{LOAD}, 2 A / div.
Time: 10 ms / div.

17.2.5 Output: 28 V / 5 A

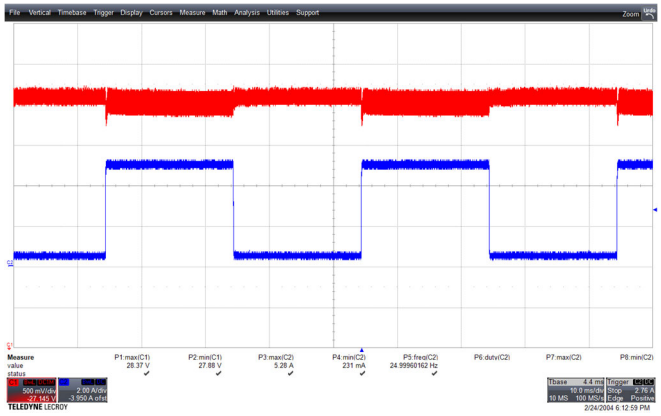


Figure 61 – Transient Response.
90 VAC, 28 V, 10% – 100% Load Step.
V_{MIN}: 27.88 V, V_{MAX}: 28.37 V.
C1: V_{OUT}, 0.5 V / div.
C2: I_{LOAD}, 2 A / div.
Time: 10 ms / div.

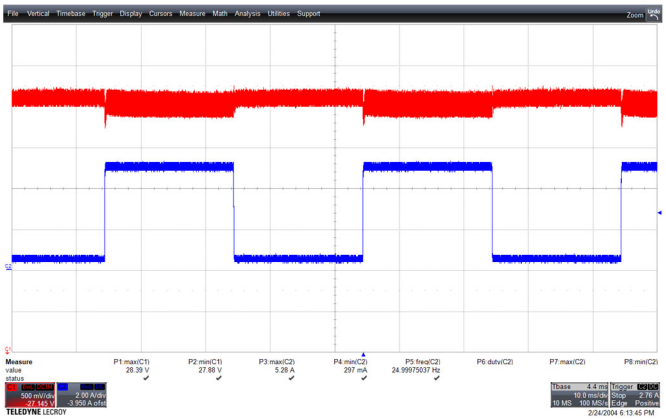


Figure 62 – Transient Response.
265 VAC, 28 V, 10% – 100% Load Step.
V_{MIN}: 27.88 V, V_{MAX}: 28.39 V.
C1: V_{OUT}, 0.5 V / div.
C2: I_{LOAD}, 2 A / div.
Time: 10 ms / div.

17.3 *InnoSwitch4-CZ Drain Voltage and Current (Steady-State)*

17.3.1 Output: 5 V / 3 A

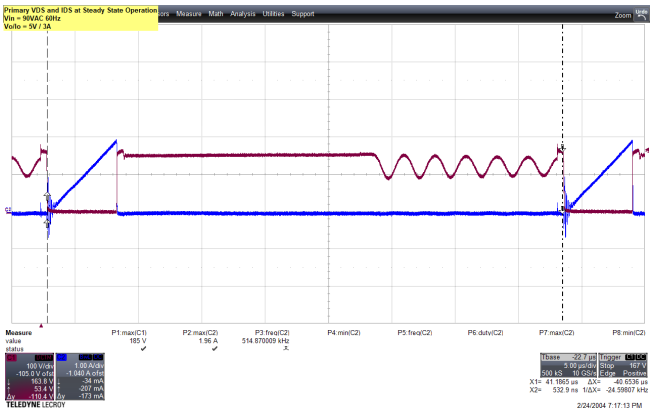


Figure 63 – InnoSwitch4-CZ Drain Voltage and Current.
90 VAC, 5 V, 3 A Load (185 V_{MAX}).
C1: V_{DRAIN}, 100 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 5 µs / div.

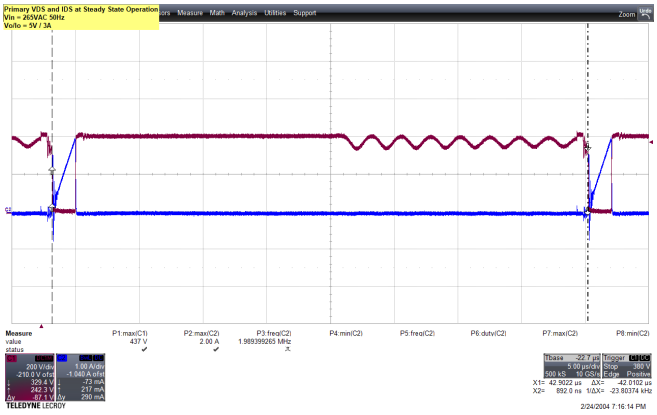


Figure 64 – InnoSwitch4-CZ Drain Voltage and Current.
265 VAC, 5 V, 3 A Load (437 V_{MAX}).
C1: V_{DRAIN}, 200 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 5 µs / div.

17.3.2 Output: 9 V / 3 A

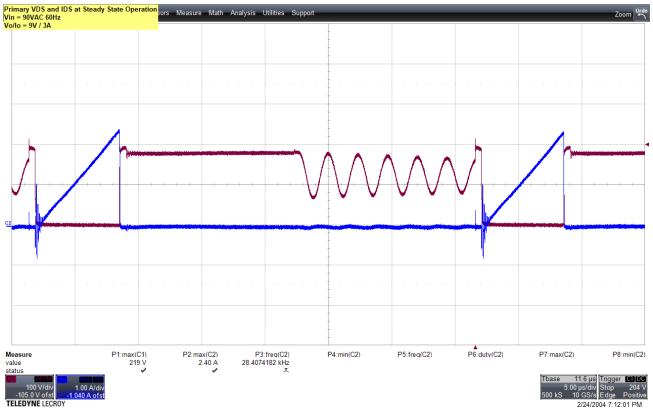


Figure 65 – InnoSwitch4-CZ Drain Voltage and Current.
90 VAC, 9 V, 3 A Load (219 V_{MAX}).
C1: V_{DRAIN}, 50 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 5 µs / div.

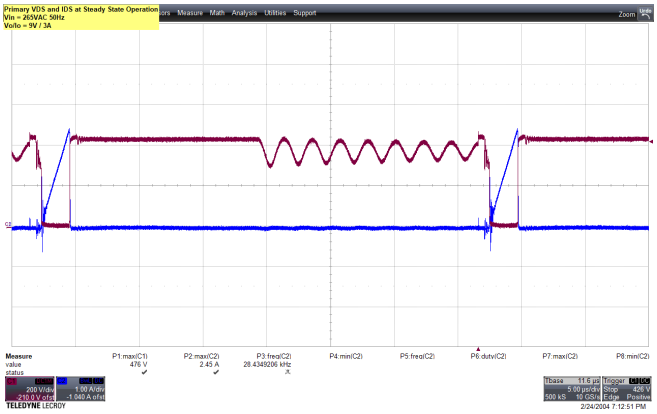


Figure 66 – InnoSwitch4-CZ Drain Voltage and Current.
265 VAC, 9 V, 3 A Load (476 V_{MAX}).
C1: V_{DRAIN}, 200 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 5 µs / div.

17.3.3 Output: 15 V / 3 A

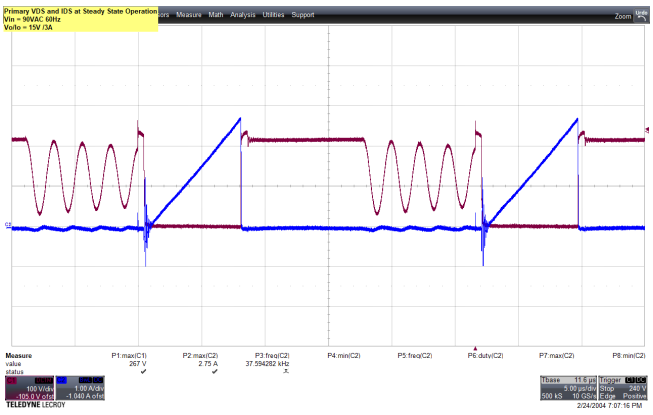


Figure 67 – InnoSwitch4-CZ Drain Voltage and Current.
90 VAC, 15 V, 3 A Load (267 V_{MAX}).
C1: V_{DRAIN}, 100 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 5 µs / div.

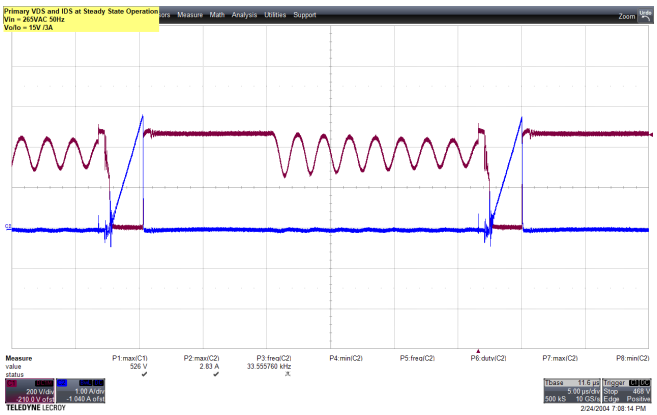


Figure 68 – InnoSwitch4-CZ Drain Voltage and Current.
265 VAC, 15 V, 3 A Load (56 V_{MAX}).
C1: V_{DRAIN}, 200 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 5 µs / div.

17.3.4 Output: 20 V / 5 A

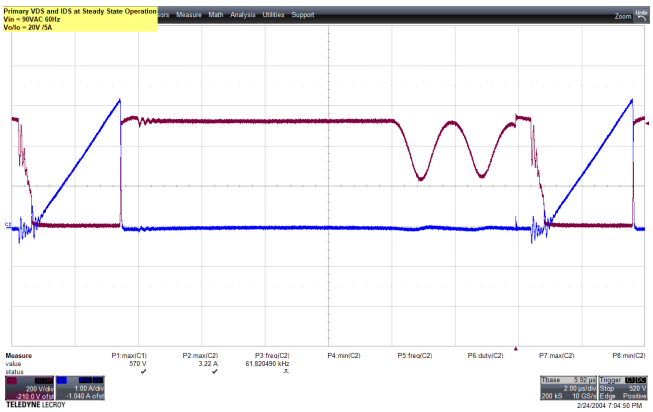


Figure 69 – InnoSwitch4-CZ Drain Voltage and Current.
90 VAC, 20 V, 5 A Load (570 V_{MAX}).
C1: V_{DRAIN}, 200 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 2 µs / div.

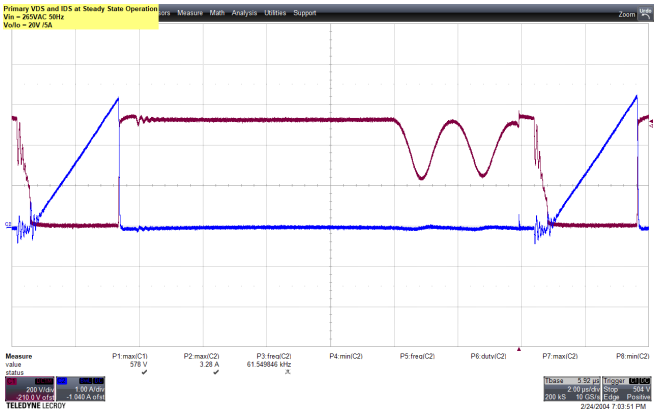


Figure 70 – InnoSwitch4-CZ Drain Voltage and Current.
265 VAC, 20 V, 5 A Load (578 V_{MAX}).
C1: V_{DRAIN}, 200 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 2 µs / div.

17.3.5 Output: 28 V / 5 A

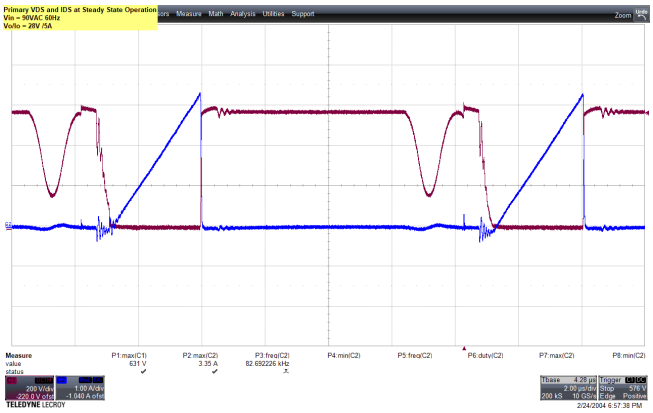


Figure 71 – InnoSwitch4-CZ Drain Voltage and Current.
90 VAC, 28 V, 5 A Load (631 V_{MAX}).
C1: V_{DRAIN}, 200 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 2 µs / div.

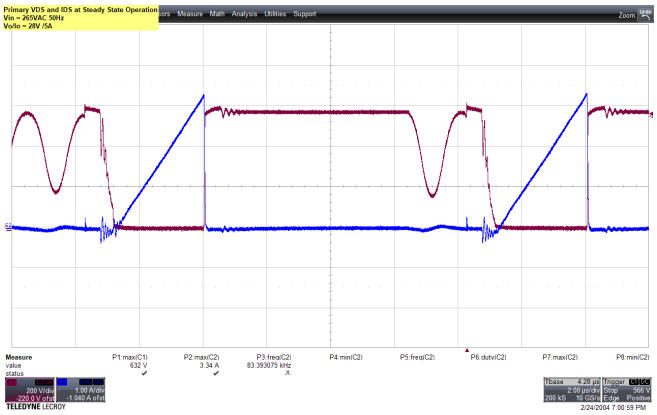


Figure 72 – InnoSwitch4-CZ Drain Voltage and Current.
265 VAC, 28 V, 5 A Load (632 V_{MAX}).
C1: V_{DRAIN}, 200 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 2 µs / div.

17.4 *ClampZero Drain Voltage and Current (Steady-State)*

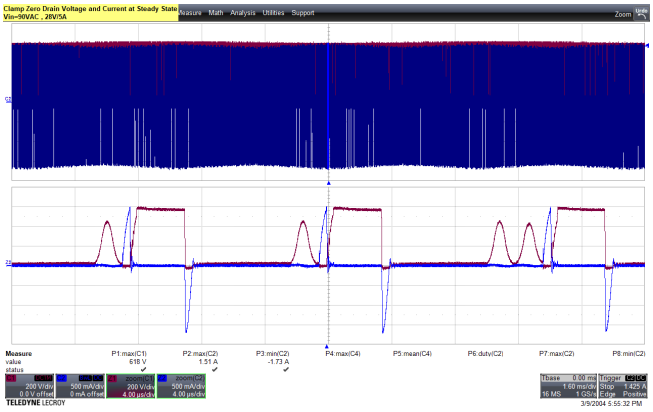


Figure 73 – ClampZero Drain Voltage and Current.
90 VAC, 28 V, 5 A Load (618 V_{MAX}).
C1: V_{DRAIN}, 200 V / div.
C2: I_{DRAIN}, 500 mA / div.
Time: 2 µs / div.

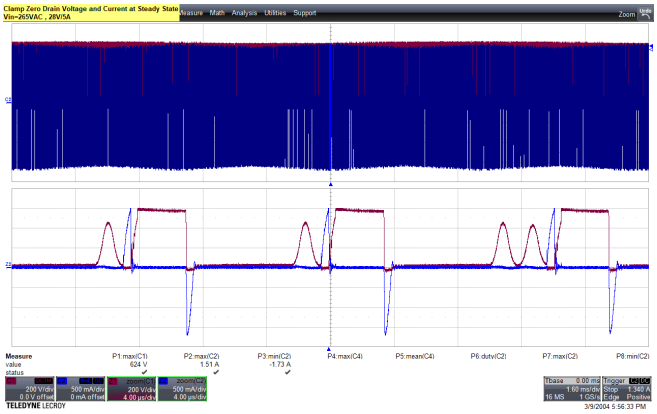


Figure 74 – ClampZero Drain Voltage and Current.
265 VAC, 28 V, 5 A Load (624 V_{MAX}).
C1: V_{DRAIN}, 200 V / div.
C2: I_{DRAIN}, 500 mA / div.
Time: 2 µs / div.

17.5 *SR FET Drain Voltage and Load Current (Steady-State)*

Figure 75 – SR FET Drain Voltage.
90 VAC, 5 V, 3 A Load (61 V_{MAX}).
C1: V_{DRAIN}, 20 V / div.
Time: 5 μs / div.

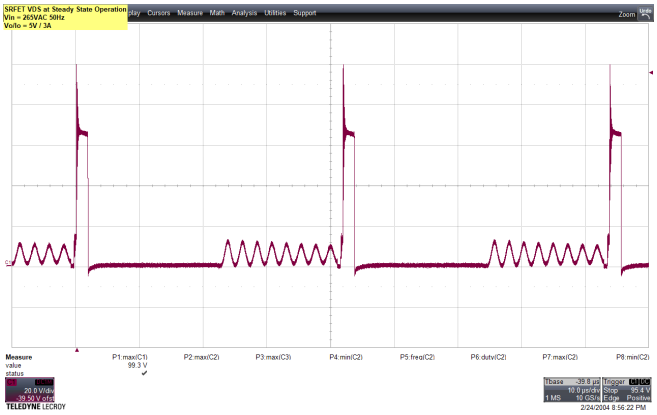


Figure 76 – SR FET Drain Voltage.
265 VAC, 5 V, 3 A Load (99.3 V_{MAX}).
C1: V_{DRAIN}, 20 V / div.
Time: 5 μs / div.

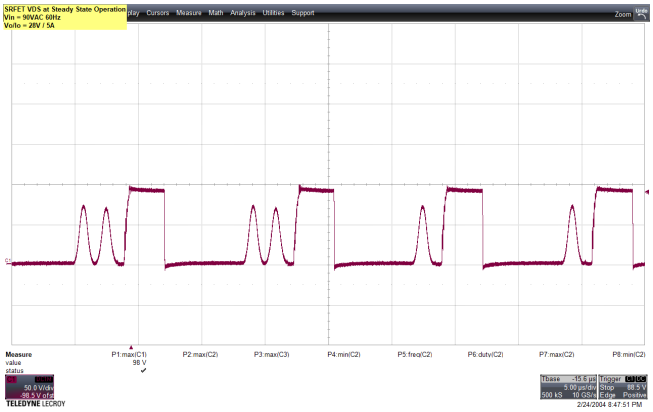


Figure 77 – SR FET Drain Voltage.
90 VAC, 28 V, 5 A Load (98 V_{MAX}).
C1: V_{DRAIN}, 50 V / div.
Time: 5 μs / div.

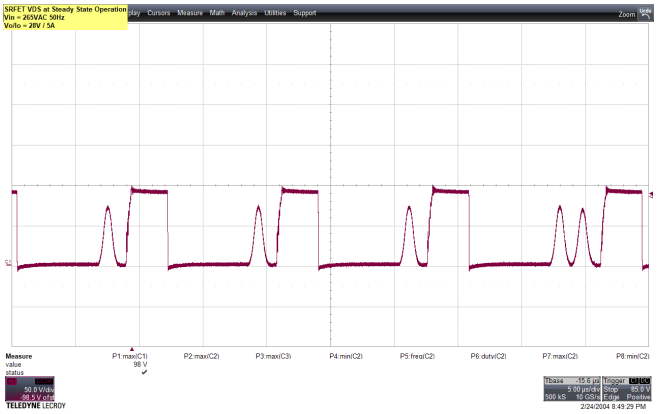


Figure 78 – SR FET Drain Voltage.
265 VAC, 28 V, 5 A Load (98 V_{MAX}).
C1: V_{DRAIN}, 50 V / div.
Time: 5 μs / div.

17.6 *HiperPFS-5 Drain Voltage and Current (Steady-State)*

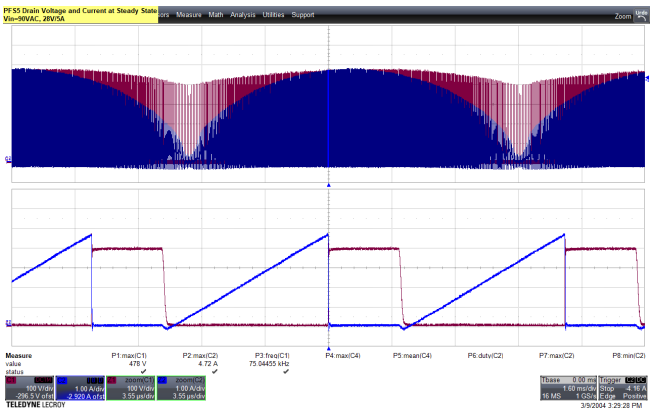


Figure 79 – HiperPFS-5 Drain Voltage and Current.
90 VAC, 28 V, 5 A Load (478 V_{MAX}).
C1: V_{DRAIN}, 100 V / div.
C2: I_{DRAIN}, 1 A / div.
Time (Zoom): 3.55 µs / div.

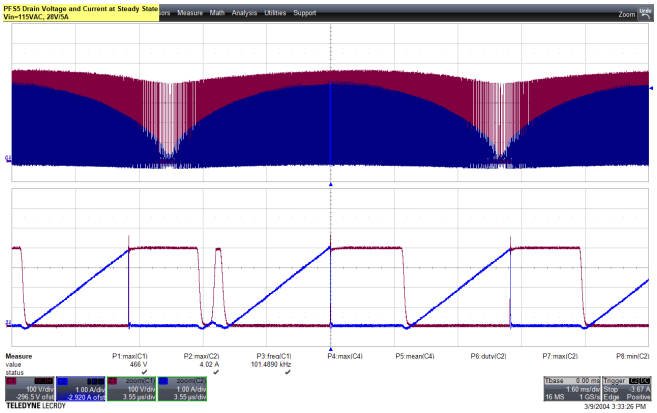


Figure 80 – HiperPFS-5 Drain Voltage and Current.
115 VAC, 28 V, 5 A Load (466 V_{MAX}).
C1: V_{DRAIN}, 100 V / div.
C2: I_{DRAIN}, 1 A / div.
Time (Zoom): 3.55 µs / div.

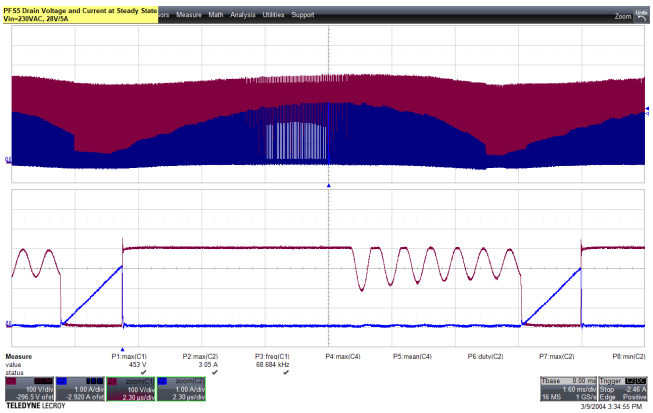


Figure 81 – HiperPFS-5 Drain Voltage and Current.
230 VAC, 28 V, 5 A Load (453 V_{MAX}).
C1: V_{DRAIN}, 100 V / div.
C2: I_{DRAIN}, 1 A / div.
Time (Zoom): 2.3 µs / div.

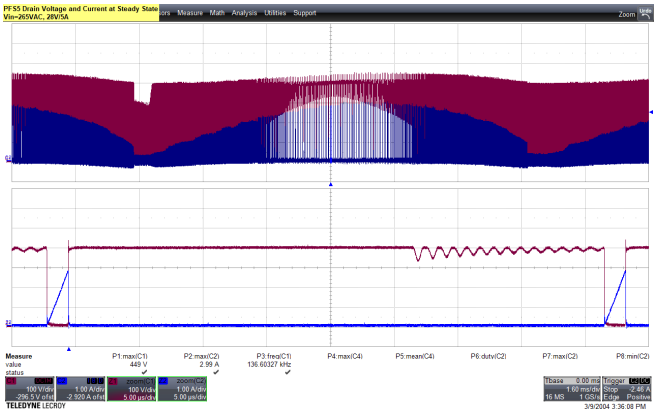


Figure 82 – HiperPFS-5 Drain Voltage and Current.
265 VAC, 28 V, 5 A Load (449 V_{MAX}).
C1: V_{DRAIN}, 100 V / div.
C2: I_{DRAIN}, 1 A / div.
Time (Zoom): 5 µs / div.

18 Output Ripple Measurements

18.1 *Ripple Measurement Technique*

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 10 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

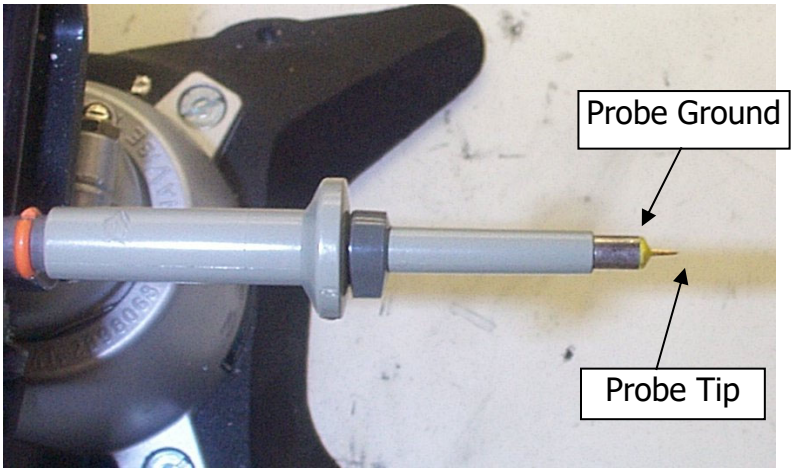


Figure 83 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

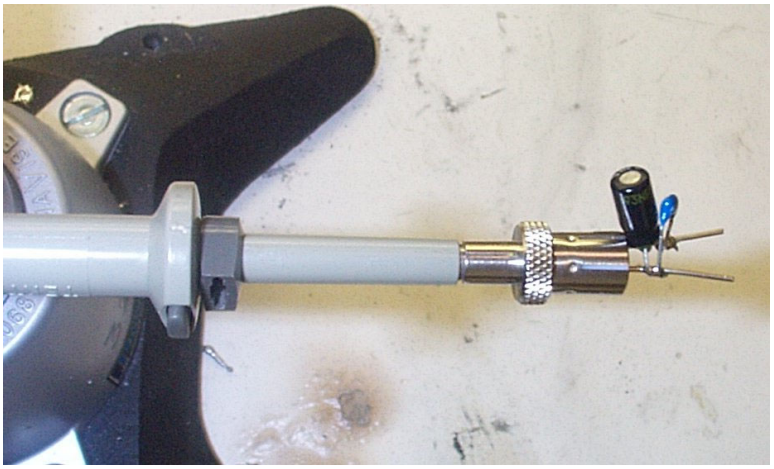


Figure 84 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added).

18.2 *Output Voltage Ripple vs. Load*

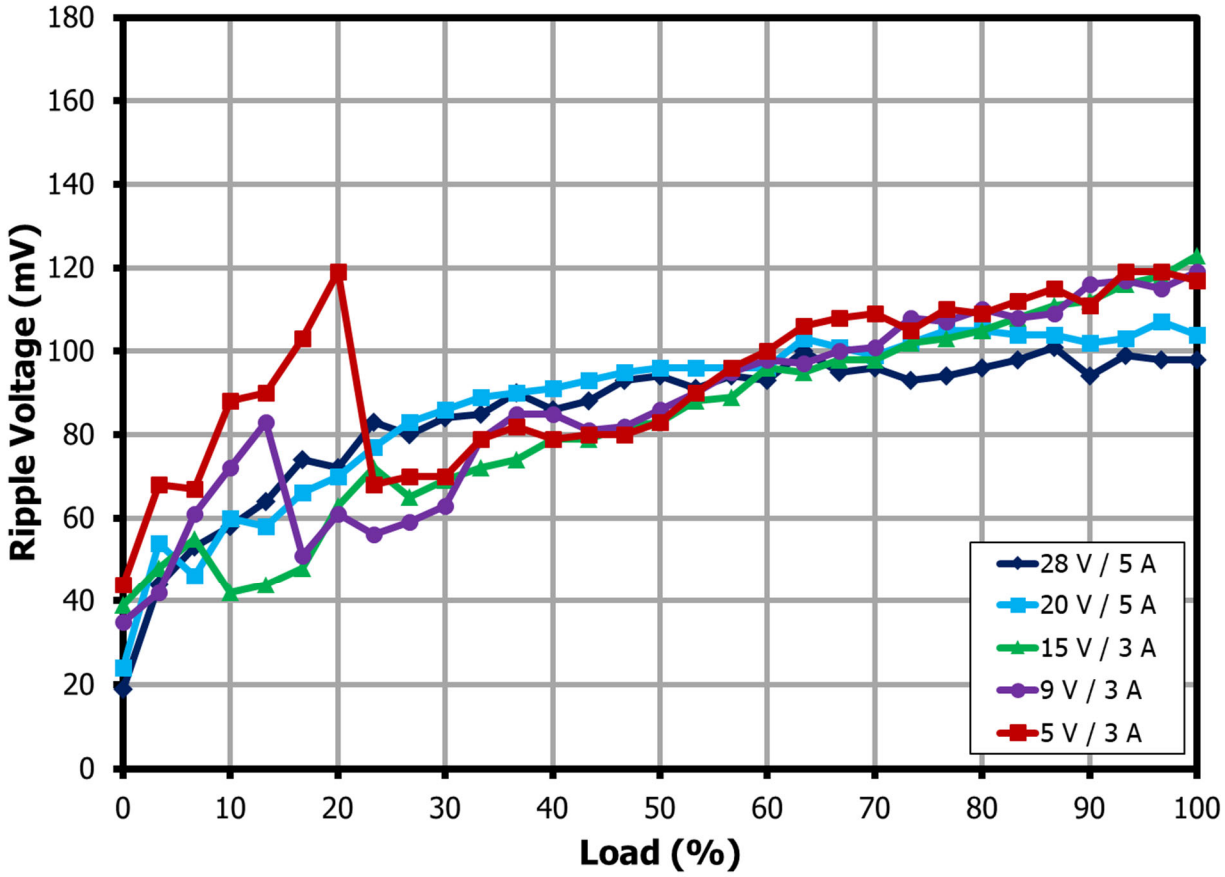


Figure 85 – Output Voltage Ripple vs. Load, 90 VAC.

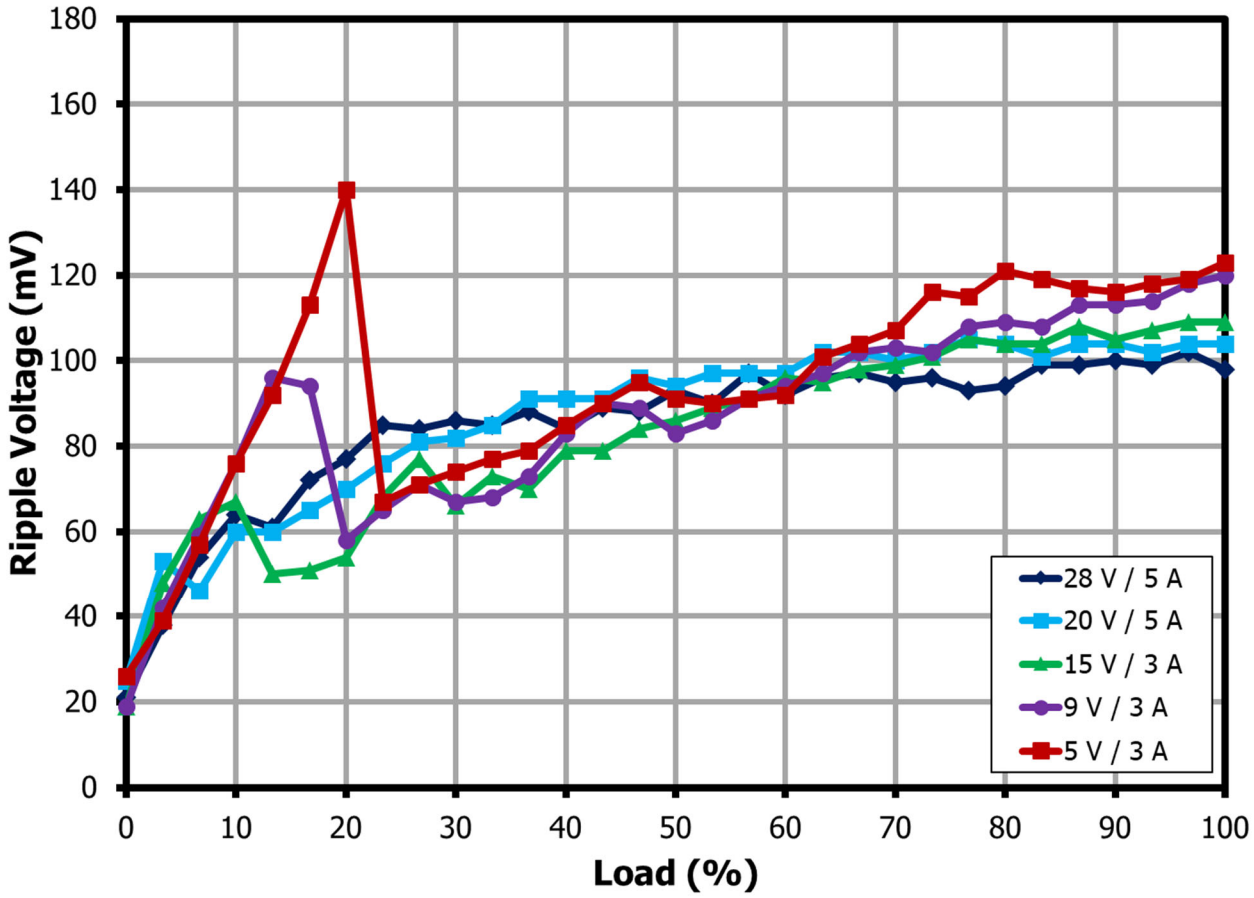


Figure 86 – Output Voltage Ripple vs. Load, 265 VAC.

18.3 *Output Voltage Ripple Waveforms*

Note 1: Output voltage ripple waveforms are captured at the end of the cable.
2: Measurements taken at room temperature (approximately 24 °C)

18.3.1 Output: 5 V / 3 A

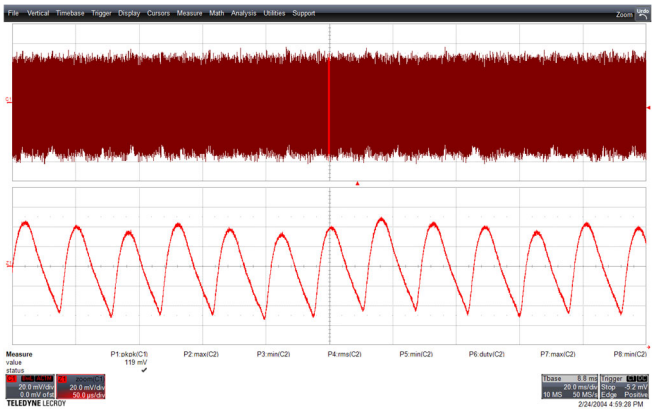


Figure 87 – Input Voltage and Current.
90 VAC, 5 V, 3 A Load.
C1: V_{IN}, 20 mV / div.
V_{RIPPLE}: 119 mV_{PK-PK}.
Time (Zoom): 50 µs / div.

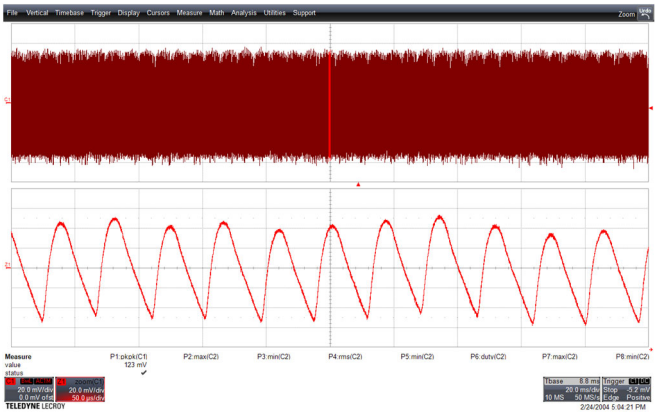


Figure 88 – Input Voltage and Current.
265 VAC, 5 V, 3 A Load.
C1: V_{IN}, 20 V / div.
V_{RIPPLE}: 123 mV_{PK-PK}.
Time (Zoom): 50 µs / div.

18.3.2 Output: 9 V / 3 A

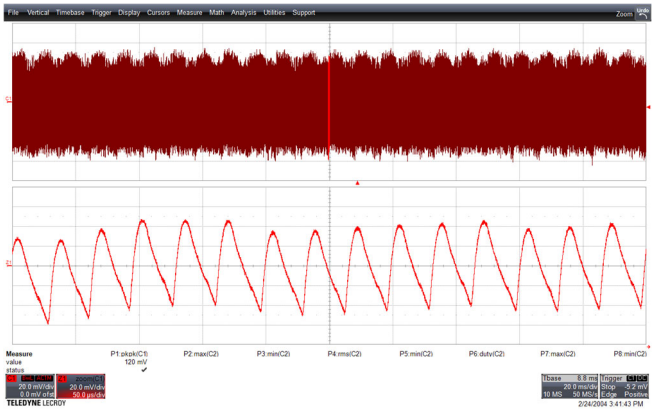


Figure 89 – Input Voltage and Current.
90 VAC, 9 V, 3 A Load.
C1: V_{IN}, 20 mV / div.
V_{RIPPLE}: 120 mV_{PK-PK}.
Time (Zoom): 50 µs / div.

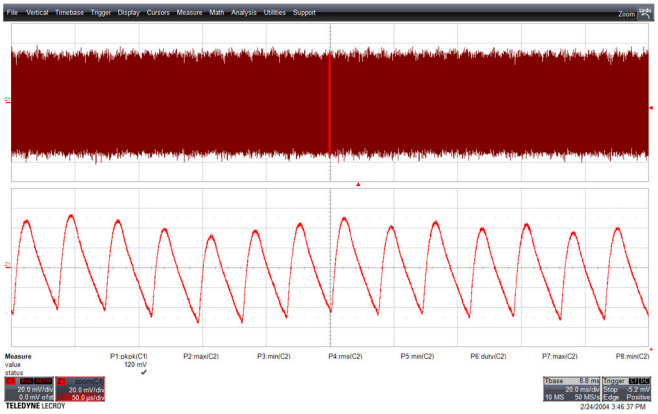


Figure 90 – Input Voltage and Current.
265 VAC, 9 V, 3 A Load.
C1: V_{IN}, 20 V / div.
V_{RIPPLE}: 120 mV_{PK-PK}.
Time (Zoom): 50 µs / div.

18.3.3 Output: 15 V / 3 A

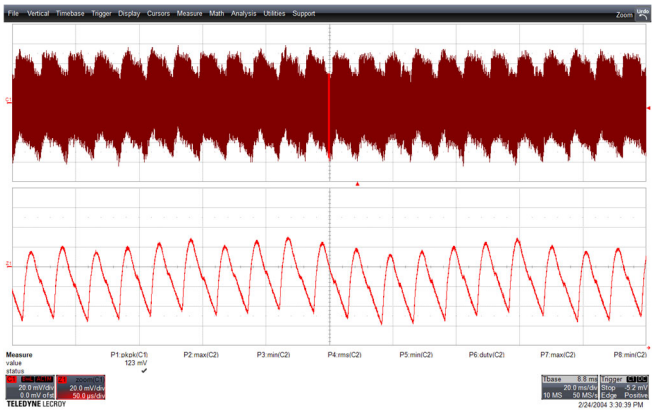


Figure 91 – Input Voltage and Current.
90 VAC, 15 V, 3 A Load.
C1: V_{IN}, 20 mV / div.
V_{RIPPLE}: 123 mV_{PK-PK}.
Time (Zoom): 50 µs / div.

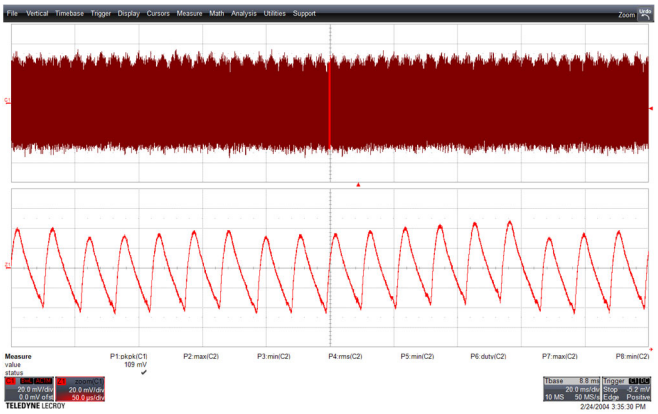


Figure 92 – Input Voltage and Current.
265 VAC, 15 V, 3 A Load.
C1: V_{IN}, 20 V / div.
V_{RIPPLE}: 109 mV_{PK-PK}.
Time (Zoom): 50 µs / div.

18.3.4 Output: 20 V / 5 A

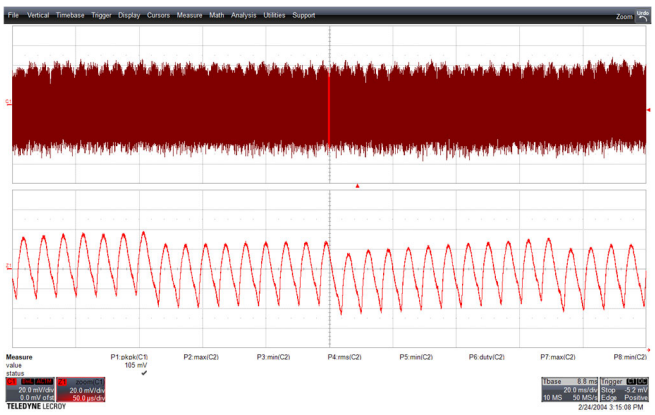


Figure 93 – Input Voltage and Current.
90 VAC, 20 V, 5 A Load.
C1: V_{IN}, 20 mV / div.
V_{RIPPLE}: 105 mV_{PK-PK}.
Time (Zoom): 50 µs / div.

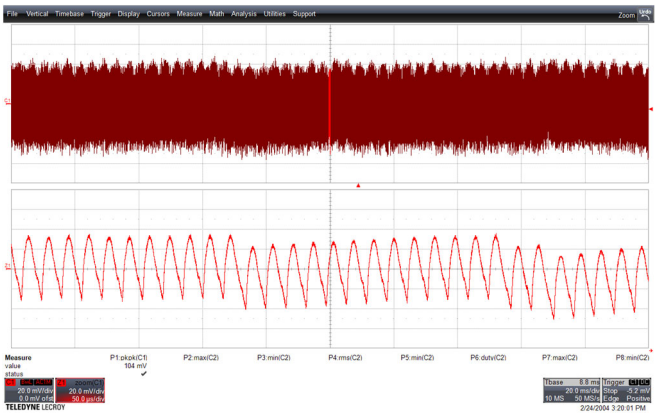


Figure 94 – Input Voltage and Current.
265 VAC, 20 V, 5 A Load.
C1: V_{IN}, 20 V / div.
V_{RIPPLE}: 104 mV_{PK-PK}.
Time (Zoom): 50 µs / div.

18.3.5 Output: 28 V / 5 A

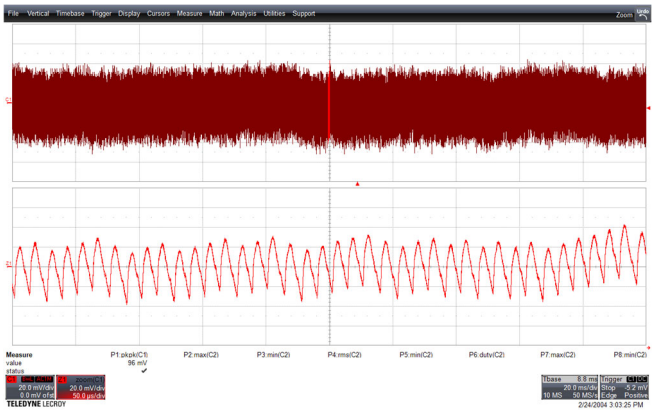


Figure 95 – Output Ripple Voltage.
90 VAC, 28 V, 5 A Load.
C1: V_{IN}, 20 mV / div.
V_{RIPPLE}: 96 mV_{PK-PK}.
Time (Zoom): 50 µs / div.

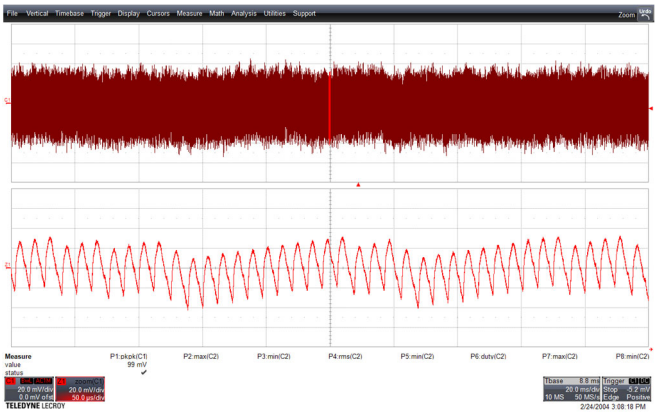


Figure 96 – Output Ripple Voltage.
265 VAC, 28 V, 5 A Load.
C1: V_{IN}, 20 V / div.
V_{RIPPLE}: 99 mV_{PK-PK}.
Time (Zoom): 50 µs / div.

18.4 ***Output Overvoltage Waveforms***

Output overvoltage condition is activated through connecting a 3 kΩ resistor across the lower feedback voltage divider resistor R36.

18.4.1 Output Overvoltage Test at No Load Steady-State

While unit is running normally at 28 V without load, a 3 kΩ resistor is connected suddenly across R36 to activate overvoltage.

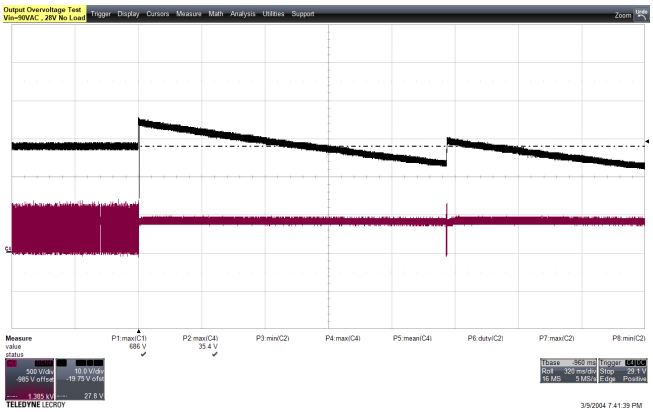


Figure 97 – Output Overvoltage Test.
90 VAC, 28 V, No-Load.
C1: V_{DS}, 500 V / div.
C4: V_{OUT}, 10 V / div.
V_{OMAX}: 35.4 V.
Time: 320 ms / div.

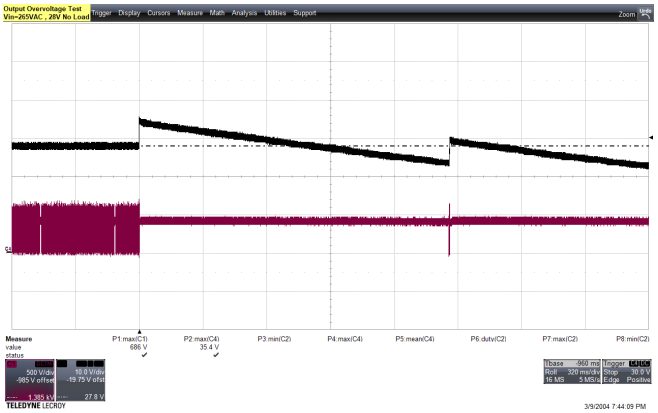


Figure 98 – Output Ripple Voltage.
265 VAC, 28 V, No-Load.
C1: V_{DS}, 500 V / div.
C4: V_{OUT}, 10 V / div.
V_{OMAX}: 35.4 V.
Time: 320 ms / div.

18.4.2 Output Overvoltage Test at Full Load

With the unit is at off state, a 3 kΩ resistor is connected across R36 then powered up the unit without load to test the overvoltage protection circuit.

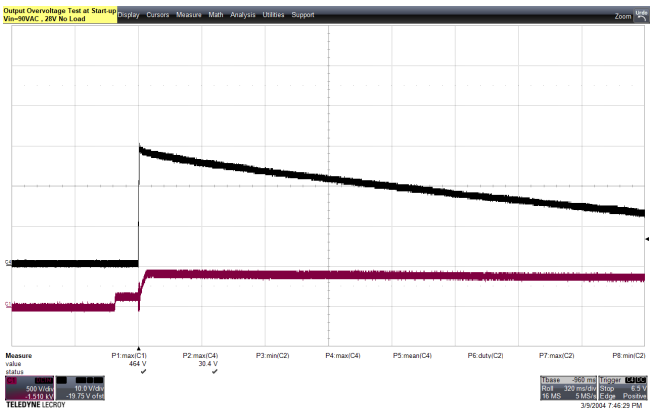


Figure 99 – Output Overvoltage Test.
90 VAC, 28 V, No-Load Start-up.
C1: V_{DS}, 500 V / div.
C4: V_{OUT}, 10 V / div.
V_{OMAX}: 30.4 V.
Time: 320 ms / div.

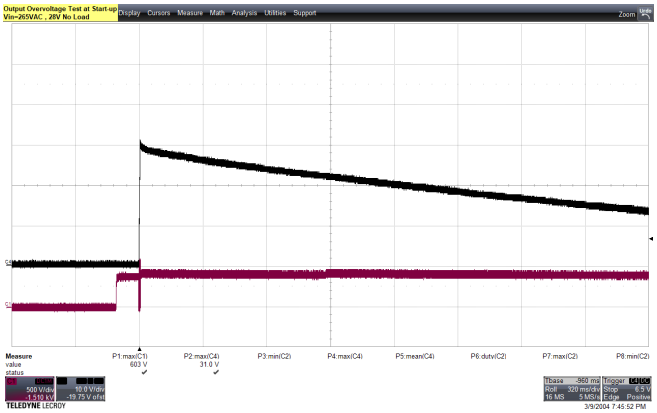


Figure 100 – Output Ripple Voltage.
265 VAC, 28 V, No-Load Start-up.
C1: V_{DS}, 500 V / div.
C4: V_{OUT}, 10 V / div.
V_{OMAX}: 31 V.
Time: 320 ms / div.

18.4.3 Output Overvoltage Test at Full Load

While unit is running normally at 28 V 5 A Load, a 3 kΩ resistor is connected suddenly across R36 to activate overvoltage.

Figure 101 – Output Overvoltage Test.
90 VAC, 28 V, 5 A Load.
C1: V_{DS}, 500 V / div.
C4: V_{OUT}, 10 V / div.
V_{OMAX}: 35 V.
Time (Zoom): 7.2 ms / div.

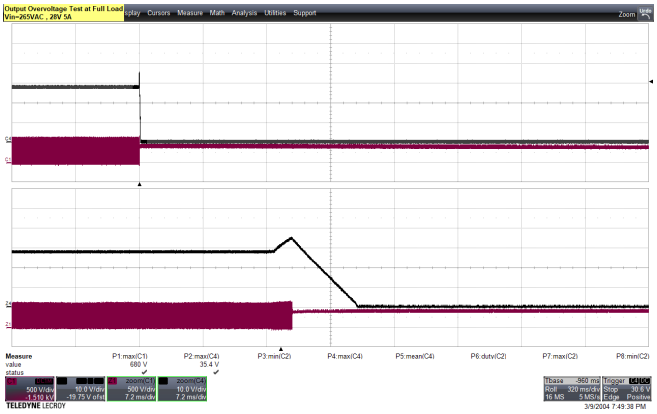
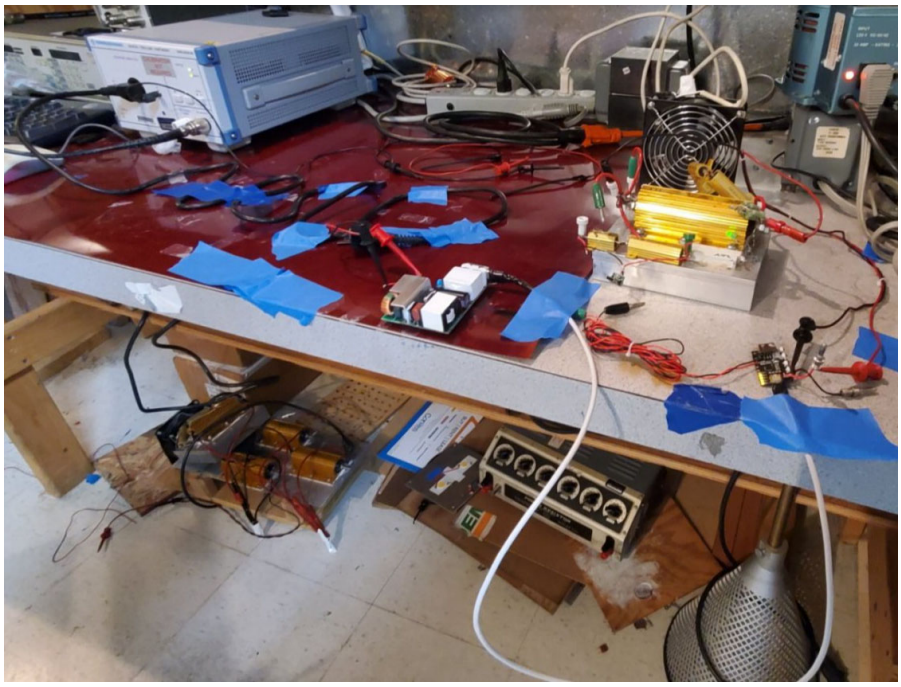


Figure 102 – Output Ripple Voltage.
265 VAC, 28 V, 5 A Load.
C1: V_{DS}, 500 V / div.
C4: V_{OUT}, 10 V / div.
V_{OMAX}: 35.4 V.
Time(Zoom): 7.2 ms / div.

19 Conducted EMI (QPK / AV)



19.1 *Floating Output*

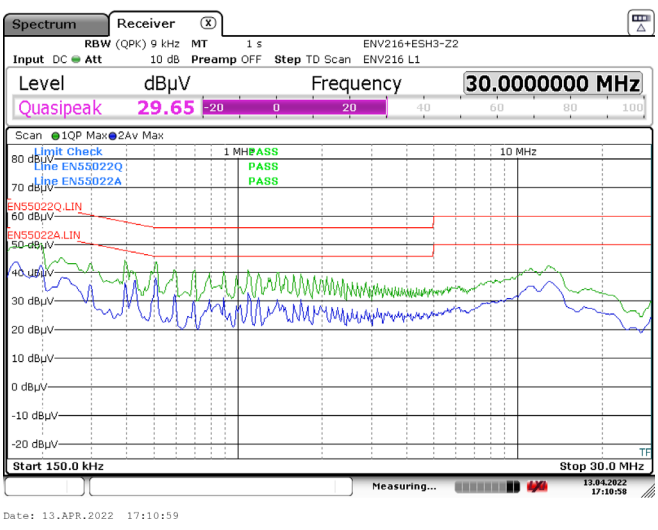


Figure 103 – Conducted EMI, Floating Output, Line. 115 VAC, 28 V, 5 A Load. Passed with 6 dB Margin.

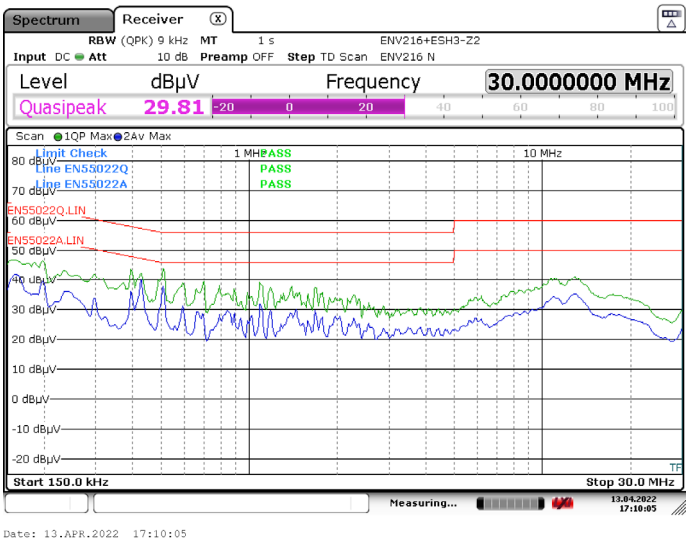


Figure 104 – Conducted EMI, Floating Output, Neutral. 115 VAC, 28 V, 5 A Load. Passed with 6 dB Margin.

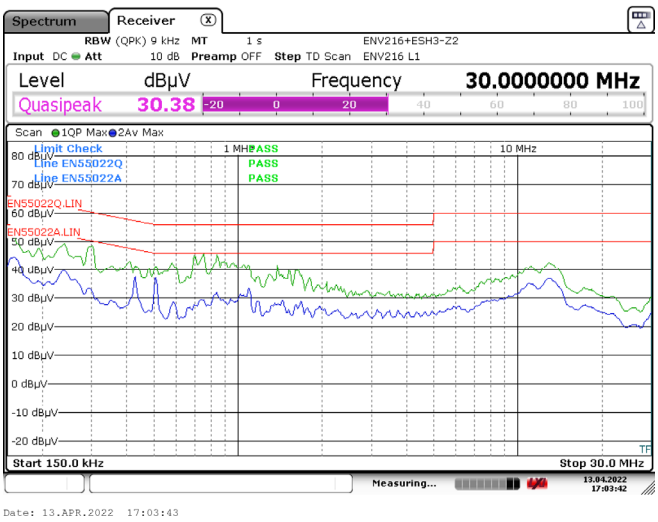


Figure 105 – Conducted EMI, Floating Output, Line.
230 VAC, 28 V, 5 A Load.
Passed with 6 dB Margin.

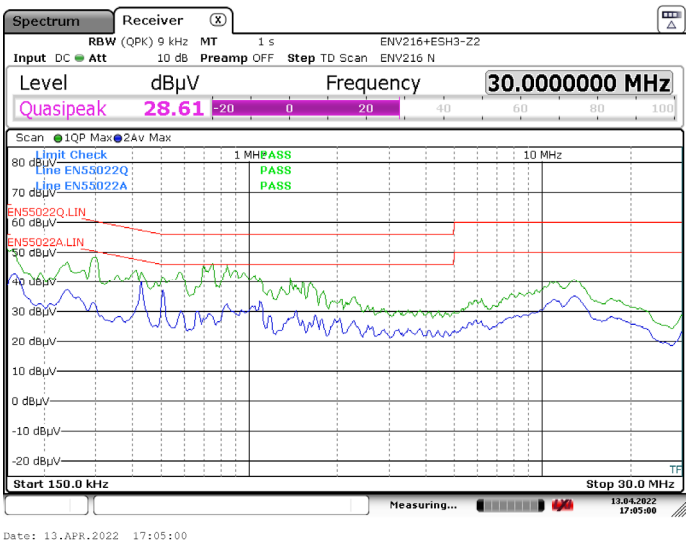


Figure 106 – Conducted EMI, Floating Output, Neutral.
230 VAC, 28 V, 5 A Load.
Passed with 6 dB Margin.

19.2 *Output Grounded*

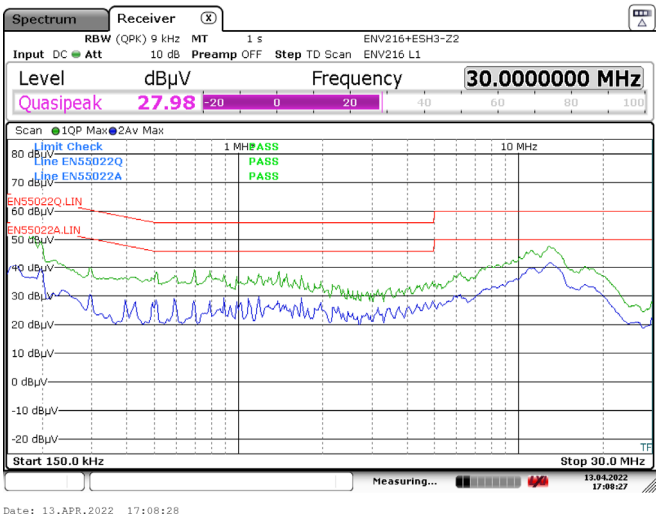


Figure 107 – Conducted EMI, Output Grounded, Line.
115 VAC, 28 V, 5 A Load.
Passed with 12 dB Margin.

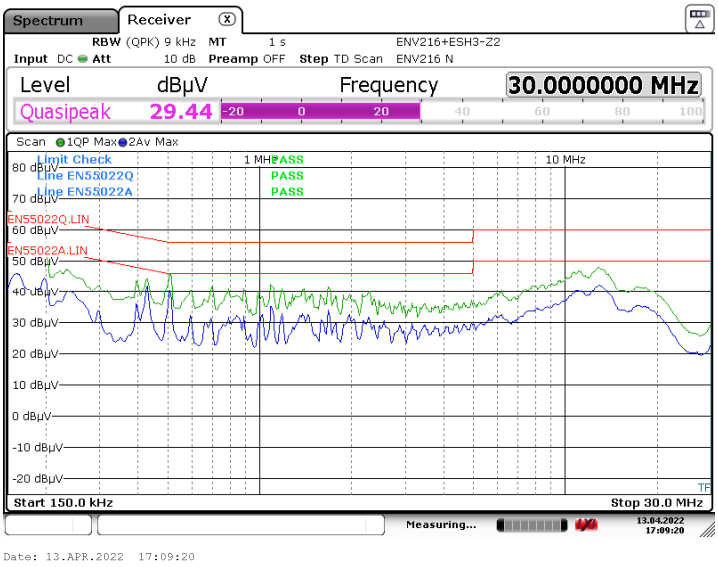


Figure 108 – Conducted EMI, Output Grounded, Neutral.
115 VAC, 28 V, 5 A Load.
Passed with 4 dB Margin.

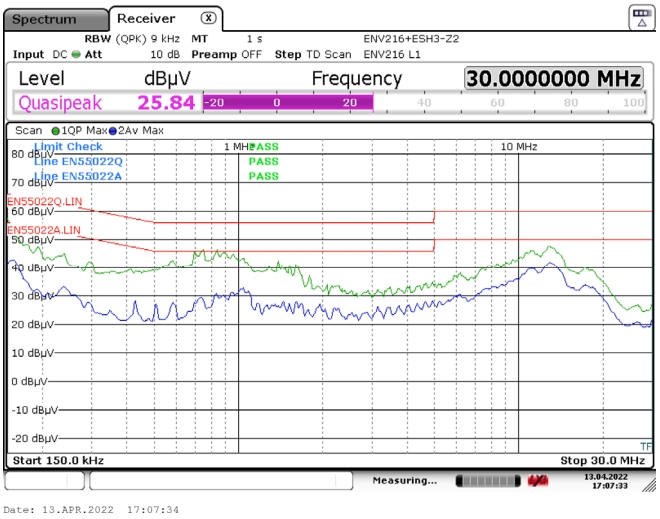


Figure 109 – Conducted EMI, Output Grounded, Line. 230 VAC, 28 V, 5 A Load. Passed with 12 dB Margin.

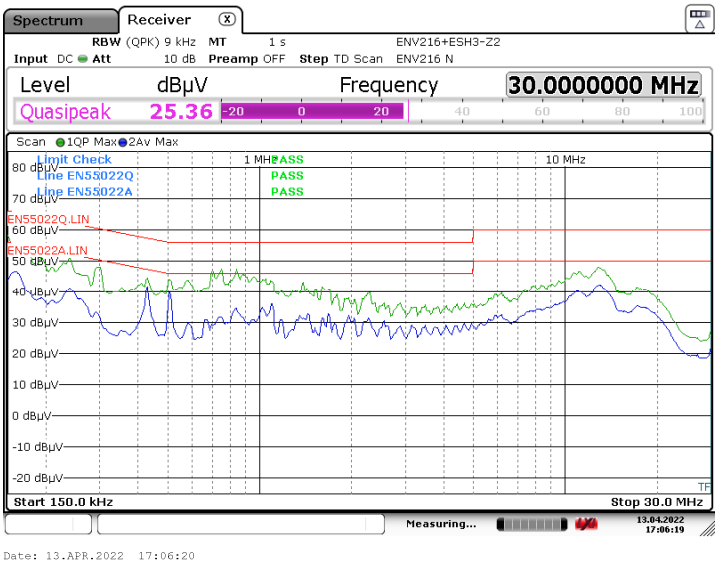


Figure 110 – Conducted EMI, Output Grounded, Neutral. 230 VAC, 28 V, 5 A Load. Passed with 5 dB Margin.

20 Surge Test

The unit was subjected to ± 2000 V differential mode and ± 2000 V common mode combination wave surge at several line phase angles with 10 strikes for each condition.

Pass* - Unit was restarting during some strikes due to line overvoltage protection.

20.1 *Combination Wave Surge at 230 VAC, Differential Mode*

Test Voltage (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
2000	230	L to N	0	Pass*
-2000	230	L to N	0	Pass
2000	230	L to N	90	Pass
-2000	230	L to N	90	Pass*
2000	230	L to N	180	Pass
-2000	230	L to N	180	Pass
2000	230	L to N	270	Pass*
-2000	230	L to N	270	Pass*

Pass* - Unit was restarting during some strikes due to line overvoltage protection.

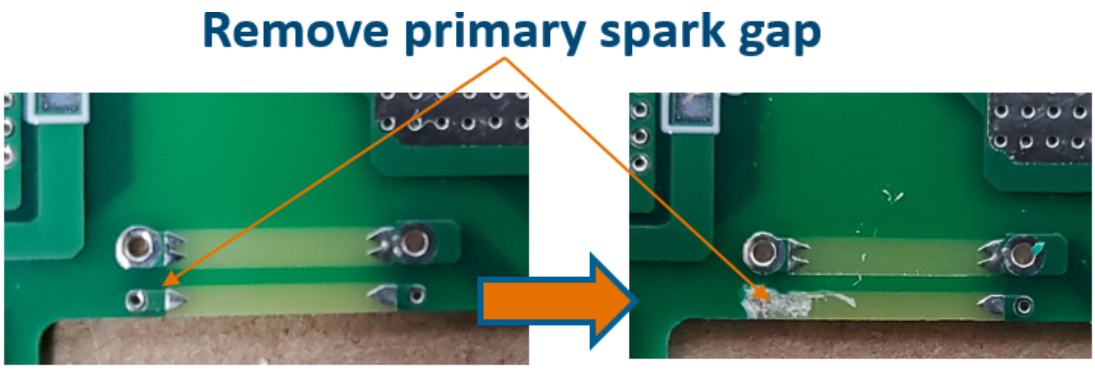
20.2 *Ring Wave Surge at 230 VAC, Differential Mode*

Test Voltage (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
2500	230	L to N	0	Pass
-2500	230	L to N	0	Pass
2500	230	L to N	90	Pass
-2500	230	L to N	90	Pass
2500	230	L to N	180	Pass
-2500	230	L to N	180	Pass
2500	230	L to N	270	Pass
-2500	230	L to N	270	Pass

21 ESD Test

ESD was tested with the PD control disabled (Q8-removed). Output load was connected across the output capacitors (C26). The feedback voltage divider resistor values were modified to provide 28 V output. For layout consideration, spark gap modification was implemented as shown in below figure. Spark gap connected to fuse (F1) must be removed to prevent arcing during ESD test

Feedback voltage divider resistor values for 28 V output:
R37 = 100 kΩ, R36 = 33 kΩ, R77 = 5.49 kΩ



No.	Test Voltage	No. of Strikes	Discharge Location	Remarks	Pass/Fail
1	+8	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
2		10	- Output Terminal End of Cable	No Damage / No AR	Pass
3	-8	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
4		10	- Output Terminal End of Cable	No Damage / No AR	Pass
5	+10	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
6		10	- Output Terminal End of Cable	No Damage / No AR	Pass
7	-10	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
8		10	- Output Terminal End of Cable	No Damage / No AR	Pass
9	+12.5	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
10		10	- Output Terminal End of Cable	No Damage / No AR	Pass
11	-12.5	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
12		10	- Output Terminal End of Cable	No Damage / No AR	Pass
13	+15	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
14		10	- Output Terminal End of Cable	No Damage / No AR	Pass
15	-15	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
16		10	- Output Terminal End of Cable	No Damage / No AR	Pass
17	+16.5	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
18		10	- Output Terminal End of Cable	No Damage / No AR	Pass
19	-16.5	10	+ Output Terminal End of Cable	No Damage / No AR	Pass
20		10	- Output Terminal End of Cable	No Damage / No AR	Pass

22 Revision History

Date	Author	Revision	Description & Changes	Reviewed
13-Jul-22	MGM	1.0	Initial Release.	Apps & Mktg

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Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Worldwide: +1-65-635-64480
Americas: +1-408-414-9621
e-mail: usasales@power.com

CHINA (SHANGHAI)
Rm 2410, Charity Plaza, No. 88,
North Caoxi Road,
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasales@power.com

CHINA (SHENZHEN)
17/F, Hivac Building, No. 2, Keji Nan 8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
e-mail: chinasales@power.com

GERMANY (AC-DC/LED Sales)
Einsteinring 24
85609 Dornach/Aschheim
Germany
Tel: +49-89-5527-39100
e-mail: eurosales@power.com

GERMANY (Gate Driver Sales)
HellwegForum 1
59469 Ense
Germany
Tel: +49-2938-64-39990
e-mail: igbt-driver.sales@power.com

INDIA
#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
e-mail: indiasales@power.com

ITALY
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI) Italy
Phone: +39-024-550-8701
e-mail: eurosales@power.com

JAPAN
Yusen Shin-Yokohama 1-chome Bldg.
1-7-9, Shin-Yokohama, Kohoku-ku
Yokohama-shi,
Kanagawa 222-0033 Japan
Phone: +81-45-471-1021
e-mail: japansales@power.com

KOREA
RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

SINGAPORE
51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
e-mail: singaporesales@power.com

TAIWAN
5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
e-mail: taiwansales@power.com

UK
Building 5, Suite 21
The Westbrook Centre
Milton Road
Cambridge
CB4 1YG
Phone: +44 (0) 7823-557484
e-mail: eurosales@power.com