

Design Example Report

Title	184 W Non-PFC Stage Forward Power Supply Using HiperTFS [™] -2 TFS7704H	
Specification	90 VAC – 132 VAC Input; 184 W (23 V at 0.5 - 8 A) Output (CV/CC)	
Application	Battery Charger	
Author	Applications Engineering Department	
Document Number DER-483		
Date	April 15, 2019	
Revision	5.0	

Summary and Features

- Integrated forward power stage and flyback standby for a very low component count design
- 90-132 VAC voltage doubler Input (no PFC)
- 132 kHz forward stage for small magnetics size
- >87% full load efficiency

PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at http://www.powerint.com/ip.htm>.

> Power Integrations 5245 Hellyer Avenue, San Jose, CA 95138 USA. Tel: +1 408 414 9200 Fax: +1 408 414 9201 www.power.com

Table of Contents

1	Introd	uction	5			
2	· •··•· ••••••••••••••••••••••••••••••					
	2.1 Actual Customer Specification for Output Voltage/ Current Limit					
3	Schem					
4	Circuit Description					
	4.1 O	/erview	11			
	4.2 EN	1I Filtering / Voltage Doubler	11			
	4.3 Pr	imary Bias Supply	11			
	4.4 M	ain Forward Converter / Standby	11			
	4.5 O	utput Rectification	13			
	4.6 0	utput Current and Voltage Control	13			
5		yout				
6	Bill of	Materials	15			
7	Magne	tics	17			
	7.1 Tr	ansformer (T1) Specification	17			
	7.1.1	Electrical Diagram	17			
	7.1.2	Electrical Specifications	17			
	7.1.3	Material List	17			
	7.1.4	Build Diagram	18			
	7.1.5	Winding Instructions				
	7.1.6	Winding Illustrations				
	7.2 St	andby Transformer Specification	26			
	7.2.1	Electrical Diagram	26			
	7.2.2	Electrical Specifications	26			
	7.2.3	Material List	26			
	7.2.4	Build Diagram	27			
	7.2.5	Winding Instructions	27			
	7.2.6	Transformer Illustrations	28			
	7.3 M	ain Output Choke	33			
	7.3.1	Schematic	33			
	7.3.2	Material List	33			
	7.3.3	Winding Illustration	33			
8	Main/S	tandby Converter Design Spreadsheet	34			
9		inks				
	9.1 Pr	imary Heat Sink				
	9.1.1	Primary Heat Sink Sheet Metal	42			
	9.1.2	Primary Heat Sink with Fasteners	43			
	9.1.3	Primary Heat Sink Assembly	44			
	9.2 Se	econdary Heat Sink	45			
	9.2.1	Secondary Heat Sink Sheet Metal	45			
	9.2.2	Secondary Heat Sink with Fasteners	46			
	9.2.3	Secondary Heat Sink Assembly	47			



10 Performance Data	.48
10.1 Output Load Considerations for Testing a CV/CC Supply in Battery Charger	
Applications	.48
10.2 Efficiency	
10.3 V-I Characteristic	.50
10.3.1 V-I Characteristic, Constant Resistance Load	
10.3.2 Output V-I Characteristic, Constant Voltage Load	.51
11 Waveforms	.52
11.1 Primary Voltage and Current, Main and Standby Converters	
11.2 Output Rectifier Peak Reverse Voltage	
11.3 Main Start-up Output Voltage/Current and Transformer Primary Current Using	J
Constant Voltage and Constant Voltage Output Loads	.54
11.4 Load Transient Response, Voltage Mode	.55
11.5 Output Ripple Measurements	.56
11.5.1 Ripple Measurement Technique	.56
11.5.2 Output Ripple Measurements	.57
12 Temperature Profiles	
12.1 Spot Temperature Measurements	.58
12.2 90 VAC, 60 Hz, 100% Load Temperature Profile	.58
13 Gain-Phase	.59
13.1 Constant Voltage Mode Gain-Phase	.59
13.2 Constant Current Mode Gain-Phase	
13.2.1 Current Mode Gain Phase Using Chroma 63106 Electronic Load Set for CV	V
Mode 60	
14 Conducted EMI	.61
14.1 Unmodified Supply EMI Scan	
14.2 EMI Results Using Supplemental HF Common Mode AC Input Choke	.63
15 Revision History	



Important Notes:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. All testing should be performed using an isolation transformer to provide the AC input to the prototype board.



1 Introduction

This engineering report describes a 23 V (nominal), 184 W reference design for a power operating from 90-132 VAC. The power supply is designed with a constant voltage / constant current output for use in battery charger applications.

The design is based on the TFS7704H operating from doubled mains, with no PFC input stage.



Figure 1 – DER-483, Top View.



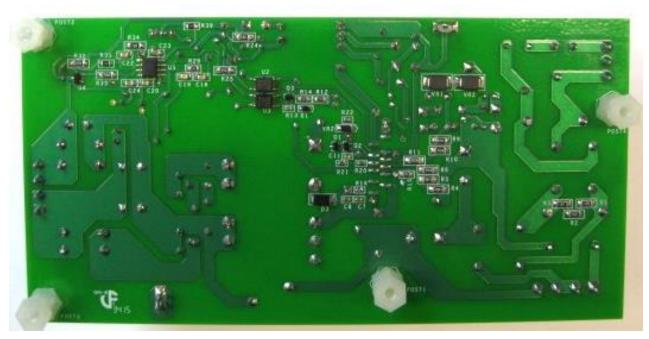


Figure 2 – DER-483, Bottom View.



2 Power Supply Specification

The table below represents the specification for the design detailed in this report. Actual performance is listed in the results section. Detailed customer specification is shown below.

Description	Symbol	Min	Тур	Max	Units	Comment
Input Voltage Frequency	V _{IN} f _{LINE}	90 47	50/60	132 64	VAC Hz	3 Wire input.
Main Converter Output						
Output Voltage	V _{OUT}	0		23	V	23 VDC (nominal – otherwise defined by battery load)
Output Current	I OUT	6		8	А	Nominal Current Limit Setting for Design
Output Current Limit (Optional)			0.5	1	А	Programmed using additional Resistor
Total Output Power						
Continuous Output Power Peak Output Power	Р _{оит} Р _{оит(рк)}		184	N/A	W W	23V/8A
Efficiency Total system at Full Load	η _{Main}		90		%	Measured at 115 VAC, Full Load
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				/ EN55022B
Safety		Designed to meet IEC950 / UL1950 Class II			0 / UL1950 Class II	
Surge Differential Common Mode					kV kV	1.2/50 μs surge, IEC 1000-4-5, Differential Mode: 2 $Ω$ Common Mode: 12 $Ω$
Ambient Temperature	Т _{АМВ}	0		60	°C	See thermal section for conditions



2.1 Actual Customer Specification for Output Voltage/ Current Limit

An actual customer specification for output voltage and current is shown below, and is considerably more complex than the simple implementation described in this report. The end application will incorporate a microcontroller that performs the function of battery recognition/authentication, and selection of output voltage and current limit depending on battery type and state of charge. Output voltage and current limit can be programmed by manipulating the reference voltages feeding the output voltage / current sensing amplifiers in the secondary control circuit.

The circuit shown in this report is designed to supply the maximum output voltage of 23 V with output current limit set to a nominal value of 8 A. A pair of holes are provided on the printed circuit board to allow inserting an extra resistor to program the output current limit down to 0.5 A in order to examine the behavior of the supply at this current limit.

Description	Symbol	Min	Тур	Max	Units	Comments
Output Voltage	Vo	0	12/14/18	23	VDC	Programmed by microcontroller depending on battery type.
Output Current	I _{O1}	0.45	0.5	1	А	Programmed by microcontroller when Vo is 0 V to 9 V.
	I _{O2}	4.5		6	A	Programmed by microcontroller when battery voltage is 12 V to 15 V for 18 V battery. Current limit is pulsed from 4.5 to 6 A.
	I _{O3}	6		8	А	Full current charging, when battery voltage is 15 V to 18 V, set be microcontroller.



3 Schematic

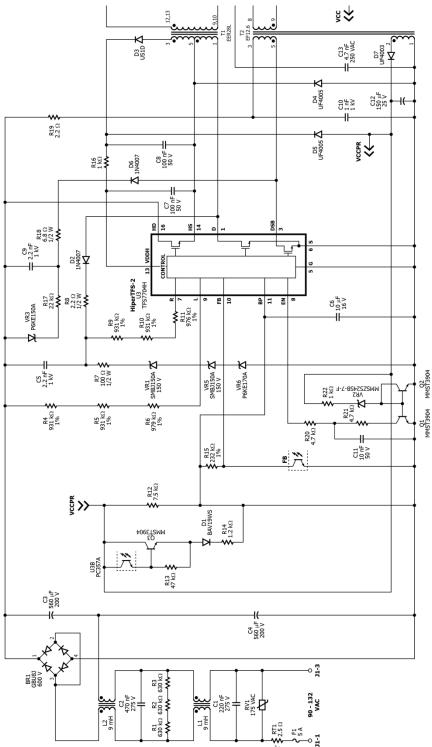


Figure 3a – Schematic HiperTFS-2 Forward Battery Charger Application Circuit - Input Filter, Forward Stage, Bias Supplies and Output Voltage/Current Control.



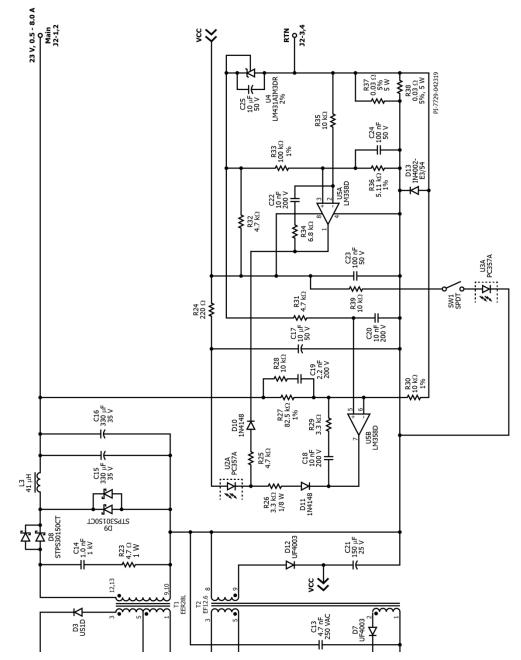


Figure 3b – Schematic HiperTFS-2 Forward Battery Charger Application Circuit - Input Filter, Forward Stage, Bias Supplies and Output Voltage/Current Control.



4 Circuit Description

4.1 **Overview**

The schematic in Figure 3 shows a forward converter topology power supply with a flyback standby utilizing the TFS7704H, powered via a voltage doubler. The secondary control circuitry provides CV/CC control for use in battery charger applications

4.2 EMI Filtering / Voltage Doubler

Capacitors C1 and C2 are used to control differential mode noise. Resistors R1-3 discharge C1 and C2 when AC power is removed. Inductors L1 and L2 primarily control common mode EMI, and to some extent, differential mode EMI. The heat sink for U1 and BR1 is connected to primary return to eliminate the heat sink as a source of radiated / capacitively coupled noise. Thermistor RT1 provides inrush limiting. Capacitor C13 filters common mode EMI. Capacitors C3 and C4, along with BR1, form a voltage doubler to provide a ~250-380 VDC B+ supply from the 90-132 VAC input.

4.3 *Primary Bias Supply*

The standby supply utilizes built-in capability of the U1 TFS2 device. Components U1, T2 Q1-2, D7, VR2, C10-12, and R20-22 comprise a regulated 15 V flyback bias supply for U1.

Components D12 and C21 generate a 12V bias supply for the secondary control circuitry via a triple insulated winding on T2 Components R24 and C17 provide extra filtering for the secondary bias supply.

4.4 Main Forward Converter / Standby

The schematic in Figure 3 depicts a 23 V, 184 W forward DC-DC converter with constant voltage/ constant current output implemented using the TFS7704H.

Integrated circuit U1 incorporates the control circuitry, drivers and output MOSFETs necessary for a 2-switch forward converter and a flyback standby converter.

Components D6, C9, R17-18, and VR3 form a turn-off clamping circuit that limits the standby drain voltage of U1. Zener diode VR3 provides a defined clamp voltage and maintains a maximum voltage (150 V) on clamp capacitor C9 for lower no / light load power consumption.

The low-side drain of the main output forward converter is clamped by D2, R7-8, C5, and VR1, VR5, and VR6. This clamping scheme is described as "clamp to ground" and enables a wider operating duty cycle for the main forward converter. This in turn allows the turns ratio of main transformer T1 to be dropped (lower peak output voltage), enabling use of lower voltage rating (lower voltage drop) components for forward output rectifier D8 and catch diode D9.



Most of the leakage and magnetizing energy associated with the main and standby converters is returned back to the B+ supply due to the slow recovery aspect of blocking diodes D2 and D6. During the main converter off-time, the main transformer is reset by a substantially higher voltage than V_{IN} , hence the main converter can operate above 50% duty cycle, lowering RMS switch currents without penalizing holdup time. Use of a clamp to ground snubber for the main converter instead of the usual clamp to rail scheme allows this advantage to be exploited even further.

The BYPASS (BP) pin along with C6 provides a decoupled regulated 5.85 V for the HiperTFS-2 controller. The value for C6 (10 μ F) also selects 132 kHz as the operating frequency for the main converter. At start-up the bypass capacitor is charged from a current source internal to U1. When the BP pin voltage reaches 5.8 V, the standby converter can begin switching and both the secondary and primary-side bias voltages will begin to rise. Output of the primary bias winding is used to supply power via resistors R12 and R14 to the HiperTFS-2 BP pin during standby-only operation. Additional current is provided via Q3 and D1 by the primary bias supply when remote-on switch SW1 activates U3A and U3B and drives Q3 into an ON state. The value of R12 is selected to maintain the minimum 700 μ A required into BP pin to inhibit the internal HiperTFS-2 high voltage current source and thus reduce no-load consumption.

The ENABLE (EN) pin is the feedback pin for the flyback standby controller section. Prior to start-up a resistor connected from EN to BP can be detected by the controller to select one of several internal current limits for standby section. In this case there is no resistor, which selects the minimum internal current limit for the standby controller. FEEDBACK (FB) pin resistor R15 can also be used to select one of three main current limits at start-up in the same manner as the EN pin. Three different values can be used for R15 to select one of the three current limit configurations for the Main section. The circuit presented here uses an open circuit at the EN pin for a standby I_{LIM} of 500 mA and 232 k Ω for R15, setting a main I_{LIM} of 3.1 A.

The FB pin provides feedback for the main converter. An increase in current sinking from FB pin to ground will reduce the operating duty cycle.

Capacitor C7 is the filtering and charge storage capacitor for the U1 high-side driver. During start-up the high-side MOSFET HS pin of U1 is briefly pulled to Source for 12 ms to precharge C7 using an internal current source. The nominal voltage on C7 during normal operation is internally shunt regulated to approximately 12 V. Components D3, C8, and R16 provide an efficient alternate source of current to power the high-side driver of U1, so that the internal high-voltage supply for the high-side driver is turned off. This increases efficiency at light load and prevents pulse skipping.



Resistors R9-R11 are used to translate the maximum available OFF time reset voltage into a current for the R pin for comparison with the L pin current to compute the maximum allowable duty cycle to prevent saturation and to also determine the maximum allowable duty factor as a function of peak on-time flux.

The LINE-SENSE (L) pin provides an input bulk voltage line-sense function. This information is used by the undervoltage and overvoltage detection circuits for both the main and standby sections. This pin can also be pulled down to SOURCE to implement a remote-ON/OFF for both the standby and main supplies simultaneously. Resistors R4- R6 are used to translate the input voltage into a current for the L pin.

4.5 *Output Rectification*

The output of main transformer T1 is rectified and filtered by D8-9, L3, C15-16. Output rectifiers D8 and D9 are 150 V Schottky rectifiers chosen for high efficiency. A snubber (R23 and C14) helps limit the peak voltage excursion on the output rectifiers.

4.6 Output Current and Voltage Control

Output current is sensed via resistors R37 and R38. These resistors are clamped by diode D13 to avoid damage to the current control circuitry during an output short circuit. Components R32 and U4 provide a voltage reference for current sense and voltage sense amplifiers U5A and U5B. The reference voltage for current sense amplifier U5A is divided down by R33 and R36, and filtered by C24. **The default current limit setting is 8 A, as programmed by R33 and R36 and R36 and R37-38.** An extra resistor can be placed from J3-J4 (across R36) to program a lower current limit. Voltage from the current sense resistors is applied to the inverting input of U5A via R35. Opamp U5A drives optocoupler U2 via D10 and R25. Components R25, R34-35, and C22 are used for frequency compensation of the current loop. Opamp U5B is used for output constant voltage control when the current limit is not engaged. Resistors R27 and R30 sense the output voltage. A reference voltage is applied to the non-inverting input of U5B from U4 via filter components R31 and C20. Opamp U5B drives optocoupler U2 via D11 and R26. Components R26-29, R30, and C18-19 all affect the frequency compensation of the voltage control loop.

Components R39, SW1, and U3 provide remote start. When SW1 is closed, the output transistor of U3 turns on Q3, providing start-up current to the main converter via the BP pin of U1. Opening SW1 turns off U3, shutting down the main converter function of U1.



5 PCB Layout

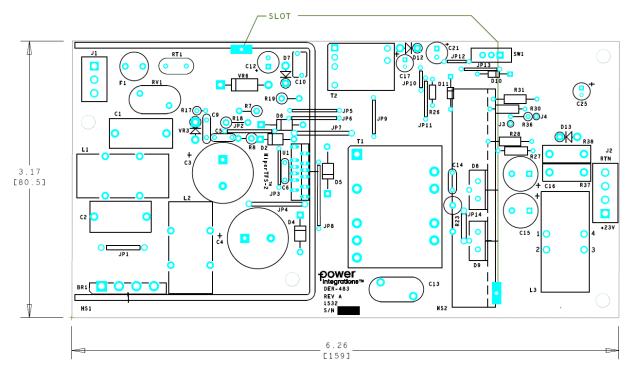
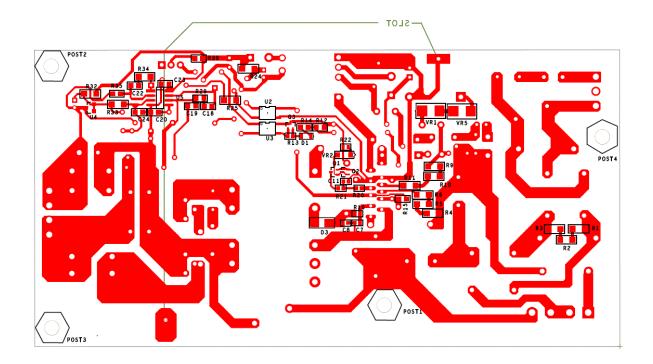


Figure 4 – Printed Circuit Layout, Top Side.







6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 8 A, Bridge Rectifier, GBU Case	GBU8J-BP	Micro Commercial
2	1	C1	220 nF, 275 VAC, Film, X2	ECQ-U2A224ML	Panasonic
3	1	C2	470 nF, 275 VAC, Film, X2	80-R46KI347050P1M	Kemet
4	2	C3 C4	560 μF, 200 V, Electrolytic, 20 %, Gen. Purpose, (18 x 47 mm)	200KXW560MEFC18X45	Rubycon
5	1	C5	2.2 nF, 1 kV, Ceramic, SL, 0.2" L.S.	DEBB33A222KA2B	Murata
6	1	C6	10 μF, 16 V, Ceramic, X5R	FK24X5R1C106K	TDK
7	2	C7 C8	100 nF 50 V, Ceramic, X7R, 0603	C1608X7R1H104K	TDK
8	1	С9	2.2 nF, 1 kV, Disc Ceramic	NCD222K1KVY5FF	NIC
9	2	C10 C14	1.0 nF, 1 kV, Disc Ceramic	562R10TSD10	Vishay
10	1	C11	10 nF 50 V, Ceramic, X7R, 0603	C0603C103K5RACTU	Kemet
11	2	C12 C21	150 μ F, 25 V, Electrolytic, Low ESR, 180 m Ω , (6.3 x 15)	ELXZ250ELL151MF15D	Nippon Chemi-Con
12	1	C13	4.7 nF, Ceramic, Y1	440LD47-R	Vishay
13	2	C15 C16	330 μ F, 35 V, Electrolytic, Low ESR, 68 m Ω , (10 x 16)	ELXZ350ELL331MJ16S	Nippon Chemi-Con
14	2	C17 C25	10 μF, 50 V, Electrolytic, Gen. Purpose, (5 x 11)	EKMG500ELL100ME11D	Nippon Chemi-Con
15	3	C18 C20 C22	10 nF, 200 V, Ceramic, X7R, 0805	08052C103KAT2A	AVX
16	1	C19	2.2 nF, 200 V, Ceramic, X7R, 0805	08052C222KAT2A	AVX
17	2	C23 C24	100 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB104	Yageo
18	1	D1	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
19	2	D2 D6	1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay
20	1	D3	DIODE ULTRA FAST, SW, 200V, 1A, SMA	US1D-13-F	Diodes, Inc.
21	2	D4 D5	600 V, 1 A, Ultrafast Recovery, 75 ns, DO-41	UF4005-E3	Vishay
22	2	D7 D12	200 V, 1 A, Ultrafast Recovery, 50 ns, DO-41	UF4003-E3	Vishay
23	2	D8 D9	150 V, 15 A, Schottky, TO-220AB	STPS30150CT	ST
24	2	D10 D11	75 V, 300 mA, Fast Switching, DO-35	1N4148TR	Vishay
25	1	D13	100 V, 1 A, Rectifier, DO-41	1N4002-E3/54	Vishay
26	1	ESIP CLIP1	Heat sink Hardware, Edge Clip, 12.40 mm x 6.50 mm	TRK-24	Kang Tang
27	1	F1	5 A, 250 V, Slow, TR5	37215000411	Wickman
28	1	HOTMELT_V1	Adhesive, Hot Melt, VO	3748 VO-TC	3M
29	1	HS1	FAB, Heat Sink, BRIDGE_Esip, DER483		Custom
30	1	HS2	FAB, Heat Sink, DIODES, DER-483		Custom
31	1	J1	3 Position (1 x 3) header, 0.156 pitch, Vertical	26-48-1031	Molex
32	1	J2	4 Position (1 x 4) header, 0.156 pitch, Vertical	26-48-1045	Molex
33	2	J3 J4	PCB Terminal Hole, #30 AWG	N/A	N/A
34	2	JP1 JP14	Wire Jumper, Insulated, TFE, #18 AWG, 0.5 in	C2052A-12-02	Alpha
35	1	JP2	Wire Jumper, Insulated, TFE, #18 AWG, 0.6 in	C2052A-12-02	Alpha
36	4	JP3 JP9 JP11 JP13	Wire Jumper, Insulated, #24 AWG, 0.5 in	C2003A-12-02	Gen Cable
37	2	JP4 JP7	Wire Jumper, Insulated, TFE, #18 AWG, 0.7 in	C2052A-12-02	Alpha
38	2	JP5 JP6	Wire Jumper, Insulated, #24 AWG, 0.6 in	C2003A-12-02	Gen Cable
39	1	JP8	Wire Jumper, Insulated, #24 AWG, 0.8 in	C2003A-12-02	Gen Cable
40	1	JP10	Wire Jumper, Insulated, #24 AWG, 0.2 in	C2003A-12-02	Gen Cable
41	1	JP12	Wire Jumper, Insulated, #24 AWG, 0.3 in	C2003A-12-02	Gen Cable
42	2	L1 L2	9 mH, 5 A, Common Mode Choke	T22148-902S P.I. Custom	Fontaine
43	1	L3	Custom, DER-483, 41 µH, Inductor Toroidal		
44	4	POST1 POST2 POST3 POST4	Post, Circuit Board, Female, Hex, 6-32, snap, 0.375L, Nylon	561-0375A	Eagle Hardware
45	3	Q1 Q2 Q3	NPN, Small Signal BJT, 40 V, 0.2 A, SOT-323	MMST3904-7-F	Diodes, Inc.
46	3	R1 R2 R3	680 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ684V	Panasonic



48	2	R6 R11	976 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF9763V	Panasonic
49	1	R7	100 Ω, 5%, 1/2 W, Carbon Film	CF12JT100R	Stackpole
50	1	R8	2.2 Ω, 5%, 1/2 W, Carbon Film	CFR-50JB-2R2	Yageo
51	1	R12	7.5 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ752V	Panasonic
52	1	R13	47 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ473V	Panasonic
53	1	R14	1.2 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ122V	Panasonic
54	1	R15	232 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2323V	Panasonic
55	2	R16 R22	1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
56	1	R17	22 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-22K	Yageo
57	1	R18	6.8 Ω, 5%, 1/2 W, Carbon Film	CFR-50JB-6R8	Yageo
58	1	R19	2.2 Ω , 5%, 1/2 W, Metal Film, Fusible/Flame Proof	NFR25H0002208JR500	Vishay
59	2	R20 R21	4.7 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ472V	Panasonic
60	1	R23	4.7 Ω, 5%, 1 W, Metal Oxide	RSF100JB-4R7	Yageo
61	1	R24	220 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ221V	Panasonic
62	2	R25 R32	4.7 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ472V	Panasonic
63	1	R26	3.3 kΩ, 5%, 1/8 W, Carbon Film	CF18JT3K30	Stackpole
64	1	R27	82.5 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-82K5	Yageo
65	1	R28	10 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-10K	Yageo
66	1	R29	3.3 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ332V	Panasonic
67	1	R30	10.0 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-10K0	Yageo
68	1	R31	4.7 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-4K7	Yageo
69	1	R33	100 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1003V	Panasonic
70	1	R34	6.8 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ682V	Panasonic
71	2	R35 R39	10 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ103V	Panasonic
72	1	R36	5.11 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-5K11	Yageo
73	2	R37 R38	0.03 Ω, 5 W, 5%, Current Sense	MPR5JB30L0	Stackpole
74	1	RT1	NTC Thermistor, 2.5 Ohms, 5 A	SL10 2R505	Ametherm
75	3	RTV1 RTV2 RTV3	Thermally conductive Silicone Grease	120-SA	Wakefield
76	1	RV1	175 V, 70 J, 14 mm, RADIAL	ERZ-V14D271	Panasonic
77	1	SCREW1	SCREW MACHINE PHIL 4-40 X 1/4 SS	PMSSS 440 0025 PH	Building Fasteners
78	3	SCREW2 SCREW3 SCREW4	SCREW MACHINE PHIL 4-40 X 3/16 SS	67413609	MSC Industrial Supply
79	2	SPACER_CER1 SPACER_CER2	SPACER RND, Steatite C220 Ceramic	CER-2	Richco
80	1	SW1	SWITCH SLIDE SPDT 30 V, 2 A PC MNT	EG1218	E-Switch
81	1	T1	Transformer, EER28L, Vertical, 14 pins		
82	1	T2	Transformer, EF12.6, Horizontal, 9 pins		1
83	1	U1	TFS-7704H, ESIP16/12	TFS7704H	Power Integrations
84	2	U2 U3	Optocoupler, 80 V, CTR 80-160%, 4-Mini Flat	PC357N1TJ00F	Sharp
85	1	U4	OBS see 45-00268-00. IC, REG ZENER SHUNT ADJ SOT-23	LM431AIM3/NOPB	National Semi
86	1	U5	DUAL Op Amp, Single7Supply, SOIC-8	LM358D	TI
87	2	VR1 VR5	150 V, 5 W, 5%, DO214AA (SMB)	SMBJ150A	Littlefuse
88	1	VR2	DIODE ZENER 15V 500MW SOD123	MMSZ5245B-7-F	Diodes, Inc.
89	1	VR3	150 V, 5 W, 5%, TVS, DO204AC (DO-15)	P6KE150A	Littlefuse
90	1	VR6	170 V, 5 W, 5%, TVS, DO204AC (DO-15)	P6KE170A	Littlefuse
91	1	WASHER1	WASHER FLAT #4 SS	FWSS 004	Building Fasteners
92	3	WASHER2 WASHER3 WASHER4	WASHER FLAT #4 Zinc, OD 0.219, ID 0.125, Thk 0.032, Yellow Chromate Finish	5205820-2	Тусо



7 Magnetics

7.1 Transformer (T1) Specification

7.1.1 Electrical Diagram

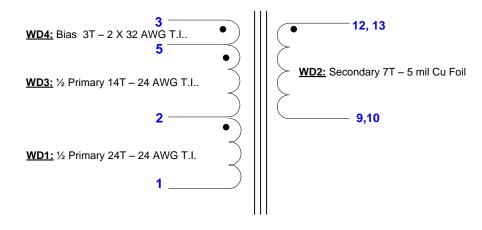


Figure 6 – Main Forward Transformer Schematic.

7.1.2 *Electrical Specifications*

Electrical Strength	1 second, 60 Hz, from pins 1-6 to 10-13.	3000 VAC
Primary Inductance	Pins 1 and 5, all other windings open, measured at 100 kHz, 0.4 V_{RMS} .	3.5 mH ±20%
Resonant Frequency	Pins 1 and 5, all other windings open.	500 kHz (Min.)
Primary Leakage Inductance	Pins 1 and 5, with pins 9-13 shorted, measured at 100 kHz, 0.4 V_{RMS} .	5 μH (Max.)

7.1.3 Material List

Item	Description	
[1]	Core Pair EER28L: TDK PC44 or equivalent.	
[2]	Bobbin: EER28L Vertical, 14 pins – PI 25-00022-00 (Yih Hwa YW-545-00B or equivalent).	
[3]	Wire: Triple Insulated, #24 AWG – Furukawa Tex-E or equivalent.	
[4]	Wire: Triple Insulated, #32 AWG – Furukawa Tex-E or equivalent.	
[5]	Wire: Tinned Bus Wire, #22 AWG.	
[6]	Copper Foil, 0.13 mm (0.005") thick, 16 mm wide, and 348.0 mm long.	
[7]	Tape: Polyester Film, 3M 1350F-1 or equivalent, 24 mm wide.	
[8]	Tape: Polyester Film, 3M 1350F-1 or equivalent, 21 mm wide.	
[9]	Tape: Polyester Film, 3M 1350F-1 or equivalent, 16 mm wide.	
[10]	Tape: Polyester Web, 3M #44 or equivalent, 3 mm wide.	
[11]	Varnish: Dolph BC-359, or equivalent.	



7.1.4 Build Diagram

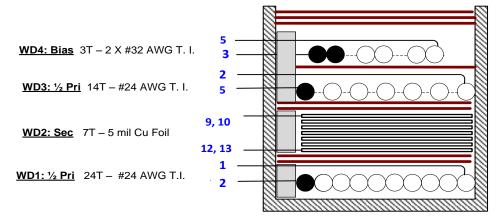


Figure 7 – Transformer Build Diagram.

7.1.5 Winding Instructions

Winding	Place the bobbin item [2] on the mandrel with pins on the left side.
preparation	Apply margin tape item [9] on pin side of bobbin. Match WD1 height.
WD1 Starting on pin 2, wind 24 turns of triple insulated wire item [3] in 1 layer, and	
(¹ / ₂ Primary)	on pin 1.
Insulation	Apply 2 layers of tape item [8].
Margin	Apply margin tape item [10] on pin side of bobbin. Match WD2 height.
WD2 (Secondary) Using items [5], [6], [7], construct a cuffed foil assembly 348 mm (13.7") lon Figure 3. Starting at pins 12 and 13, wind 7 turns of foil, finishing at pins 9 an Secure foil using tape item [8].	
Insulation Apply 2 layers of tape item [8].	
Margin	Apply margin tape item [10] on pin side of bobbin. Match WD3 & 4 height.
WD3 (½ Primary)	Starting on pin 2, wind 14 turns of triple insulated wire item [3] in 1 layer, and finish on pin 1. Secure this winding with 1 layer of tape item [9].
WD4 (Bias) Starting at pin 3, wind 3 bifilar turns of triple insulated wire [4], finishing on pin 5	
Finish Wrap	Apply 3 layers of tape item [8].
AssemblyRemove pins 4, 8, 11, and 14. Cut pin 2 short. Assemble and secure core halves. Dip varnish [11].	



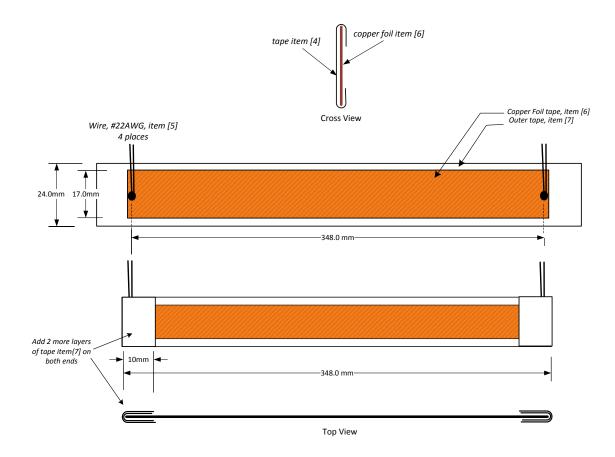


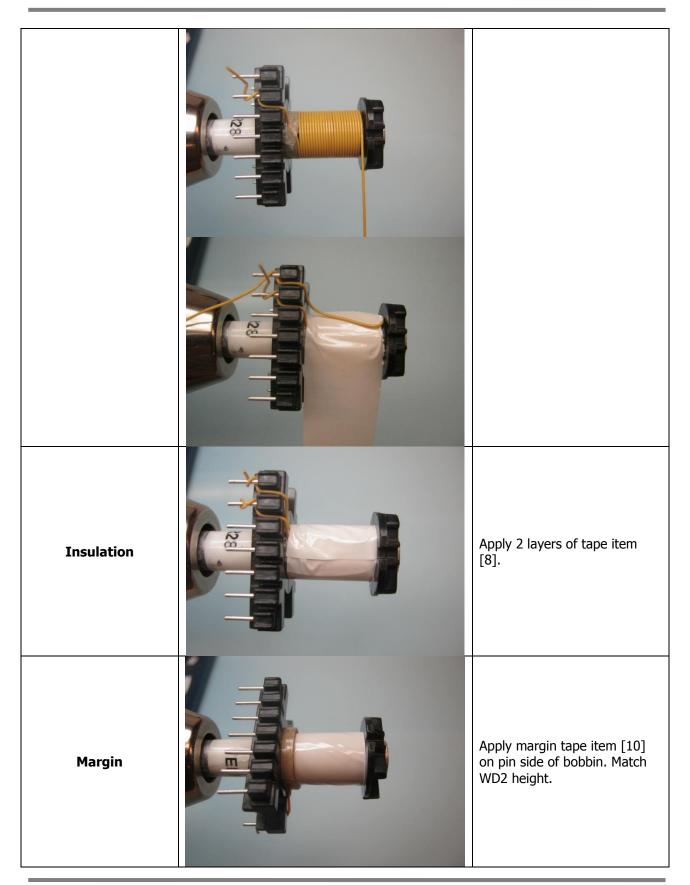
Figure 8 – Main Transformer Output Foil Design.



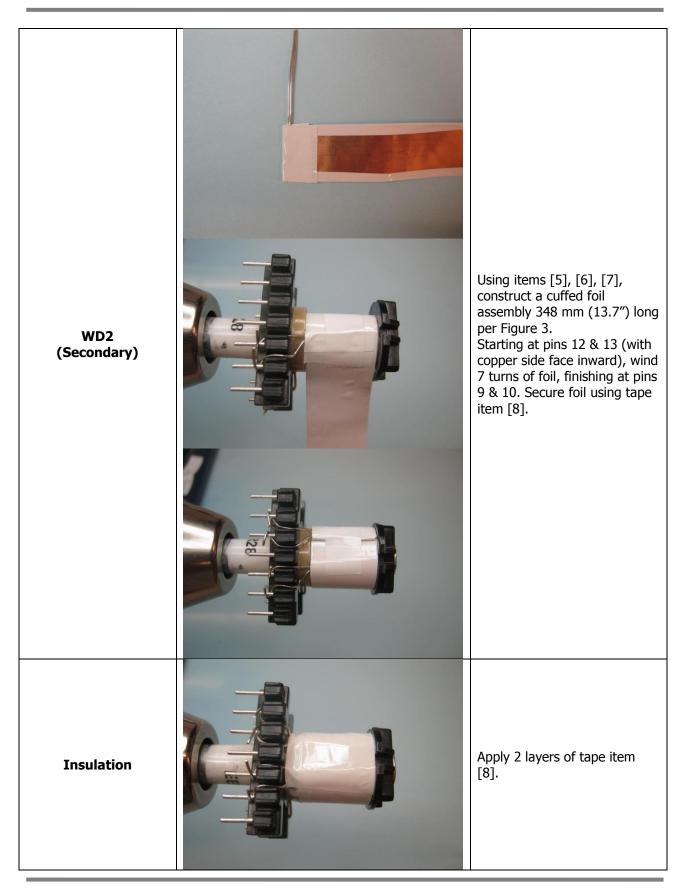
7.1.6 Winding Illustrations

Winding Preparation	Place the bobbin item [2] on the mandrel with pins on the left side. Apply margin tape item [9] on pin side of bobbin. Match WD1 height.
WD1 (½ Primary)	Starting on pin 2, wind 24 turns of triple insulated wire item [3] in 1 layer, and finish on pin 1.

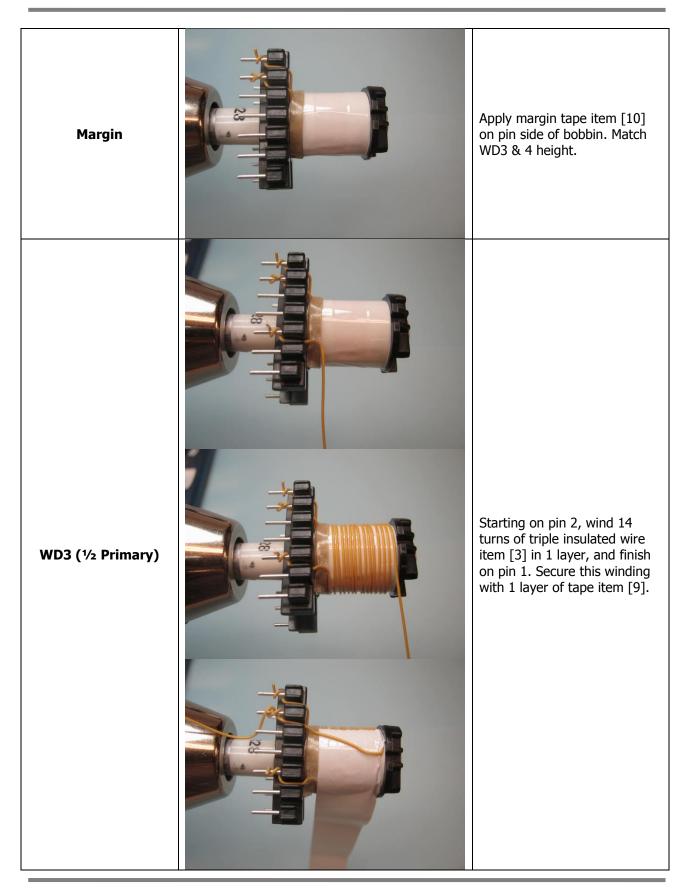








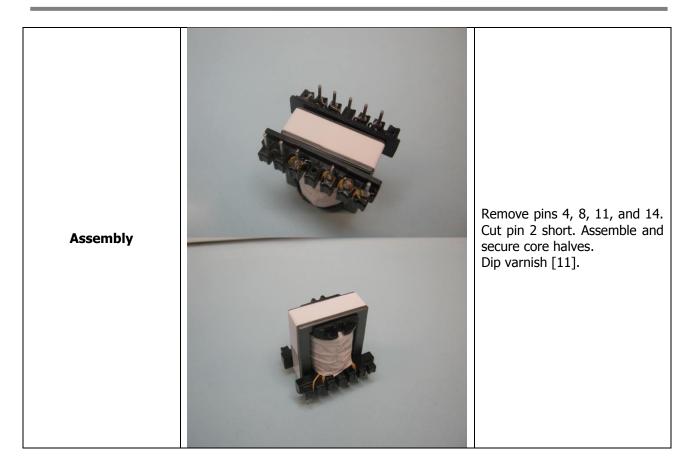






WD4 (Bias)	Starting at pin 3, wind 3 bifilar turns of triple insulated wire [4], finish on pin 5.
Finish Wrap	Apply 3 layers of tape item [8].







7.2 Standby Transformer Specification

7.2.1 Electrical Diagram

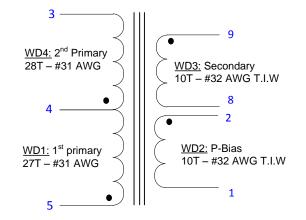


Figure 9 – Transformer Electrical Diagram.

7.2.2 Electrical Specifications

Electrical Strength 1 second, 60 Hz, from pins 1-5 to 6-10.		3000 VAC
Primary Inductance	Pins 3 & 5 all other windings open, measured at 100 kHz, 0.4 V_{RMS} .	300 μH ±10%
Resonant Frequency	Pins 3 & 5, all other windings open.	6 00 kHz (Min.)
Primary Leakage Inductance	Pins 3 & 5, with pins 1, 2, 8, 9 shorted, measured at 100 kHz, 0.4 V_{RMS} .	8 μH (Max.)

7.2.3 *Material List*

Item	Description
[1]	Core: EF12.6, TDK PC44 material, or equivalent.
	Gap for inductance coefficient (A_L) of 99 nH/T ² .
[2]	Bobbin, EF12.6, Horizontal, 9 pins (5/4) PI P/N 22-1058-00. Feryster EF12.6-K-H-9P-P1212
	or equivalent.
[3]	Tape, Polyester film, 3M 1350F-1 or equivalent, 7.4 mm wide.
[4]	Wire, Magnet #31 AWG, solderable double coated.
[5]	Wire, Triple Insulated, Furukawa TEX-E or equivalent, #32 AWG.
[6]	Transformer Varnish, Dolph BC-359 or equivalent.



7.2.4 Build Diagram

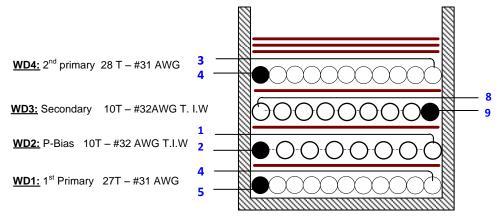


Figure 10 – Transformer Build Diagram

7.2.5 Winding Instructions

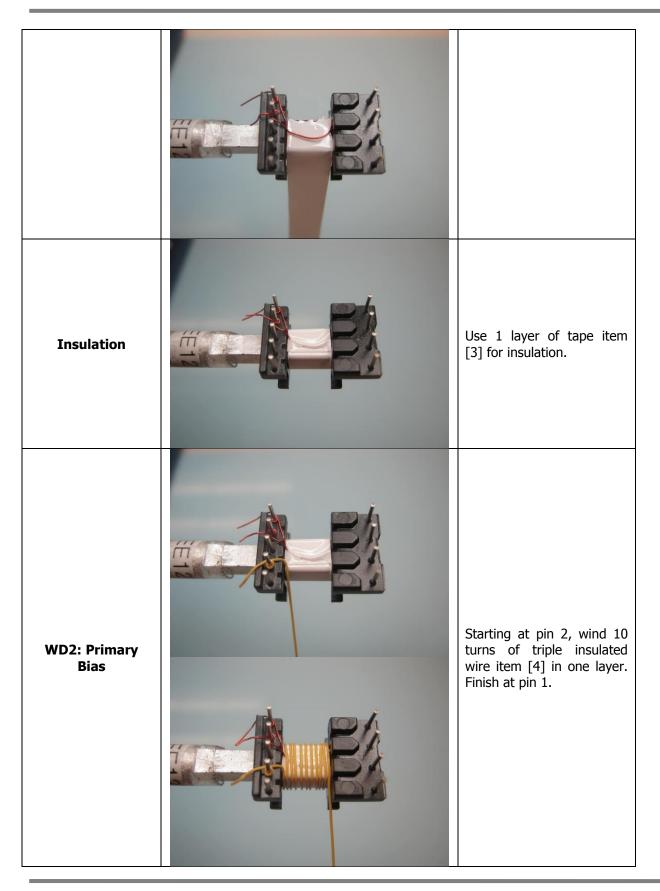
General Note	For the purpose of these instructions, bobbin is oriented on winder such that pins 1-5 are on the left side (see illustration). Winding direction as shown is clockwise.		
WD1: 1 st Primary	Starting at pin 5, wind 27 turns of wire item [4] in 1 layer. Finish at pin 4.		
Insulation	Use 1 layer of tape item [3] for insulation.		
WD2: Primary Bias	Starting at pin 2, wind 10 turns of triple insulated wire item [4] in one layer. Finish at pin 1.		
Insulation	Use 1 layer of tape item [3] for insulation.		
WD3: Secondary	Starting at pin 9, wind 10 turns of triple insulated wire item [4] in one layer. Finish at pin 8.		
Insulation	Use 1 layer of tape item [3] for insulation.		
WD4: 2 nd Primary	Starting at pin 4, wind 28 turns of wire item [4] in 1 layer. Finish at in 3.		
Insulation	Use 3 layers of tape item [3] to secure the windings.		
Assembly	Grind core halves for specified primary inductance, and secure core halves with tape. Remove pins 6 & 7, cut pin 4 short. Dip varnish item [6].		



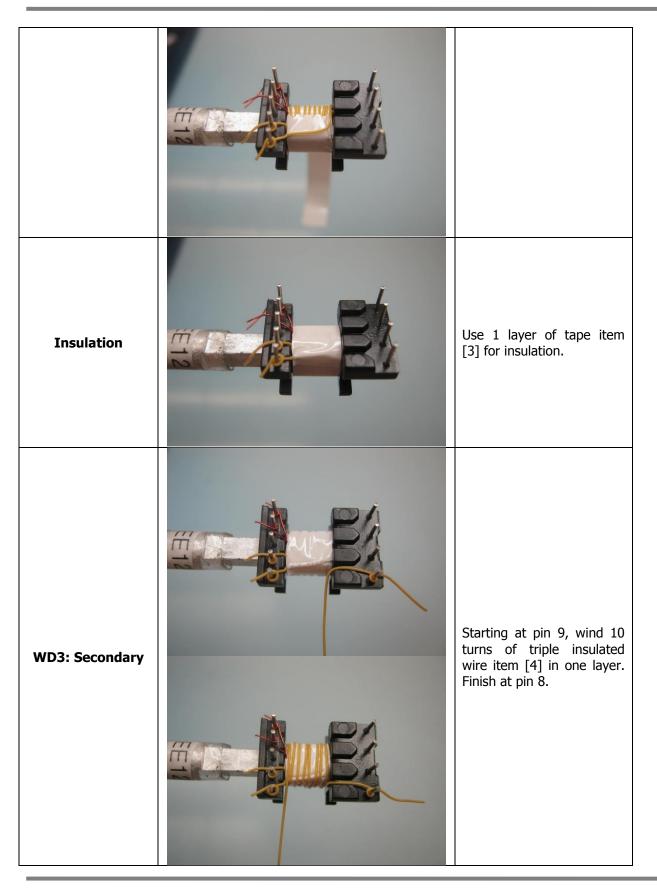
7.2.6 Transformer Illustrations

General Note	For the purpose of these instructions, bobbin is oriented on winder such that pins 1-5 are on the left side (see illustration). Winding direction as shown is clockwise.
WD1: 1 st Primary	Starting at pin 5, wind 27 turns of wire item [4] in 1 layer. Finish at pin 4.

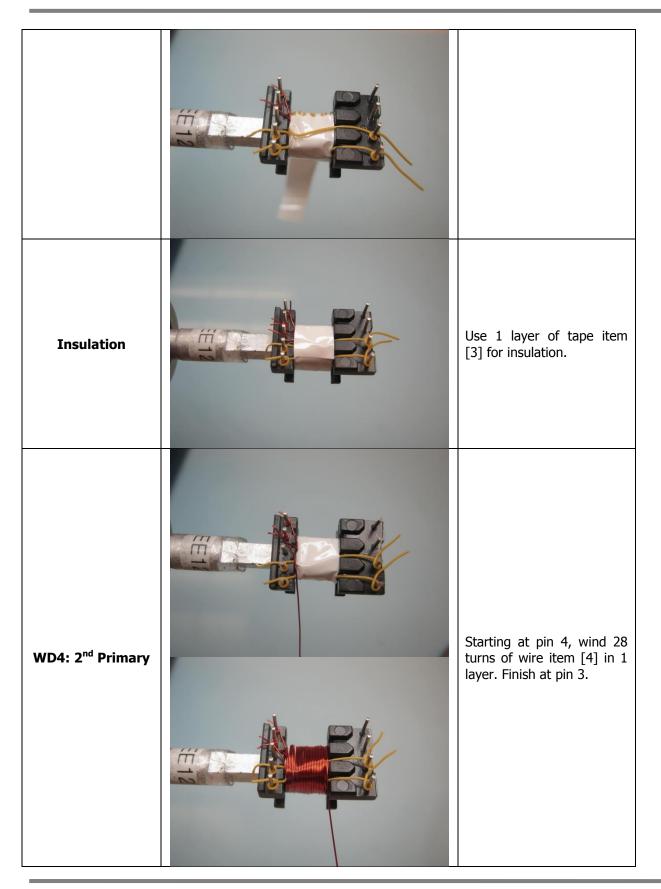


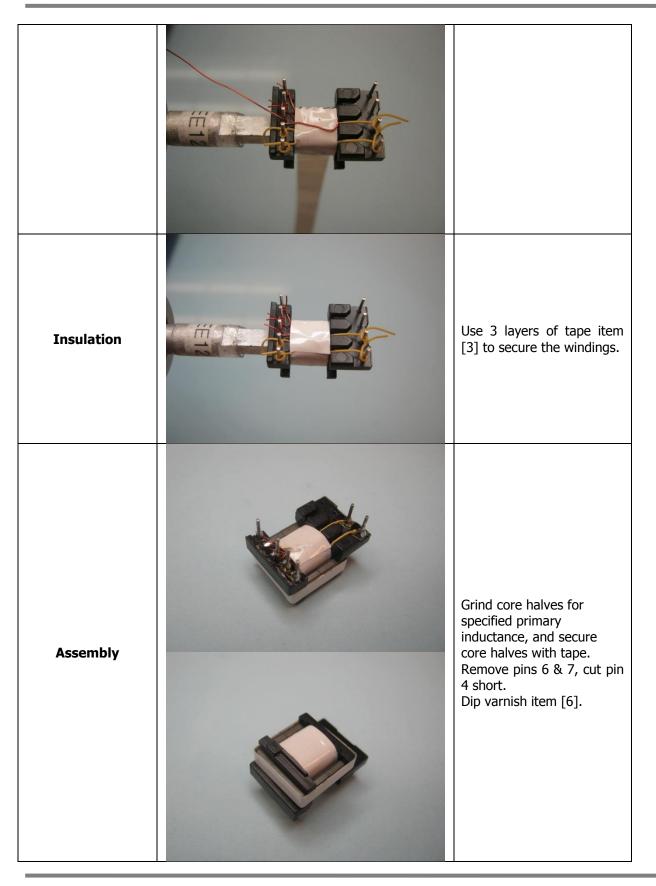








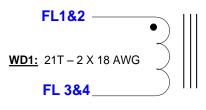






7.3 Main Output Choke

7.3.1 *Schematic*



Inductance - 41 uH +/- 15%

Figure 11 – Output Choke Schematic.

7.3.2 Material List

Item	Description
[1]	Core: Powdered Iron Toroid, Micrometals T106-52 or equivalent.
[4]	Wire, Magnet, 18 AWG, solderable double coated.

7.3.3 Winding Illustration



Figure 12 – Finished Output Choke.



8 Main/Standby Converter Design Spreadsheet

The main transformer design shown in this spreadsheet was refined by measuring the actual minimum B+ value at 90 VAC, 100% load (measured at the bottom of the ripple trough) and entering it as the VMIN value in the "Input Voltage and UV/OV" section of the spreadsheet.

HiperTFS2_Two- switch_Forward_041114; Rev.2.0; Copyright Power Integrations 2013	INPUT	INFO	OUTPUT	UNIT	HiperTFS2_041114_Rev2-0.xls; Two-switch Forward Transformer Design Spreadsheet
Hiper-TFS MAIN OUTPUT (TWO OUTPUT VOLTAGE AND CURRE		VARD STA	GE)		
VMAIN	23.00		23.00	V	Main output voltage
IMAIN	8.00		8.00	A	Main output voltage Main output current
	0.00				Output2 voltage - enter zero or leave
VOUT2			0.00	V	blank if none
IOUT2			0.00	А	Output2 current - enter zero or leave blank if none
Post Regulated Output					
Post Regulator	NONE		NONE		Select post regulator from Mag-Amp, Buck, or NONE
V_SOURCE	NONE		NONE	v	Select source of input voltage for post regulator. Enter None if Post regulator not used.
VOUT3			0.00	v	Enter post regulator output voltage. Enter zero or leave blank if none
IOUT3			0.00	A	Enter post regulator output current. Enter zero or leave blank if none
n_PR			1.00		Enter post regulator efficiency (Buck only)
Coupled Inductor (Low Power) derived output				
VOUT4			0.00	v	Output choke derived (low power) output voltage (typically -12 V)
IOUT4			0.00	A	Output choke derived (low power) output current
System Power					· ·
POUT(Main)			184.0	W	Total output power (Main converter)
POUT_PEAK(Main)	184.0		184.0	w	Peak Output power (Main converter). If there is no peak power requirement enter value equal to continuous power
POUT(Standby)			3.3	w	Continuous output power from Standby power supply
POUT_PEAK(Standby)			3.3	w	Peak output power from Standby section below
POUT(System Total)			187.3	w	Total system continuous output power
POUT_PEAK(System Total)			187.3	W	Total system peak output power
INPUT VOLTAGE AND UV/OV					
CIN_MIN			141	uF	Minimum Input Capacitance to meet holdup time. To increase CMIN, increase T_HOLDUP
T_HOLDUP			20.0	ms	Holdup time
CIN_ACTUAL	270		270	uF	Select Actual Bulk Capacitor
CIN_ESR			0.27	Ω	Bulk capacitor ESR
IRMS_CIN			0.88	A	RMS current through bulk capacitor
PLOSS_CIN			0.21	W	Bulk capacitor ESR losses
VMIN	205		205	v	Minimum input voltage to guarantee output regulation at full load
VNOM	322		322	V	Nominal input voltage



VMAX	370	370	V	Maximum DC input voltage
RR	370	3,32	MΩ	R pin resistor
RL		3.32	ΜΩ	Line Sense resistor value (L-pin) - goal seek (VUV OFF) for std 1% resistor series
UV and OV thresholds				
Clamp Section				
Clamp Selection	CLAMP TO GND			Select either "CLAMP TO RAIL" (default) or "CLAMP TO GND"
VCLAMP		530	V	Asymmetric Clamp Zener Voltage
VDSOP		530	v	Estimated Maximum Hiper-TFS Drain voltage (at VOVOFF_MAX)
DUTY CYCLE VALUES (REG	ULATION)			
DVMIN		0.68		Duty cycle at minimum DC input voltage
DVNOM_GOAL		0.44		Target duty cycle at nominal input voltage (VNOM)
DVNOM		0.43		Duty cycle at nominal DC input voltage
DVMAX		0.37		Duty cycle at maximum DC input voltage
DOVOFF MIN		0.35		Duty cycle at over-voltage DC input voltage (DOVOFF_MIN)
Maximum Duty Cycle value	es			
DMAX_UVOFF_MIN		0.78		Max duty cycle clamp at VUVOFF_MIN
DMAX_VMIN		0.73		Max duty clamp cycle at VMIN
DMAX_VNOM		0.56		Max duty clamp cycle at VNOM
DMAX VMAX		0.49		Max duty clamp cycle at VMAX
DMAX_OVOFFMIN		0.46		Max duty clamp cycle at VOVOFF_MAX
DEVICE VARIABLES	1 1			
Device	TFS7704	TFS7704		Selected HiperTFS device
Select Frequency mode	132	132	kHz	Select Frequency mode.
ILIMIT_MIN		3.35	A	Device current limit (Minimum)
 ILIMIT_TYP		3.60	Α	Device current limit (Typical)
ILIMIT_MAX		3.85	A	Device current limit (Maximum)
fSMIN		124,000	Hz	Device switching frequency (Minimum)
fS		132,000	Hz	Device switching frequency (Typical)
fSMAX		140,000	Hz	Device switching frequency (Maximum)
KI	1.0	1.0		Select Current limit factor (KI=1.0 for default ILIMIT, or select KI=0.9 or KI=0.7)
R(FB)		232	kΩ	Feedback Pin Resistor value
ILIMIT SELECT		3.35	А	Selected current limit
RDS(ON)		4.20	Ω	Sum of Rds(on) of high and low-side MOSFETs at 100°C
VDS		5.26	V	HiperTFS full-load average on-state Drain to Source Voltage (sum for both MOSFETs)
Main MOSFET losses				
MAIN TRANSFORMER				
Transformer core selection				
Core Type	EER28L	EER28L		Selected core type
AE		0.814	cm^2	Core effective cross sectional area
LE		7.55	cm	Core Effective Path Length
AL		2520	nH/T^2	Ungapped Core Effective Inductance
BW		21.8	mm	Bobbin Physical Winding Width
	1			
B_HT		4.33	mm	Height of bobbin (to calculate fit)
B_HT B_WA				
	1.50	4.33 0.94 1.5	mm cm^2 mm	Height of bobbin (to calculate fit) Bobbin Winding area Bobbin safety margin tape width (2 *



					M = Total Margin)
Primary Inductance					
LMAG_MAX			7.1	mH	Max LMAG to hit min zero-load resonant frequency, calculated from C_PRI. Do not exceed.
LMAG	3.4		3.4	mH	Actual magnetizing inductance (measured) of transformer
GAP		Info	0.00	mm	Info, zero gap at 132 kHz may cause hi-side driver pulse-skipping. If unacceptable, Decrease LMAG (add gap) or use high side bias winding
FRES_SYS	173		173	kHz	Total XFMR + system resonant frequency; enter value along with actual LMAG
C_SYS			249	pF	Estimated total XFMR + Sys parasitic cap reflected to primary, calc'd from LMAG and FRES
Diode Vf Selection					
Turns	7.0		_	T .	
NMAIN NS2	7.0		7	turns	Main rounded turns 2nd output number of turns
1102			N/A	turns	
VOUT2 ACTUAL			0.0	v	Approximate Output2 voltage with NS2 = 0 turns (AC stacked secondary). VDMAIN and VDOUT2 affect this.
NP			38	turns	Primary rounded turns. NMAIN and DVNOM_GOAL affect this.
HI SIDE BIAS WINDING (optional)	Yes		Yes		Can be used to eliminate pulse skipping at light load 132 kHz when zero transformer gap; better efficiency than adding gap
VBIAS			17.0	v	DC bias voltage from main transformer optional aux winding
NBIAS			3	turns	VBias rounded turns
VBIAS_ACTUAL			15.5	V	Approximate Forward Bias Winding Voltage at VMIN with NB = 3 turns
Flux calculations					<u> </u>
BM_MAX			2062	Gauss	Peak positive flux density at nominal switching frequency
ВМ РК-РК			3124	Gauss	Peak-peak flux density at nominal conditions. Used to calculate core losses
BP_MAX			2928	Gauss	Max transient positive flux density at Vmax (limited by DVMAX clamp)
BP PK-PK			4437	Gauss	Max transient peak-peak flux density at Vmax (limited by DVMAX clamp)
					de vindx (inniced by bvi i/v(clamp)
TRANSFORMER LOSSES AND	FIT ESTIMATE				
Core loss	-		2007		
Core loss Core material	FIT ESTIMATE PC95		PC95		Core material
Core loss Core material core_loss_multiplier	-		23.97		Core material Core Loss coefficient
Core loss Core material core_loss_multiplier f_coeff	-		23.97 1.56		Core material Core Loss coefficient Core Loss Frequency co-efficient
Core loss Core material core_loss_multiplier f_coeff BAC_coeff	-		23.97 1.56 2.89		Core material Core Loss coefficient Core Loss Frequency co-efficient Core Loss AC flux density co-efficient
Core loss Core material core_loss_multiplier f_coeff BAC_coeff specific core loss	-		23.97 1.56 2.89 225	mW/cc	Core material Core Loss coefficient Core Loss Frequency co-efficient Core Loss AC flux density co-efficient Core loss per unit volume
Core loss Core material core_loss_multiplier f_coeff BAC_coeff specific core loss core volume	-		23.97 1.56 2.89 225 6.15	cm^3	Core material Core Loss coefficient Core Loss Frequency co-efficient Core Loss AC flux density co-efficient Core loss per unit volume Volume of core
Core loss Core material core_loss_multiplier f_coeff BAC_coeff specific core loss core volume core loss	PC95		23.97 1.56 2.89 225		Core material Core Loss coefficient Core Loss Frequency co-efficient Core Loss AC flux density co-efficient Core loss per unit volume
Core loss Core material core_loss_multiplier f_coeff BAC_coeff specific core loss core volume	PC95		23.97 1.56 2.89 225 6.15	cm^3	Core material Core Loss coefficient Core Loss Frequency co-efficient Core Loss AC flux density co-efficient Core loss per unit volume Volume of core Core loss Transformer primary layers (split
Core loss Core material core_loss_multiplier f_coeff BAC_coeff specific core loss core volume core loss Primary Winding Fit and losse L	PC95		23.97 1.56 2.89 225 6.15 1.39 3.0	cm^3 W layers	Core material Core Loss coefficient Core Loss Frequency co-efficient Core Loss AC flux density co-efficient Core loss per unit volume Volume of core Core loss Transformer primary layers (split primary recommended)
Core loss Core material core_loss_multiplier f_coeff BAC_coeff specific core loss core volume core loss Primary Winding Fit and losse	PC95		23.97 1.56 2.89 225 6.15 1.39	cm^3 W	Core material Core Loss coefficient Core Loss Frequency co-efficient Core Loss AC flux density co-efficient Core loss per unit volume Volume of core Core loss Transformer primary layers (split



	r r			
DCR_PRI		218	mΩ	DC resistance of primary winding
PCOND_PRI		0.26	W	Conduction loss in primary winding
FILL_PRI		8	%	Fill factor (primary only)
Secondary Winding 1 (lower	winding when AC stac			Constitution of the sector of
VOUT		23.0	V	Specified voltage for this winding
NS1		7.0	turns	Number of turns
IRMS_SEC1		6.4	A	RMS current through winding
Foil/Wire	FOIL	FOIL	foil/wire	Select FOIL or WIRE for winding
OD/Thickness		0.125	mm	Wire diameter or Foil thickness
FILAR_SEC1		N/A	strands	Number of parallel strands (wire selection only)
SEC1_WIDTH		18.00	mm	Foil Width (Applicable if FOIL winding used)
SEC1_MLT		5.22	cm	Mean length per turn
DCR_SEC1		3.59	mΩ	DC resistance of secondary winding
PCOND_SEC1		0.15	W	Conduction loss in secondary winding
FILL_SEC1		17	%	Fill factor (secondary 1 only)
Secondary Winding 2 (upper	winding when AC stac	ked)		
VOUT		0.0	V	Specified voltage for this winding
NS2		0.0	turns	Number of turns
IRMS_SEC2		0.0	Α	RMS current through winding
Foil/Wire	FOIL	FOIL	foil/wire	Select FOIL or WIRE for winding
OD/Thickness		0.125	mm	Wire diameter or Foil thickness
FILAR_SEC2		N/A	strands	Number of parallel strands (wire selection only)
SEC2_WIDTH		18.0	mm	Foil Width (Applicable if FOIL winding used)
SEC2_MLT		5.22	cm	Mean length per turn
DCR_SEC2		0.00	mΩ	DC resistance of secondary winding
PCOND_SEC2		0.00	W	Conduction loss in secondary winding
FILL_SEC2		0	%	Fill factor (secondary 1 only)
Fill Factor and losses of main	n transformer			
FILL_TOTAL		25	%	Total transformer fill factor
TOTAL_CU_LOSS		0.40	W	Total copper losses in transformer
TOTAL_CORE_LOSS		1.39	Ŵ	Total core losses in transformer
TOTAL_TRF_LOSS		1.79	Ŵ	Total losses in transformer
CURRENT WAVESHAPE PARA	METERS	1.75		
IP		2.10	A	Peak primary current at Full Load, VNOM
IP_PEAK		2.10	А	Peak primary current at Peak Load and VNOM
IPRMS(NOM)		1.09	А	Primary RMS current at Full Load, VNOM
IMAG		0.30	А	Peak magnetizing current at VMIN
OUTPUT INDUCTOR				
KDI_ACTUAL		0.45		Current ripple factor of combined Main and Output2 outputs
Turns				
POWDER TURNS MULTIPLIER	3.00	3.0		Powder only. Multiplier factor between main number of turns in transformer and inductor (default value = 3 for 66kHz or 4 for 132kHz).
NMAIN_INDUCTOR		21.0	turns	Main output inductor number of turns - affected by powder turns multiplier or ferrite Target BM
NOUT2_INDUCTOR			turns	Output 2 inductor number of turns
NOUT4_INDUCTOR		N/A	turns	Output 4 number of turns (low power)
Inductance and flux				
LMAIN_ACTUAL		31.3	uH	Estimated inductance of main output at full load



					output at full load
BM_IND			1926	gauss	DC component of flux density
BAC_IND			426	gauss	AC component of flux density
Core Selection	· · ·				· · ·
Core Type	Pow Iron		Pow Iron		Select core type
Core	T106- 52(0.D)=26.9		T106- 52(O.D)=26.9		Output choke core size - verify on bench
AE	52(0.0)=20.9		65.9	mm^2	Core Effective Cross Sectional Area
LE			64.9	mm	Core Effective Path Length
AL			95.0	nH/T^2	Ungapped Core Effective Inductance
BW			45.6	mm	Bobbin Physical Winding Width
VE			4280	mm^3	Volume of core
Powder cores (Sendust and	Powdered Iron) Cores	5	4200	11111 3	Volume of core
		•			Relative permeability of material at 0
MUR			75		bias
Н			27.5	AT/cm	Magnetic field strength
MUR_RATIO			0.75		Ratio of permeability at full load divided by initial permeability
LMAIN_0bias			41.9	uH	Estimated inductance of main output with 0 DC bias
Ferrite Cores					
LG			N/A	mm	Gap length of inductor cores
Target BM			N/A	Gauss	Target maximum flux density
Choke wires					
Total number of layers			0.82	layers	Total number of layers for chosen toroid
IRMS_MAIN			8.01	А	RMS current through main inductor windings
IRMS_AUX			0.00	А	RMS current through aux winding
AWG_MAIN			20	AWG	Main inductor winding wire gauge
OD_MAIN			0.88	mm	Main winding wire gauge outer diameter
FILAR_MAIN			2	strands	Number of parallel strands for main output
RDC_MAIN			12.82	mΩ	Resistance of wire for main inductor winding
AC Resistance Ratio (Main)			1.97		Ratio of total resistance (AC + DC) to the DC resistance (using Dowell curves)
CMA_MAIN			255	CMA	Cir mils per amp for main inductor winding
J_MAIN			13.20	A/mm^2	Current density in main inductor winding
AWG_AUX			0	AWG	Aux winding wire gauge
OD_AUX			N/A	mm	Auxiliary winding wire gauge outer diameter
FILAR_AUX			2	strands	Number of parallel strands for aux output
RDC_AUX			0.00	mΩ	Resistance of wire for aux inductor winding
AC Resistance Ratio (Aux)			0.00		Ratio of total resistance (AC + DC) to the DC resistance (using Dowell curves)
CMA_AUX		Info	0	CMA	III Info. Low CMA may cause overheating. Verify acceptable temperature rise
J_AUX			0.00	A/mm^2	Current density in auxiliary winding
Choke Losses					
PCOPPER_MAIN			0.82	W	Copper loss in main inductor winding
PCOPPER_AUX			0.00	W	Copper loss in aux inductor windings
PCORE			3.87	W	Total core loss
PTOTAL_IND			4.69	W	Total losses in output choke



SECONDARY OUTPUT DIO	DE PARAMETERS			
Main Output				
ISFWDRMS		6.40	А	Full load forward diode RMS current at nominal input voltage
ISCATCHRMS		7.40	А	Freewheeling diode RMS current at nominal input voltage
IDAVMAINF		5.44	А	Worst case average current of forward rectifier at VMIN (single device rating)
IDAVMAINC		5.02	A	Worst case average current of freewheeling diode at VMAX(single device rating)
IRMSMAIN		1.03	А	Maximum RMS current, Main output capacitor
PD_LOSS_MAIN		4.00	W	Conduction loss of forward diode
Second Output				
ISFWD2RMS		0.00	А	Full load forward diode RMS current at nominal input voltage
ISCATCH2RMS		0.00	А	Freewheeling diode RMS current at nominal input voltage
IDAVOUT2F		0.00	А	Worst case average current of forward rectifier at VMIN (single device rating)
IDAVOUT2C		0.00	A	Worst case average current of freewheeling diode at VMAX(single device rating)
IRMSOUT2		0.00	А	Maximum RMS current, Main output capacitor
PD_LOSS_OUT2		0.00	W	Conduction loss of forward diode
Diode Derating				
VPIVMAINF	0.80	122.0	V	Main Forward Diode peak-inverse voltage (at VDSOP), including derating
VPIVMAINC	0.80	85.2	v	Main Catch Diode peak-inverse voltage (at VOVOFF_MAX), including derating
VPIVOUT2F	1.00	0.0	V	Output2 Forward Diode peak-inverse voltage (at VDSOP), including derating
VPIVOUT2C	1.00	0.0	v	Output2 Catch Diode peak-inverse voltage (at VOVOFF_MAX), including derating
VPIVB	1.00	41.8	V	Bias output rectifier peak-inverse voltage (at VDSOP), including derating
Hiper-TFS STANDBY SECT	ION (FLYBACK STAGE)			
ENTER APPLICATION VAR	IABLES			
VACMIN		85	V	Minimum AC Input Voltage
VACMAX		265	V	Maximum AC Input Voltage
fL III	12.0	50	Hz	AC Mains Frequency
VO_SB	12.0	12.0	V	Output Voltage (at continuous power) Power Supply Output Current
IO_SB	0.25	0.25	Α	(corresponding to peak power)
IO_SB_PK		0.25	A	Peak output current
POUT_SB		3.00	W	Continuous Output Power
POUT_SB_TOTAL		3.34	W	Total Standby power (Includes Bias winding power)
POUT_SB_PK		3.34	W	Peak Standby Output Power
n		0.70		Efficiency Estimate at output terminals. Under 0.7 if no better data available
Z		0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC		3.00	ms	Bridge Rectifier Conduction Time Estimate



ENTER Hiper-TFS STANDE	BY VARIABLES			
Select Current Limit	LOW	Low current Limit		Enter "LOW" for low current limit, "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications)
ILIM_MIN		0.47	A	Minimum Current Limit
ILIM_TYP		0.50	А	Typical Current Limit
ILIM_MAX		0.54	A	Maximum Current Limit
R(EN)		NONE	kΩ	Enable pin resistor
fSmin		124,000	Hz	Minimum Device Switching Frequency
I^2fmin		29.7	A^2kHz	I^2f (product of current limit squared and frequency is trimmed for tighter tolerance)
VOR		100	V	Reflected Output Voltage (VOR < 135 V Recommended)
VDS		10.0	V	Hiper-TFS Standby On State Drain to Source Voltage
VD_SB		0.7	V	Output Winding Diode Forward Voltage Drop
KP		4.03		Ripple to Peak Current Ratio (KP < 6)
KP_TRANSIENT		3.72		Transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25
ENTER BIAS WINDING VA	-	·		
VB	17.00	17.0	V	Bias Winding Voltage
IB		20.0	mA	Bias winding Load current
PB		0.34	W	Bias winding power
VDB		0.70	V	Bias Winding Diode Forward Voltage Drop
NB		9.8	turns	Bias Winding Number of Turns
VZOV		23	v	Over Voltage Protection zener diode voltage.
UVLO VARIABLES			•	•
RLS		3.32	MΩ	Line sense resistor (from Main converter section)
V_UV_ACTUAL		85	V	Typical DC start-up voltage
ENTER TRANSFORMER CO	DRE/CONSTRUCTION VAR	IABLES		
Core Type	Custom	Custom		Enter Transformer Core
AE	0.12	0.12	cm^2	Core Effective Cross Sectional Area
LE	2.96	2.96	cm	Core Effective Path Length
AL	850.00	850	nH/T^2	Ungapped Core Effective Inductance
BW	7.50	7.5	, mm	Bobbin Physical Winding Width
М		0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L		3		Number of Primary Layers
NS_SB	7	7		Number of Secondary Turns
DC INPUT VOLTAGE PARA			•	· · · · ·
VMIN_SB		118	V	Minimum DC Input Voltage
VMAX_SB		375	V	Maximum DC Input Voltage
CURRENT WAVEFORM SH	APE PARAMETERS		•	· · · · · · ·
DMAX_SB		0.17		Duty Ratio at full load, minimum primary inductance and minimum input voltage
IAVG		0.04	A	Average Primary Current
IP_SB		0.47	А	Minimum Peak Primary Current
IR_SB		0.47	А	Primary Ripple Current
 IRMS_SB		0.13	A	Primary RMS Current
TRANSFORMER PRIMARY	DESIGN PARAMETERS		•	
LP_SB		300	uH	Typical Primary Inductance. +/- 10% to ensure a minimum primary inductance of 273 uH
			•	•



LP_TOLERANCE		10	%	Primary inductance tolerance
NP_SB		55	turns	Primary Winding Number of Turns
ALG		99	nH/T^2	Gapped Core Effective Inductance
ВМ		2430	Gauss	Maximum Operating Flux Density, BM<3000 is recommended
BAC		1215	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur		1668		Relative Permeability of Ungapped Core
LG		0.13	mm	Gap Length (Lg > 0.1 mm)
BWE		22.5	mm	Effective Bobbin Width
OD		0.41	mm	Maximum Primary Wire Diameter including insulation
INS		0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA		0.35	mm	Bare conductor diameter
AWG		28	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
СМ		161	Cmils	Bare conductor effective area in circular mils
СМА	Info	1253	Cmils/Amp	CAN DECREASE CMA < 500 (decrease L (primary layers), increase NS,use smaller Core)
TRANSFORMER SECONDARY DESIG	N PARAMETERS			
Lumped parameters				
ISP		3.7	А	Peak Secondary Current
ISRMS		1.10	А	Secondary RMS Current
IRIPPLE		1.07	A	Output Capacitor RMS Ripple Current
CMS		220	Cmils	Secondary Bare Conductor minimum circular mils
AWGS		26	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS				
VDRAIN		605	v	Maximum Drain Voltage Estimate (Assumes 20% zener clamp tolerance and an additional 10% temperature tolerance)
PIVS		60	V	Output Rectifier Maximum Peak Inverse Voltage
Forward DC-DC System efficiency				
P_MOSFET_MAIN_TOTAL		5.93	W	HiperTFS losses
P_XFMR_LOSS		1.8	W	Main transformer losses
P_MAIN_OUT_DIODE		4.0	W	Output diode losses
P_CIN_ESR		0.21	W	Bulk capacitor ESR losses
P_IND_MAIN		4.7	W	Output choke losses
OTHER_LOSSES		0.15	W	Other losses (includes PCB traces, clamp loss, magamp loss etc.)
EFFICIENCY_STDBY		70.0%		Estimated efficiency of flyback power supply
EFFICIENCY_MAIN		91.4%		Estimated Forward efficiency
EFFICIENCY_SYSTEM		91.0%		Estimated System efficiency (forward + standby)



9 Heat Sinks

9.1 *Primary Heat Sink*

9.1.1 Primary Heat Sink Sheet Metal

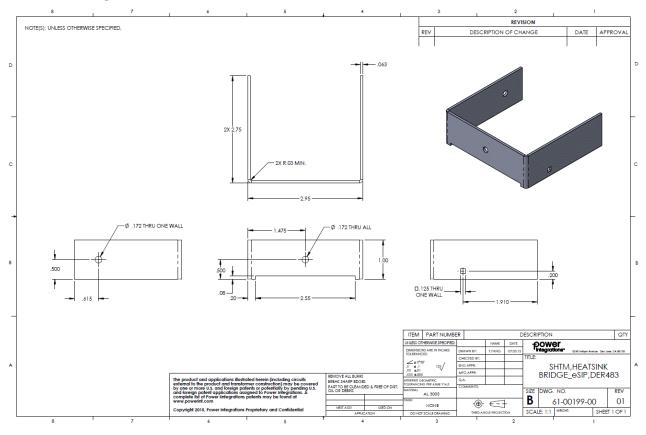
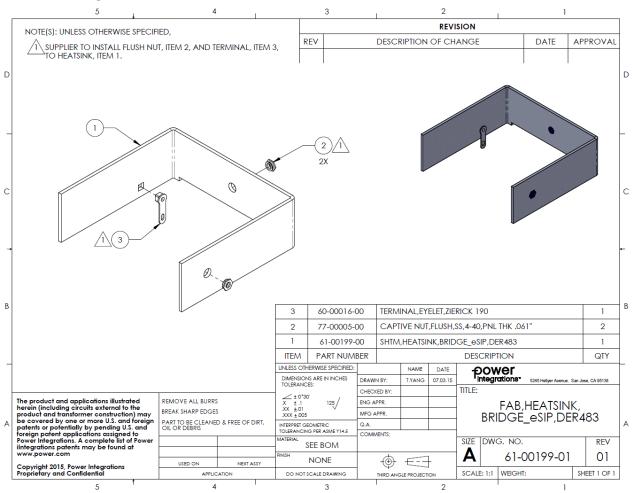


Figure 13 – Primary Heat Sink Sheet Metal Drawing.





9.1.2 Primary Heat Sink with Fasteners

Figure 14 – Finished Primary Heat Sink Drawing with Installed Fasteners.



9.1.3 Primary Heat Sink Assembly

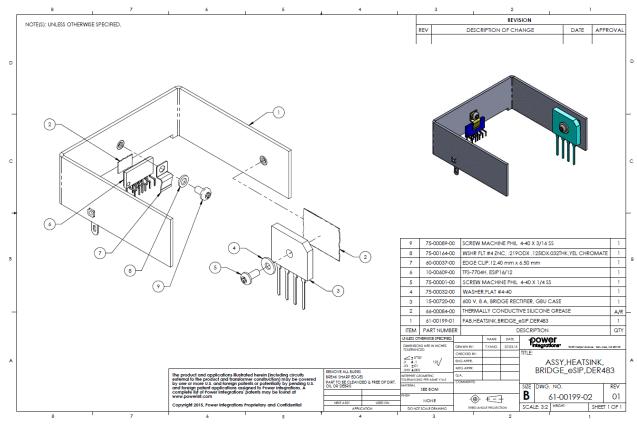


Figure 15 – Primary Heat Sink Assembly.



9.2 Secondary Heat Sink

9.2.1 Secondary Heat Sink Sheet Metal

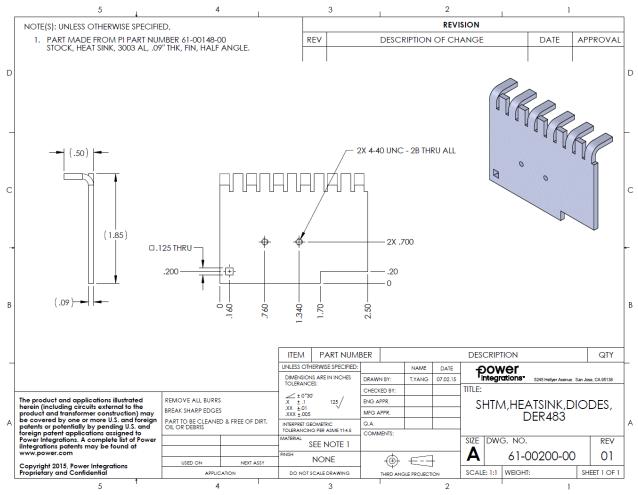
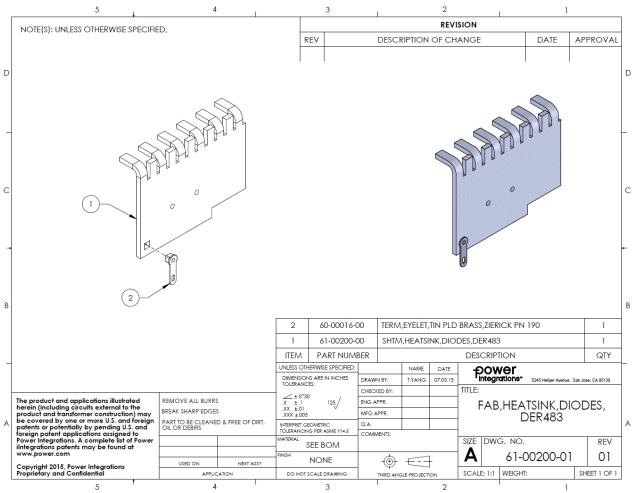


Figure 16 – Secondary Heat Sink Sheet Metal Drawing.





9.2.2 Secondary Heat Sink with Fasteners

Figure 17 – Finished Secondary Heat Sink with Installed Fasteners.



	5 +	4	1		3		I		2		I.	1			
	NOTE(S): UNLESS OTHERWISE SPECIFIEI	s): UNLESS OTHERWISE SPECIFIED, REVISION]					
				R	EV		DESCR	RIPTION	OF CH	ANGE		DATE	APPR	OVAL]
															1
D															
		20						/	20						-
	Ŧ							\bigtriangledown	R	NA					
			\sim							SID	5				
											200				L
		Ĺ									AS A	2			
	l	~ ~	Ť								¥				
		\geq													
С			4 .								\leq				С
	5 ^{2X}	1		$\overline{)}$											
		_										Ø			
		2	-00								-ul	g			
-		2X													+
		3													
	Ň	2X		5	75-00089-	-00	SCRE	W MAC	HINE PH	HL 4-40 X	3/16 SS			2	
в				4	75-00164-	-00	WSHR	RFLT #4	ZNC,.2	190DX.12	5IDX.032	THK,YEL CH	RMT	2	в
D				3	15-00914-	00	150V,	15A,SC	ΗΟΠΚΥ	,TO-220A	В			2	
				2	66-00084-	-00	THER/	MALLY (CONDU	CTIVE SILI	CONE G	REASE		A/R	
				1	61-00200-	01	FAB,H	IEATSIN	K,DIODI	ES,DER483	3			1	
				ITEM	PART NUM	BER				DESCR				QTY	Ļ
				DIMENSION	ERWISE SPECIFIED: AS ARE IN INCHES	DRAW	N BY:	NAME T.YANG	DATE 07.03.15		wer grations	5245 Hellyer Avenue	. San Jose. C	A 95138	
				TOLERANC			ED BY:			TITLE:					1
	The product and applications illustrated herein (including circuits external to the	REMOVE ALL BURRS BREAK SHARP EDGES		.X ±.1 .XX ±.01	125	ENG A				ASS	SY,HEA	ATSINK,E	IOD	ES,	
Α	product and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and	PART TO BE CLEANED OIL OR DEBRIS		INTERPRET GA	XXX ±.005 MFG TERPRET GEOMETRIC JLERANCING PER ASME Y14.5 TERIAL CON		MFG APPR.			-	E	DER483			A
	foreign patent applications assigned to Power Integrations. A complete list of Power	OIL OR DEBRIS		MATERIAL						SIZE DWG. NO.				REV	
	ilntegrations patents may be found at www.power.com			FINISH	SEE BOM		\$		1	A		00200-02		01	
	Copyright 2015, Power Integrations Proprietary and Confidential	USED ON APPLIC	NEXT ASSY			-	() ()		t ON	SCALE: 1:					-
l		4	a surger f		3	1	THIRD ANG	ALE PROJECTI	2			. 1	- OF ICC		1

9.2.3 Secondary Heat Sink Assembly

Figure 18 – Secondary Heat Sink Assembly.



10 Performance Data

All measurements were taken at room temperature and 60 Hz (input frequency) unless otherwise specified. Output voltage measurements were taken at the output connectors.

10.1 *Output Load Considerations for Testing a CV/CC Supply in Battery Charger Applications*

Since this power supply has a constant voltage/constant current output and normally operates in CC mode in its intended application (battery charging), some care must be taken in selecting the type/s of output load for testing.

The default setting for most electronic loads is constant current. This setting can be used in testing a CV/CC supply in the CV portion of its load range below the power supply current limit set point. Once the current limit of the DUT is reached, a constant current load will cause the output voltage of the DUT to immediately collapse to the minimum voltage capability of the electronic load.

To test a CV/CC supply in both its CV and CC regions (an example - obtaining a V-I characteristic curve that spans both the CV and CC regions of operation), an electronic load set for constant resistance can be used. However, in an application where the control loop is strongly affected by the output impedance, use of a CR load will give results for loop compensation that are overly optimistic and will likely oscillate when tested with an actual low impedance battery load.

For final characterization and tuning the output control loops, a constant voltage load should be used.

Having said this, many electronic loads incorporate a constant voltage setting, but the output impedance of the load in this setting may not be sufficiently low to successfully emulate a real-world battery (impedance on the order of tens of milliohms). Simulating this impedance can be crucial in properly setting the compensation of the current control loop in order to prevent oscillation in a real-life application.



10.2 *Efficiency*

To make this measurement, the supply was powered with an AC source. The figure shown includes the efficiency of the main forward stage combined with that of the standby/bias flyback supply.

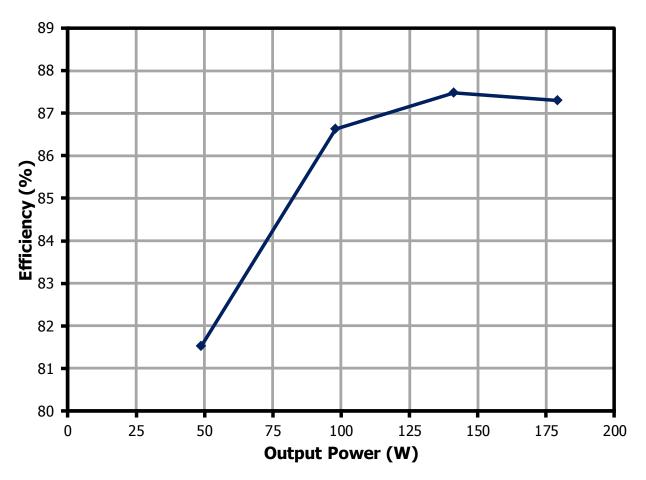


Figure 19 – Efficiency vs. Load, AC Input.



10.3 V-I Characteristic

The V-I characteristic showing the transition from constant voltage mode to constant current mode was measured using a Chroma electronic load set for constant resistance mode. This setting allows proper operation of the DUT in both CV and CC mode. The measurements cut off at ~5.5 V, as this is the minimum load voltage attainable by the electronic load in CR mode.



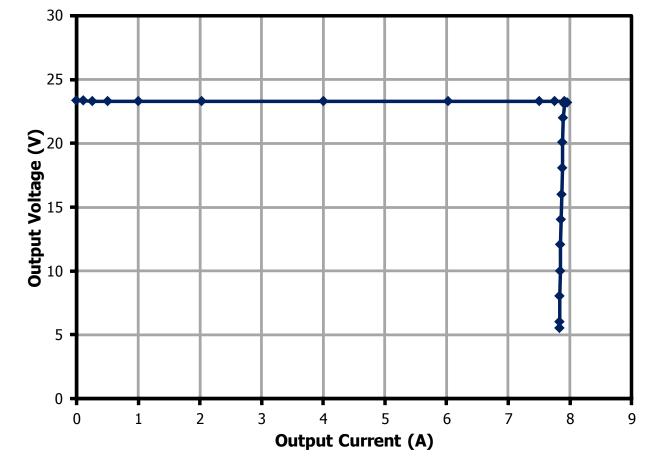


Figure 20 – V-I Characteristic with CR Load.



10.3.2 Output V-I Characteristic, Constant Voltage Load

The V-I characteristic in constant current mode was measured using a Chroma electronic load set for constant voltage mode. The minimum operating voltage of the load in CV mode is 0.66 V.

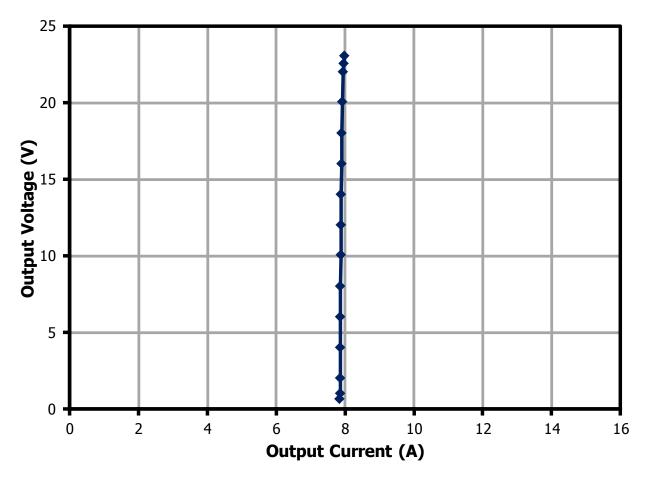


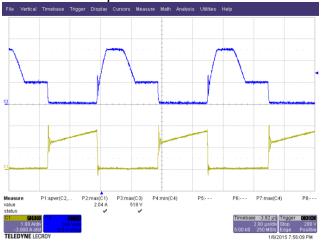
Figure 21 – V-I Characteristic with CV Load.

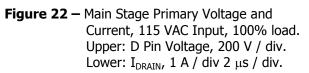


11 Waveforms

11.1 Primary Voltage and Current, Main and Standby Converters

The Main stage current was measured by inserting a current sensing loop in series with the U7 "HS" pin.





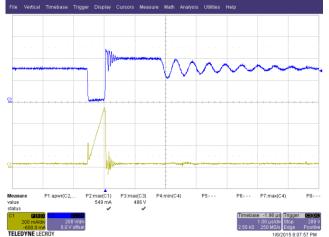
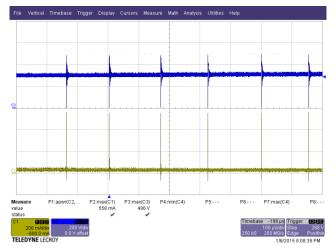
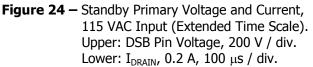
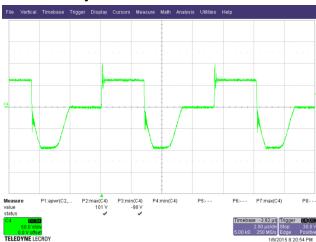


Figure 23 – Standby Primary Voltage and Current, 115 VAC Input. Upper: DSB Pin Voltage, 200 V / div. Lower: I_{DRAIN}, 0.2 A /, 1 μs / div.

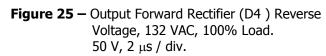








11.2 Output Rectifier Peak Reverse Voltage



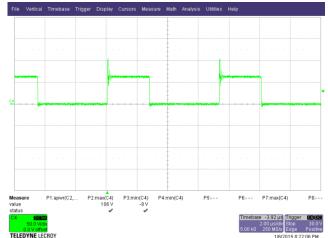
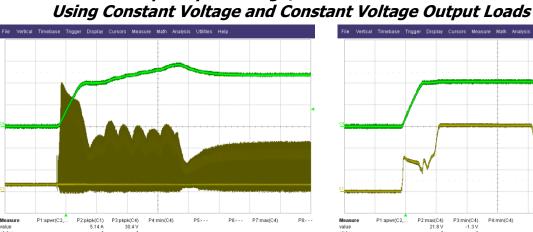


Figure 26 – Output Catch Rectifier (D16) Reverse Voltage, 132 VAC, 100% Load. 50 V, 2 μs / div.





11.3 Main Start-up Output Voltage/Current and Transformer Primary Current

Figure 27 – CV Start-up. 115 VAC, 7.5 A CC Load. Upper: Main V_{OUT}, 10 V / div. Lower: Main I_{PRIMARY}, 1 A, 1 ms / div.







Figure 29 – CC Start-up. 115 VAC, Low Impedance CV Load, 12 V Setting. Upper: Main V_{OUT} , 5 V / div. Lower: Main I_{OUT}, 5 A, 2 ms / div.



Figure 30 - CC Start-up. 115 VAC, Low Impedance CV Load, 7.5 V Setting. Upper: Main V_{OUT} 5 V / div. Lower: Main I_{OUT}, 5 A, 2 ms / div.





11.4 Load Transient Response, Voltage Mode

Figure 31 – Main Output transient Response for 4A-6A-4A Load
Transient. Averaging was Used on Upper Trace to
Isolate Contribution of Load Transient to Output
Voltage Excursion.
Upper: Main V_{OUT} , 200 mV / div., AC Coupled.
Lower: Main I_{OUT} , 2 A, 500 μ s / div.



11.5 *Output Ripple Measurements*

11.5.1 Ripple Measurement Technique

For DC output ripple measurements a modified oscilloscope test probe is used to reduce spurious signals. Details of the probe modification are provided in the figures below.

Tie two capacitors in parallel across the probe tip of the 4987BA probe adapter. Use a 0.1 μF / 50 V ceramic capacitor and 1.0 μF / 100 V aluminum electrolytic capacitor. The aluminum-electrolytic capacitor is polarized, so always maintain proper polarity across DC outputs.

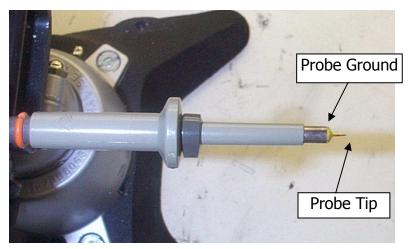


Figure 32 – Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).



Figure 33 – Oscilloscope Probe with Probe Master 4987BA BNC Adapter (Modified with Wires for Probe Ground for Ripple measurement and Two Parallel Decoupling Capacitors Added).



11.5.2 Output Ripple Measurements

Measurements were taken for main output ripple voltage with the supply operating in constant voltage mode, and for both output ripple voltage and current with the supply operating in CC mode. CC mode measurements were taken using a low impedance CV load at 20 V, 17 V, and 7.5 V CV settings. Output ripple voltage/current measurements were made using an AC coupled voltage and/or current probes.

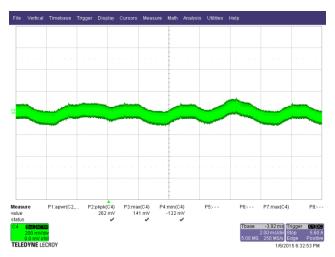
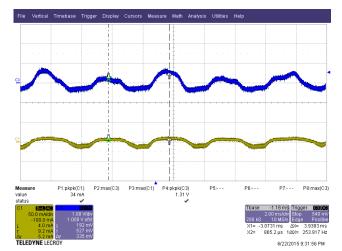
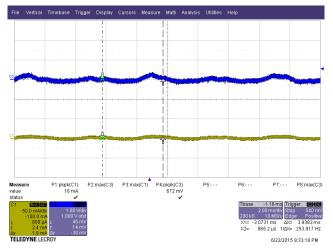


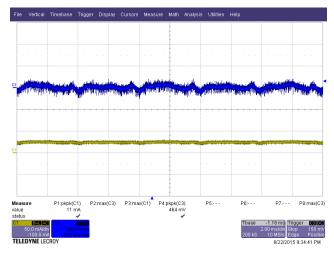
Figure 34 – Main Output Ripple, 115 VAC, CV Mode, 100% Load, CC Load Setting – 200 mV, 2 ms / div.



 $\label{eq:Figure 35-Output Voltage and Current Ripple, \\ 115 VAC, Chroma CV Load, 22 V Setting. \\ Upper: Main V_{OUT} Ripple, 1 V / div. \\ Lower: I_{OUT} Ripple, 50 mA, 2 ms / div. \\ \end{array}$



 $\label{eq:Figure 36} \begin{array}{l} \mbox{--} \mbox{Output Voltage and Current Ripple,} \\ 115 \mbox{VAC, Chroma CV Load, 11 V Setting.} \\ \mbox{Upper: Main V}_{\mbox{OUT}} \mbox{Ripple, 1 V / div.} \\ \mbox{Lower: I}_{\mbox{OUT}} \mbox{Ripple, 50 mA, 2 ms / div.} \end{array}$



 $\label{eq:Figure 37} \begin{array}{c} \textbf{Figure 37} & - \mbox{ Output Voltage and Current Ripple,} \\ 115 \mbox{ VAC, Chroma CV Load, 5.5 V Setting.} \\ \mbox{ Upper: Main V}_{OUT} \mbox{ Ripple, 500 mV / div.} \\ \mbox{ Lower: I}_{OUT} \mbox{ Ripple, 50 mA, 2 ms / div.} \end{array}$



12 Temperature Profiles

The board was operated at room temperature, with output set at maximum using a constant voltage load. For each test condition the unit was allowed to thermally stabilize $(\sim 1 \text{ hr})$ before measurements were made.

Position	Temperature (°C)
	90 VAC
T1 (Main)	83
T2 (SBY)	42
BR1	72.7
L1 (CM)	58
L2 (CM)	59
L3 (Main)	77
U1	90.9
D8/D9 (FWD/CTH)	85/90
R37/R38 (C Sense)	66
AMB	25

12.1 *Spot Temperature Measurements*

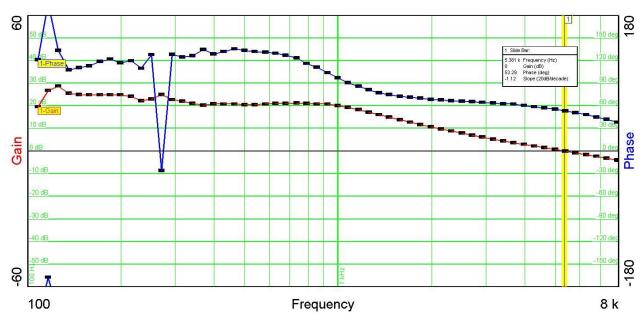
12.2 90 VAC, 60 Hz, 100% Load Temperature Profile



Figure 38 – Top View Thermal Picture, 90 VAC.



13 Gain-Phase



13.1 Constant Voltage Mode Gain-Phase





13.2 *Constant Current Mode Gain-Phase*

Gain-phase was tested using an electronic load set to constant voltage mode at 22 V, 11 V, and 5.5 V with the output current limit of the UUT set for 8 A. This characterizes the current control loop at three separate points along its V-I characteristic curve. Using a CV load maximizes the CC loop gain (worst case for control loop) and simulates operating while charging a battery. Using the constant resistance setting for the electronic load will yield overly optimistic results for gain-phase measurements and for determining component values for frequency compensation.

13.2.1 *Current Mode Gain Phase Using Chroma 63106 Electronic Load Set for CV Mode*

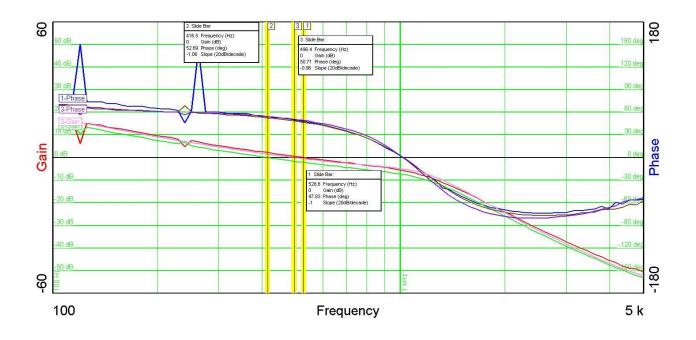


 Figure 40 – Gain-Phase, Constant Current Output, Chroma 63106 Load in Constant Voltage Mode. Red/Blue – 22 V Gain and Phase – Crossover Frequency – 527 Hz, Phase Margin – 48°. Brown/Green – 11 V Gain and Phase – Crossover Frequency – 416 Hz, Phase Margin – 53°. Pink/Purple – 5.5 V Gain and Phase – Crossover Frequency – 496 Hz, Phase Margin – 51°.



14 Conducted EMI

Conducted EMI tests were performed using a floating resistive load (3 Ω).



Figure 41 – EMI Set-Up with Floating Resistive Load.



14.1 Unmodified Supply EMI Scan

The scan shown in Figure 42 has a problem area at \sim 30 MHz. This peak can be reduced using a high frequency common mode choke at the AC input as described in the next section.

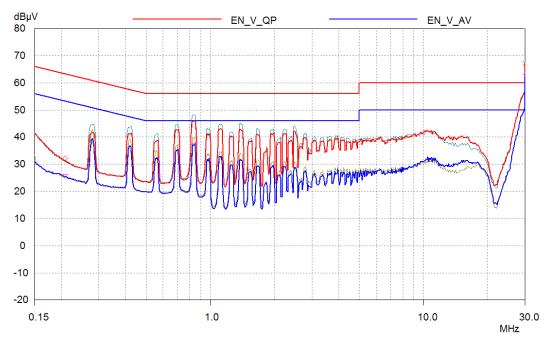


Figure 42 – Conducted EMI, 115 VAC, 3 Ω Floating Load.

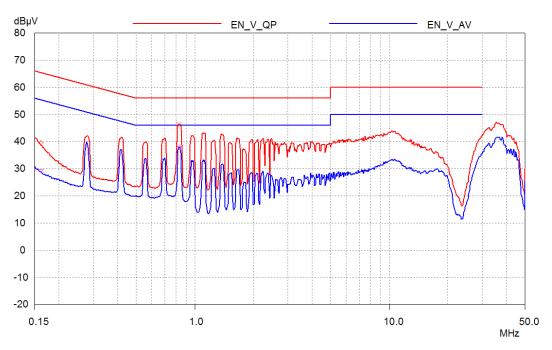


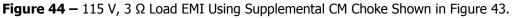
14.2 EMI Results Using Supplemental HF Common Mode AC Input Choke

A supplemental common mode choke was added to the AC input cable harness of the supply as shown in Figure 43. This choke consisted of 4 turns on a Fair-Rite 5943000201 toroidal bead. In practice, this choke would be wound into the AC input cord inside the power supply enclosure. As seen in Figure 46, the extra choke greatly reduces the amplitude of the \sim 30 MHz problem peak.



Figure 43 – Supplemental CM Choke (4T on Fair-Rite 5943000201).







15 Revision History

Date	Author	Revision	Description and Changes	Reviewed
25-Sep-15	RH	4.0	Initial Release	Apps & Mktg
15-Apr-19	RH	5.0	Change R33 value to center C.L.	



For the latest updates, visit our website: www.power.com

Power Integrations reserves the right to make changes to its products at any time to improve reliability or manufacturability. Power Integrations does not assume any liability arising from the use of any device or circuit described herein. POWER INTEGRATIONS MAKES NO WARRANTY HEREIN AND SPECIFICALLY DISCLAIMS ALL WARRANTIES INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF THIRD PARTY RIGHTS.

Patent Information

The products and applications illustrated herein (including transformer construction and circuits' external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at <u>www.power.com</u>. Power Integrations grants its customers a license under certain patent rights as set forth at http://www.power.com/ip.htm.

The PI Logo, TOPSwitch, TinySwitch, LinkSwitch, LYTSwitch, InnoSwitch, DPA-Switch, PeakSwitch, CAPZero, SENZero, LinkZero, HiperPFS, HiperTFS, HiperLCS, Qspeed, EcoSmart, Clampless, E-Shield, Filterfuse, FluxLink, StackFET, PI Expert and PI FACTS are trademarks of Power Integrations, Inc. Other trademarks are property of their respective companies. ©Copyright 2015 Power Integrations, Inc.

Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS

5245 Hellyer Avenue San Jose, CA 95138, USA. Main: +1-408-414-9200 Customer Service: Phone: +1-408-414-9665 Fax: +1-408-414-9765 e-mail: usasales@power.com

CHINA (SHANGHAI)

Rm 2410, Charity Plaza, No. 88, North Caoxi Road, Shanghai, PRC 200030 Phone: +86-21-6354-6323 Fax: +86-21-6354-6325 e-mail: chinasales@power.com

CHINA (SHENZHEN)

17/F, Hivac Building, No. 2, Keji Nan 8th Road, Nanshan District, Shenzhen, China, 518057 Phone: +86-755-8672-8689 Fax: +86-755-8672-8690 e-mail: chinasales@power.com

GERMANY

Lindwurmstrasse 114 80337, Munich Germany Phone: +49-895-527-39110 Fax: +49-895-527-39200 e-mail: eurosales@power.com

INDIA #1, 14th Main Road Vasanthanagar Bangalore-560052 India Phone: +91-80-4113-8020 Fax: +91-80-4113-8023 e-mail: indiasales@power.com

ITALY

Via Milanese 20, 3rd. Fl. 20099 Sesto San Giovanni (MI) Italy Phone: +39-024-550-8701 Fax: +39-028-928-6009 e-mail: eurosales@power.com

JAPAN

Kosei Dai-3 Building 2-12-11, Shin-Yokohama, Kohoku-ku, Yokohama-shi, Kanagawa 222-0033 Japan Phone: +81-45-471-1021 Fax: +81-45-471-3717 e-mail: japansales@power.com

KOREA

RM 602, 6FL Korea City Air Terminal B/D, 159-6 Samsung-Dong, Kangnam-Gu, Seoul, 135-728 Korea Phone: +82-2-2016-6610 Fax: +82-2-2016-6630 e-mail: koreasales@power.com

SINGAPORE

51 Newton Road, #19-01/05 Goldhill Plaza Singapore, 308900 Phone: +65-6358-2160 Fax: +65-6358-2015 e-mail: singaporesales@power.com

TAIWAN

5F, No. 318, Nei Hu Rd., Sec. 1 Nei Hu District Taipei 11493, Taiwan R.O.C. Phone: +886-2-2659-4570 Fax: +886-2-2659-4550 e-mail: taiwansales@power.com

UK

Cambridge Semiconductor, a Power Integrations company Westbrook Centre, Block 5, 2nd Floor Milton Road Cambridge CB4 1YG Phone: +44 (0) 1223-446483 e-mail: eurosales@power.com

