



Design Example Report

Title	10 W Non-Isolated Tapped Buck Power Supply Using LNK626DG
Specification	Input: 85 VAC – 265 VAC; Output: 20.0 V / 500 mA
Application	Embedded Power Supply
Author	Applications Engineering Department
Document Number	DER-572
Date	January 10, 2017
Revision	1.0

Summary and Features

- 82% efficiency at 115VAC and 230VAC during full load
- Output voltage adjustable from 12V to 20V
- Excellent output voltage load regulation (< 5% V_{TYP})
- Smaller, lower cost output capacitors
- Low no-load input power < 200 mW
- Low output voltage ripple < 200 mV_{PK-PK}

PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at <<http://www.powerint.com/ip.htm>>.

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.



1 Introduction

This document is an engineering report describing a single output 20 V, 500 mA embedded power supply utilizing a device from LinkSwitch-CV family of ICs. This design shows the high power density and efficiency that is possible due to the high level of integration while still providing exceptional performance.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.



Figure 1 – Populated Circuit Board Photograph, Top.

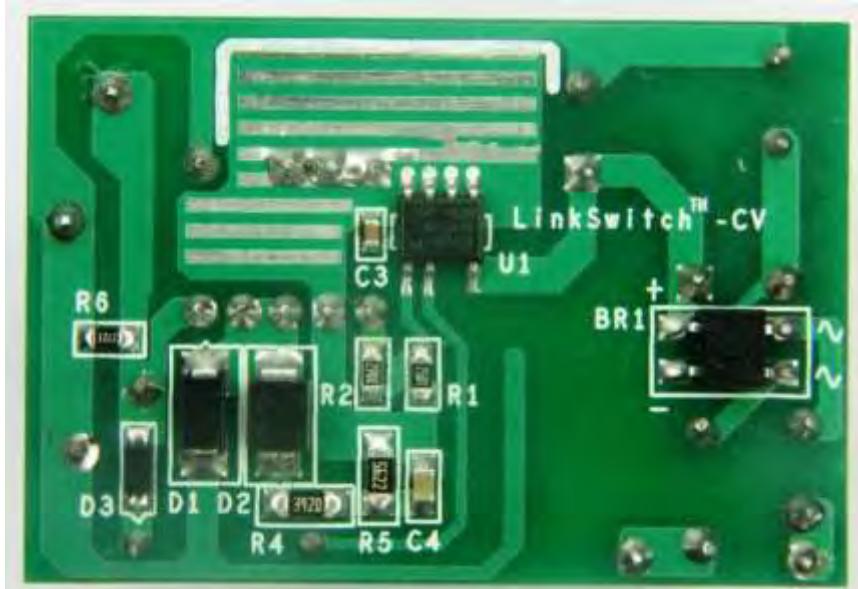


Figure 2 – Populated Circuit Board Photograph, Bottom.



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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – No P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
No-load Input Power			120		mW	115 VAC.
Output						
Output Voltage	V_{OUT}	19	20	21	V	$\pm 5\%$
Output Current	I_{OUT}	0	500		mA	
Output Voltage Ripple	V_{RIPPLE}		200		mV	20 MHz Bandwidth.
Peak Power Output	P_{OUT PEAK}			10	W	
Efficiency at 115 VAC / 230 VAC	η		82		%	Measured at Output Terminal.
Full load			CISPR22B / EN55022B Floating			Resistive Load
Environmental						
Conducted EMI						
Line Surge				1	kV	IEC 61000-4-5
Differential Mode						1.2 μ s / 50 μ s Surge Mode, 2 Ω .
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level in Sealed Enclosure.



3 Schematic

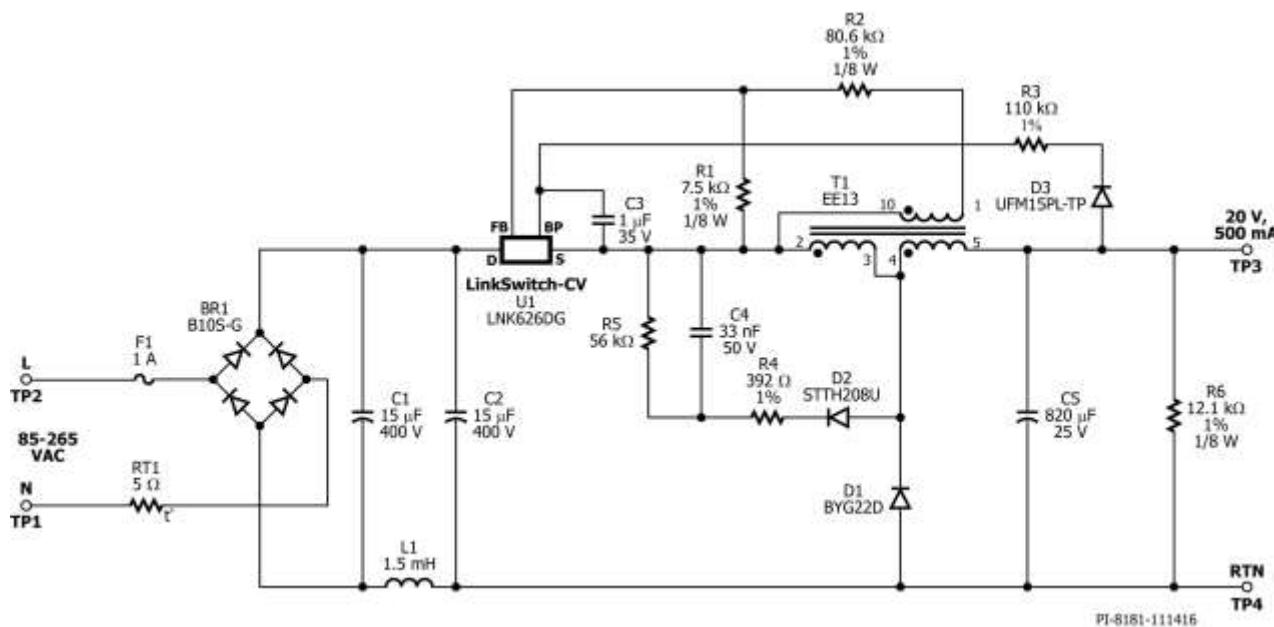


Figure 3 – Schematic.

4 Circuit Description

4.1 Input Protection and EMI Filtering

Fuse F1 and RT1 provides protection from inrush current and surge events. A bridge rectifier BR1 rectifies the AC line voltage and provides full wave rectified DC across C1. Capacitor C1, L1 and C2 forms a pi filter, which is used to reduce the differential mode conducted emissions.

4.2 Power Stage

The circuit consisting of a switching controller U1, T1, D1 and C5 forms a tapped buck configuration, which is used to step down the rectified AC input voltage. The circuit also includes a snubber circuit and bias supply.

The LinkSwitch-CV IC was utilized and configured as a high-side driver. The LNK626DG IC was selected to deliver typical power of 10 W. When the power MOSFET switches ON, current ramps up and flows through the transformer T1 and through the output. Freewheeling diode D1 is reverse biased. The capacitor C3, connected to the BYPASS pin is charged. The current continues to ramp up until it reaches the current limit set by capacitor C3, which causes the power MOSFET to turn-off. When the power MOSFET switches OFF, the energy in the T1 couples through to the output. The peak current in the output winding steps up by the inductor ratio. This stepped current flows out of the output winding, through freewheeling diode D1, and back through the load.

The freewheeling diode, D1, should be an ultrafast type. Reverse recovery time $t_{RR} < 25$ ns should be used at a temperature of 70 °C or above. Continuous mode of operation will always occur during start-up thus using slower diodes is not acceptable because of high leading-edge current spikes, terminating the operation and preventing the output reaching regulation.

During normal operation, the BYPASS (BP) pin is powered from the main output of the circuit through D3 and R3. For very low no-load input power consumption, R3 must be optimized.

For output capacitor C5, select a very low ESR capacitor to minimize the output ripple to less than 200 mV.

The leakage energy in the T1 causes Drain voltage spikes. The Drain voltage spikes should be limited to less than 90% of the breakdown voltage rating. To minimize the leading edge spikes, a snubber circuit consisting of RCD (D2, C4, R4 and R5) is used. Ringing on the Drain voltage can be minimized by optimizing the snubber design.



4.3 *Feedback Loop*

The output voltage is regulated by an indirect feedback method. The feedback loop is formed by the auxiliary winding of T1, R1 and R2. Resistor R1 and R2 are configured to deliver an output voltage of 20 V.



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5 PCB Layout

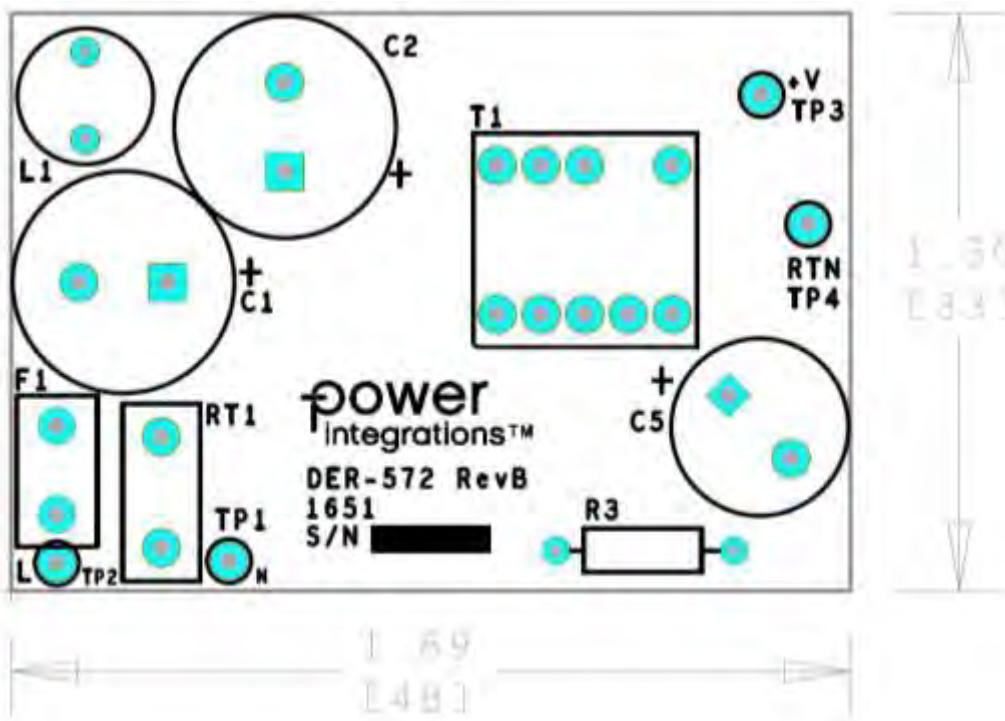


Figure 4 – Printed Circuit Layout, Top.

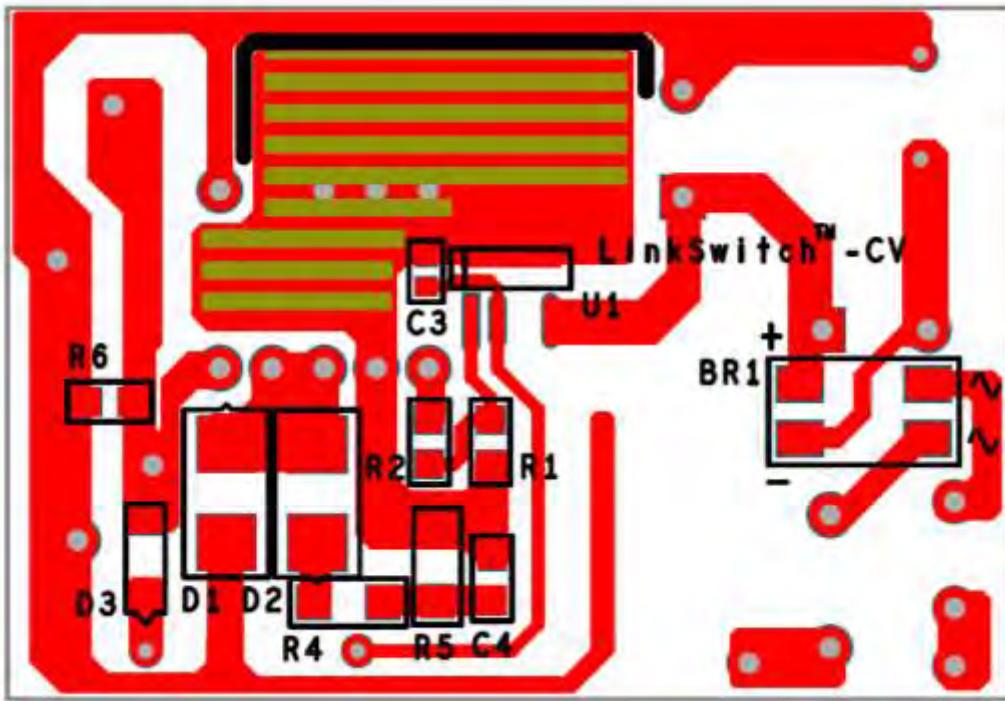


Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	B10S-G	Comchip
2	1	C1	15 μ F, 400 V, Electrolytic, (12.5 x 22)	UCS2G150MHD1TO	Nichicon
3	1	C2	15 μ F, 400 V, Electrolytic, (12.5 x 22)	UCS2G150MHD1TO	Nichicon
4	1	C3	1 μ F 35 V, Ceramic, X7R, 0603	C1608X7R1V105M	TDK
5	1	C4	33 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB333	Yageo
6	1	C5	820 μ F, 25 V, Electrolytic, Low ESR, (10 x 20)	UHV1E821MPD	Nichicon
7	1	D1	200 V, 2 A, Ultrafast Recovery, 25 ns, DO-214AA	BYG22D/54	General Semi
8	1	D2	800 V, 2 A, Ultrafast Recovery, 75 ns, DO-214AA	STTH208U	ST
9	1	D3	600 V, 1 A, Ultrafast Recovery, 75 ns, SOD-123	UFM15PL-TP	Micro Commercial
10	1	F1	1 A, 250 V, Slow, Long Time Lag, RST 1	RST 1	Belfuse
11	1	FL1	Flying Lead , Hole size 30mils	N/A	N/A
12	1	L1	1.5 mH, 0.52 A, 9 x 9 mm	SL1016-152K-B	Yago
13	1	R1	RES, 7.50 k Ω , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF7501V	Panasonic
14	1	R2	RES, 80.6 k Ω , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF8062V	Panasonic
15	1	R3	RES, 110 k Ω , 1%, 1/4 W, Metal Film	MFR-25FBF-110K	Yageo
16	1	R4	RES, 392 Ω , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF3920V	Panasonic
17	1	R5	RES, 56 k Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ563V	Panasonic
18	1	R6	RES, 12.1 k Ω , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1212V	Panasonic
19	1	RT1	TKS Thermistor, 5 Ω , 3 A	SCK08053MSY	Thinking Elect.
20	1	T1	Bobbin, EE13, Vertical, 10 pins	YW-538-02B	Yih-Hwa
21	1	TP1	Test Point, BLK,Miniature THRU-HOLE MOUNT	5001	Keystone
22	1	TP2	Test Point, WHT,Miniature THRU-HOLE MOUNT	5002	Keystone
23	1	TP3	Test Point, RED,Miniature THRU-HOLE MOUNT	5000	Keystone
24	1	TP4	Test Point, BLK,Miniature THRU-HOLE MOUNT	5001	Keystone
25	1	U1	LinkSwitch-CV, SO-8C	LNK626DG	Power Integrations



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7 Transformer Specification

7.1 Electrical Diagram

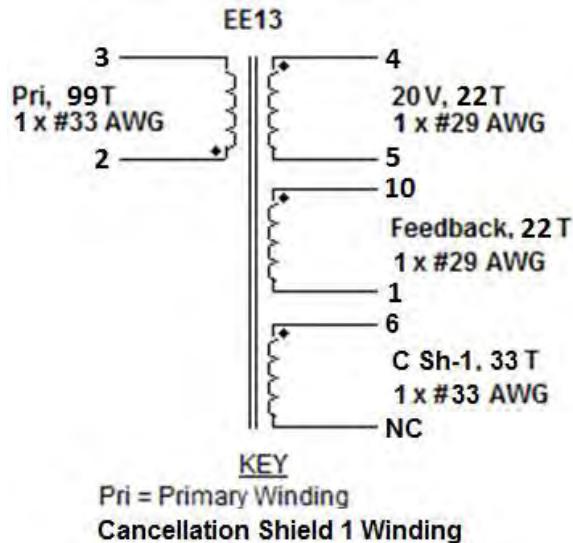


Figure 6 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Main Inductance	Pin 2 and pin 3 together, measured at 100 kHz, 1.0 V _{RMS} .	1140 μ H $\pm 5\%$
Resonant Frequency	Pin 2 and pin 3 are shorted together with all other windings open.	1.1 MHz
Electrical Strength	1 second, 60 Hz, from primary to secondary.	n/a

7.3 Material List

Item	Description
[1]	Core: EE13, NC-2H (Nicera) or Equivalent, gapped for ALG of 178 nH/T ² .
[2]	Bobbin: Generic, 5 pri. + 5 sec.
[3]	Barrier Tape: Polyester Film [1 mil (25 μ m) Base Thickness], 7.40 mm Wide.
[4]	Separation Tape: Polyester Film [1 mil (25 μ m) Base Thickness], 7.40 mm Wide.
[5]	Magnet Wire: #33 AWG, Solderable Double Coated.
[6]	Magnet Wire: #29 AWG, Solderable Double Coated.
[7]	Varnish.

7.4 Transformer Build Diagram

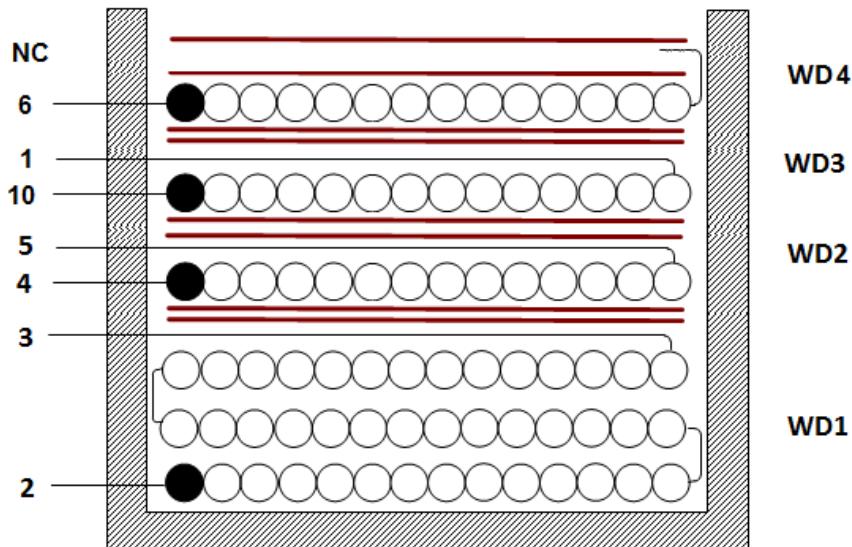


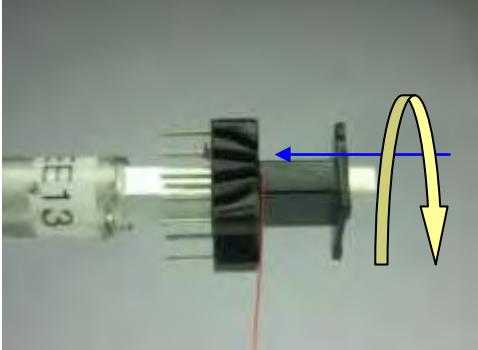
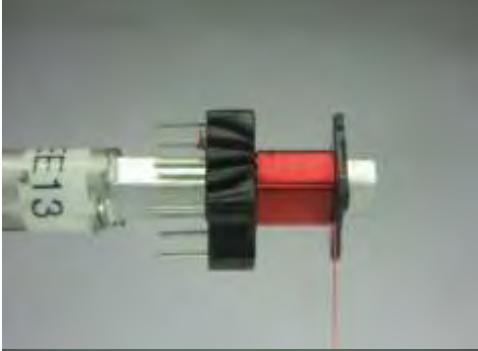
Figure 7 – Transformer Build Diagram.

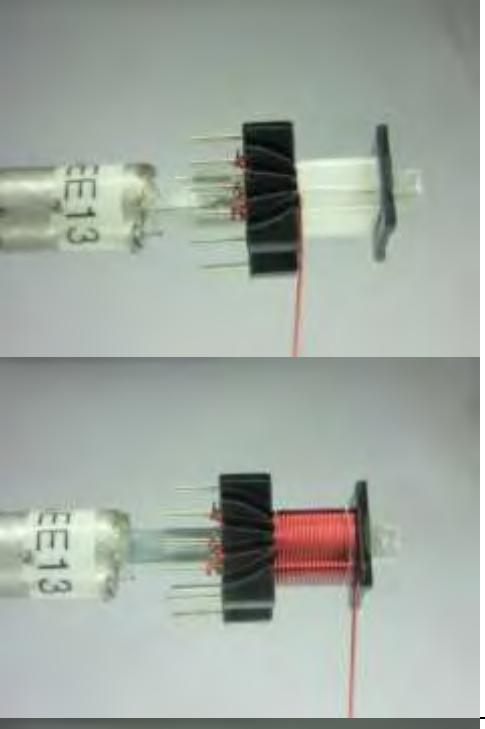
7.5 Transformer Instructions

General Note	For the purpose of these instructions, bobbin is oriented on winder such that pin-side is on the left side (see illustration). Winding direction as shown is counter-clockwise.
WD1	Start at pin 2, wind 99 turns of wire item [5] in three layers. Finish at pin 3.
Tape	Use 2 layers of tape item [4] for insulation.
WD2	Start at pin 4, wind 22 turns of wire item [6] in one layer. Finish at pin 5.
Tape	Use 2 layers of tape item [4] for insulation.
WD3	Start at pin 10, wind 22 turns of wire item [6] in one layer. Finish at pin 1.
Tape	Use 2 layers of tape item [4] for insulation.
WD4	Start at pin 6, wind 33 turns of wire item [5] in clockwise direction in one layer. End of wire floating (NC)
Tape	Use 2 layers of tape item [4] for insulation. On the first layer of tape, attach the end of WD4.
Assembly	Grind core halves for specified main inductance, insert bobbin, and secure core halves.
Tape	Use 2 layer of tape item [4] for bobbin. Use 2 layer of tape item [3] for secure core.
Varnish	Dip varnish [7].

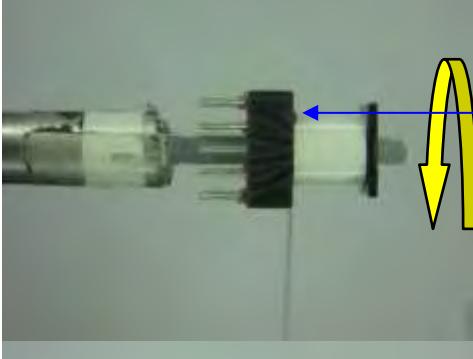


7.6 Transformer Winding Illustrations

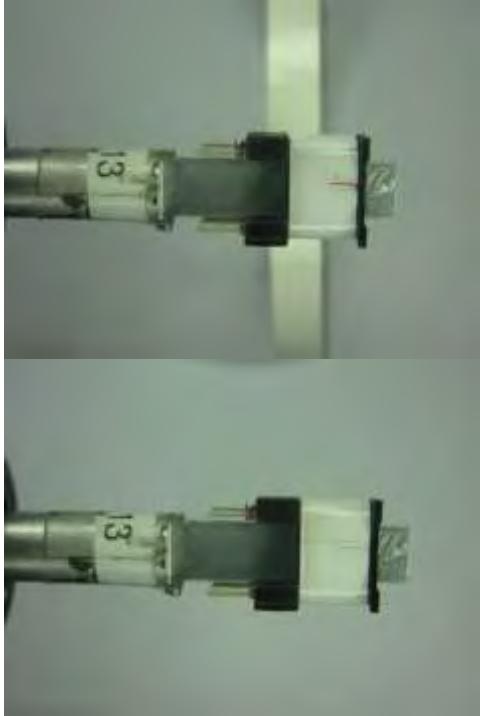
General Note		For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side (see illustration). Winding direction as shown is counter-clockwise.
WD 1		Start at pin 2, wind 99 turns of wire item [5] in three layers. Finish at pin 3.
Tape	 	Use 2 layers of tape item [4] for insulation.

WD 2		Start at pin 4, wind 22 turns of wire item [6] in one layer. Finish at pin 5.
Tape		Use 2 layers of tape item [4] for insulation.
WD3		Start at pin 10, wind 22 turns of wire item [6] in one layer. Finish at pin 1.

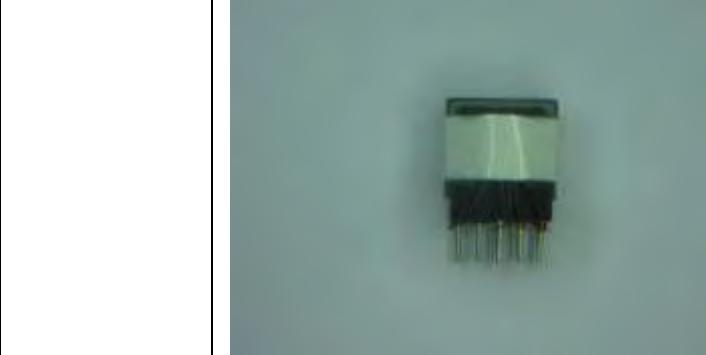
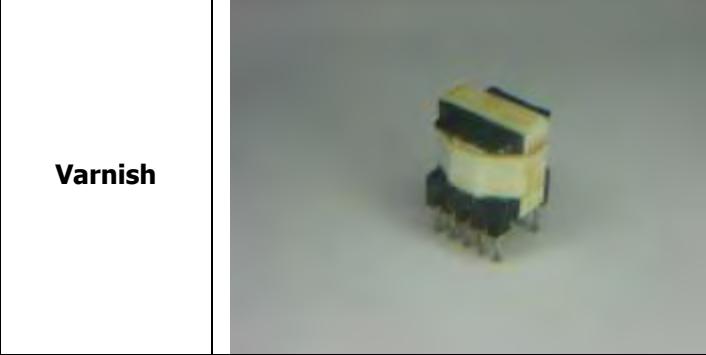


		
Tape		Use 2 layers of tape item [4] for insulation.
WD4	 	Start at pin 6, wind 33 turns of wire item [5] in clockwise direction in one layer. End of wire floating (NC)



Tape		Use 2 layers of tape item [4] for insulation. On the first layer of tape, attach the end of WD4.
Assembly		Grind core halves for specified main inductance, insert bobbin, and secure core halves.
Tape		Use 2 layer of tape item [4] for bobbin. Use 2 layer of tape item [3] for secure core.



		
Varnish		Dip varnish [7].



8 Transformer Design Spreadsheet

ACDC_LinkSwitch-CV_Tapped Inductor Buck_082016; Rev.1.0; Copyright Power Integrations 2016	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitch-CV_Tapped Inductor Buck_082016_Rev1.6.xls; LinkSwitch-CV Discontinuous Tapped-Buck Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	85			V	Minimum AC Input Voltage
VACMAX	265			V	Maximum AC Input Voltage
fL	50			Hz	AC Mains Frequency
VO	20.00			V	Output Voltage of LED strings
IO	0.50			A	Output Current riving LED strings
Power			10.00	W	Continuous Output Power
n	0.82		0.82		Efficiency Estimate at output terminals. Under 0.7 if no better data available
tC			3.50	ms	Bridge Rectifier Conduction Time Estimate
CIN	30.00			uF	Input Capacitance
DC INPUT VOLTAGE PARAMETERS					
VMIN			95.74	V	Minimum Input DC bus voltage
VMAX			374.77	V	Maximum Input DC bus voltage
ENTER LinkSwitch-CV VARIABLES					
Chosen Device	LNK626		LNK626		Chosen LinkSwitch-CV device
Package	PG		PG		Select package (PG or DG)
ILIMITMIN			0.42	A	Minimum Current Limit
ILIMITTYP			0.45	A	Typical Current Limit
ILIMITMAX			0.48	A	Maximum Current Limit
FS	100.00		100.00	kHz	!!! Info. Typical Switching frequncies above 100 kHz or below 90 kHz are generally not recommended. This may result in insufficient range for Lp and ILIMIT correction.
VDS			10.00	V	LinkSwitch-CV on-state Drain to Source Voltage
VD			0.5	V	Output Winding Diode Forward Voltage Drop
DESIGN PARAMETERS					
DCON			4.65	us	Output diode conduction time
TON			5.35	us	LinkSwitch-CV On-time (calculated at minimum inductance)
TDEAD			0.00	us	LinkSwitch-CV dead time when both the switch and diode are NOT conducting (calculated at minimum inductance)
ENTER INDUCTOR CORE/CONSTRUCTION VARIABLES					
Core Type					
Core	EE13		EE13		Enter Transformer Core
Bobbin			EE13_BOBBIN		Generic EE13_BOBBIN
AE			17.10	mm^2	Core Effective Cross Sectional Area
LE			30.20	mm^2	Core Effective Path Length
AL			1130.00	nH/turn^2	Ungapped Core Effective Inductance
BW			7.90	mm	Bobbin Physical Winding Width
INDUCTOR DESIGN PARAMETERS					
LPMIN			1083.17	uH	Minimum Inductance (Includes inductance of input and output winding)
LPTYP			1140.18	uH	Typical inductance (Includes inductance of input and output winding)
LP_TOLERANCE	5.00		5.00	%	Tolerance in inductance
NL_TOTAL			121.00		Total number of turns (Includes input and output winding turns). To adjust Total number of turns change BM_TARGET
ALG			77.68	nH/turn^2	Gapped Core Effective Inductance
BM_TARGET	2480.00		2480.00	Gauss	Target Flux Density
BM			2473.53	Gauss	Maximum Operating Flux Density (calculated)



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					at nominal inductance), BM < 3000 is recommended
BP			2770.35	Gauss	Peak Operating Flux Density (calculated at maximum inductance and max current limit), BP < 3300 is recommended
BAC			1236.76	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			158.81		Relative Permeability of ungapped Core
LG			0.27	mm	Gap Length (LG > 0.1 mm)
INDUCTOR_RATIO	0.18		0.18		Ratio of Output winding turns to Total inductor turns. Adjust ratio to ensure discontinuous operation
<i>Input Section</i>					Section of winding that conducts only during ON time of the Linkswitch-CV
NL_INPUT			99.00		Number of turns in Input section.
AWG	33		33.00		Primary Wire Gauge (Rounded to next smaller standard AWG value)
L			2.71		Number of Layers (Input section)
CMA			338.02	Cmils	Primary Winding Current Capacity (200 < CMA < 500)
<i>Output Section</i>					Section of winding that conducts both when the Linkswitch-CV is ON and OFF.
NL_OUTPUT			22.00		Number of Turns in Output winding. To adjust number of turns change INDUCTOR_RATIO
AWG_OUTPUT	29		29.00		Output Winding Wire Gauge (Rounded to next smaller standard AWG value)
L_OUTPUT			0.92		Number of Layers (Output winding)
CMA_OUTPUT	INFO**	INFO**	131.32	Cmils	Info. CMA is less than 200 and may cause overheating of the primary winding. This may be acceptable if number of turns is low. Reduce AWG_OUTPUT
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.53		Maximum duty cycle measured at VMIN
IAVG			0.13	A	Input Average current
IP			0.42	A	Peak primary current
ID_PK			2.64	A	Output Winding Peak current
ISW_RMS			0.15	A	Switch RMS current
ID_RMS			0.97	A	Freewheeling Diode RMS current
IL_RMS			0.15	A	Inductor - Input section RMS current
IL_TAP_RMS			0.97	A	Inductor - Output winding section RMS current
IR			0.42	A	Primary ripple current
FEEDBACK WINDING PARAMETERS					
NFB			22.00		Feedback winding turns
VFLY			20.50	V	Voltage across diode at turn off
VFOR			13.77	V	Voltage across Output winding of inductor when switch is on.
RUPPER			75.91	k-ohm	Upper resistor in Feedback resistor divider
RLOWER			7.31	k-ohm	Lower resistor in resistor divider
VOLTAGE STRESS PARAMETERS					
VDRAIN			534.77	V	Maximum Drain Voltage Estimate (Assumes 50 V leakage spike)
VOR			110.00	V	Reflected output voltage at turn off (appears in series with Linkswitch-CV)
PIVS			68.14	V	Output Rectifier Maximum Peak Inverse Voltage

****NOTE**

CMA_OUTPUT – The temperature of the transformer was measured and found to be below the limits.



9 Performance Data

9.1 Full Load Efficiency vs. Input Line Voltage

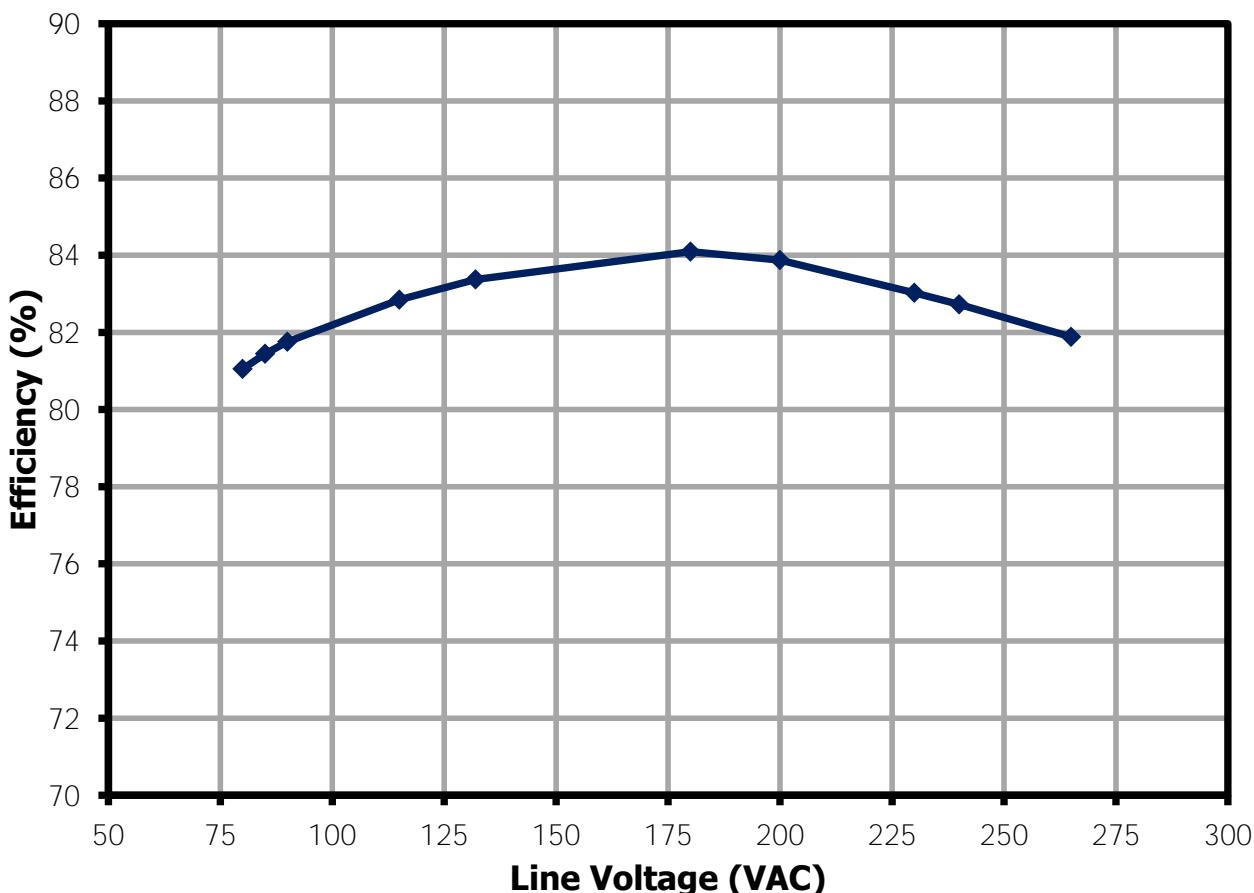


Figure 8 – Efficiency vs. Line Voltage, Room Temperature.



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9.2 Efficiency vs. Load

9.2.1 Efficiency at 20 V Output (25 mA - 500 mA on 20 V)

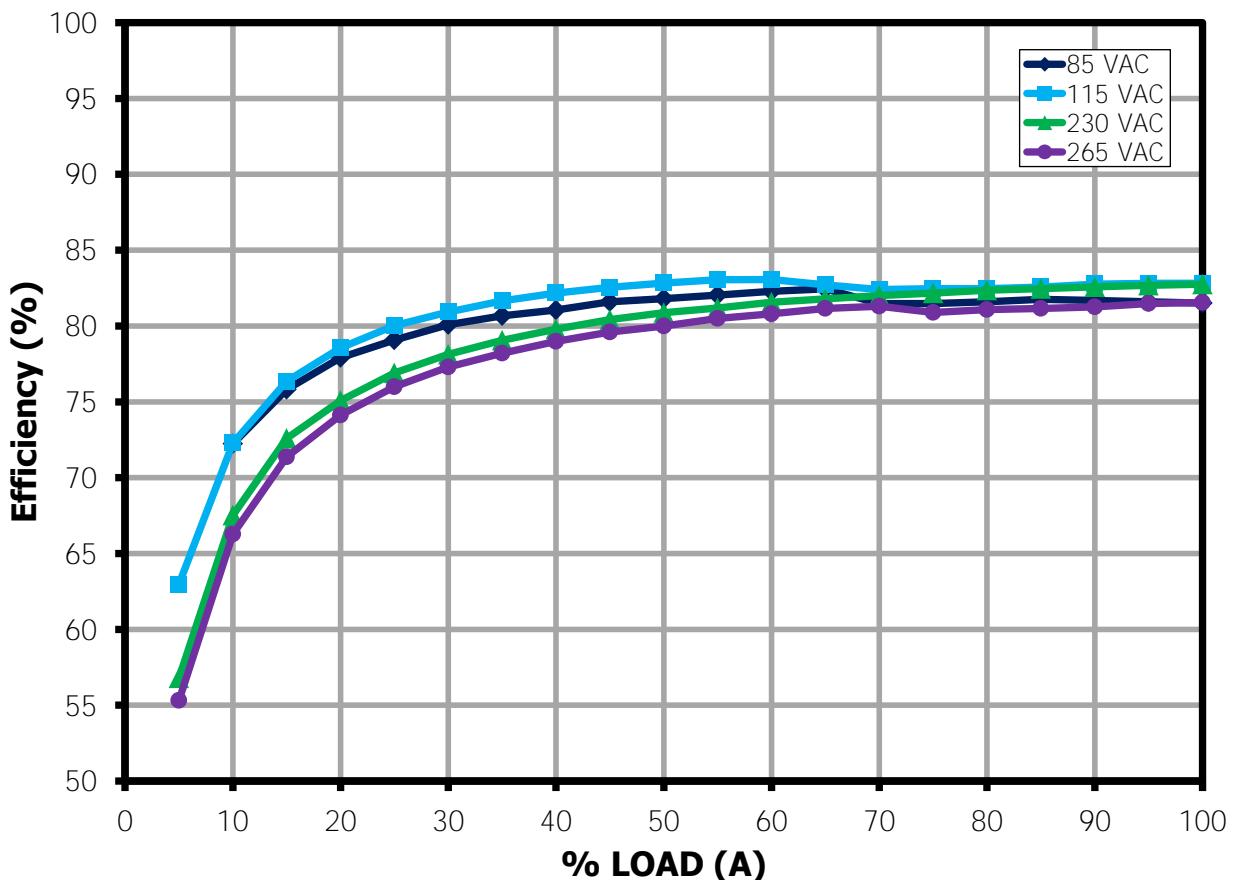


Figure 9 – Efficiency vs. Load, Room Ambient (measured at the Output Terminal).

9.3 **No-Load Input Power**

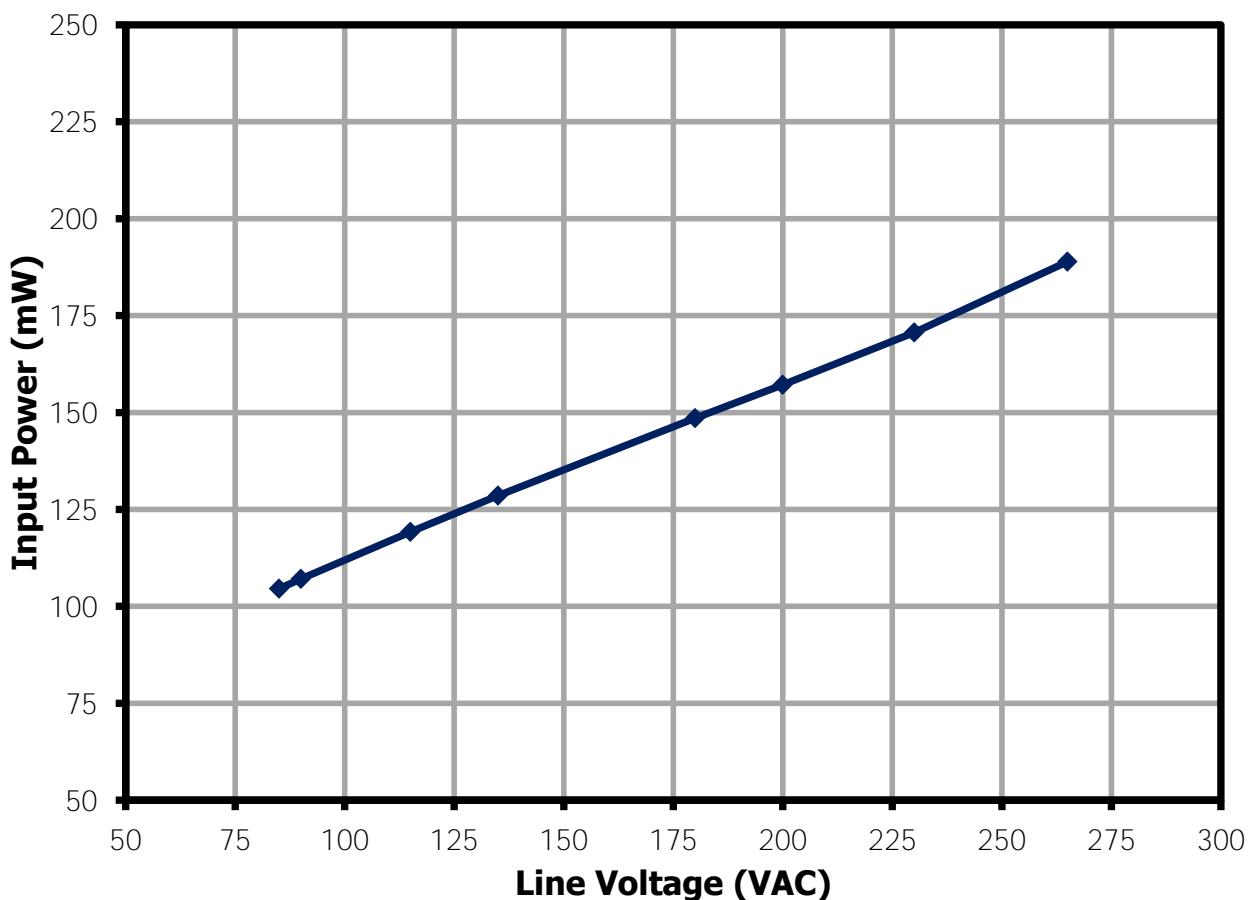


Figure 10 – Input Power vs. Input Line Voltage at No load, Room Temperature.



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9.4 *Line and Load Regulation*

9.4.1 Line Regulation

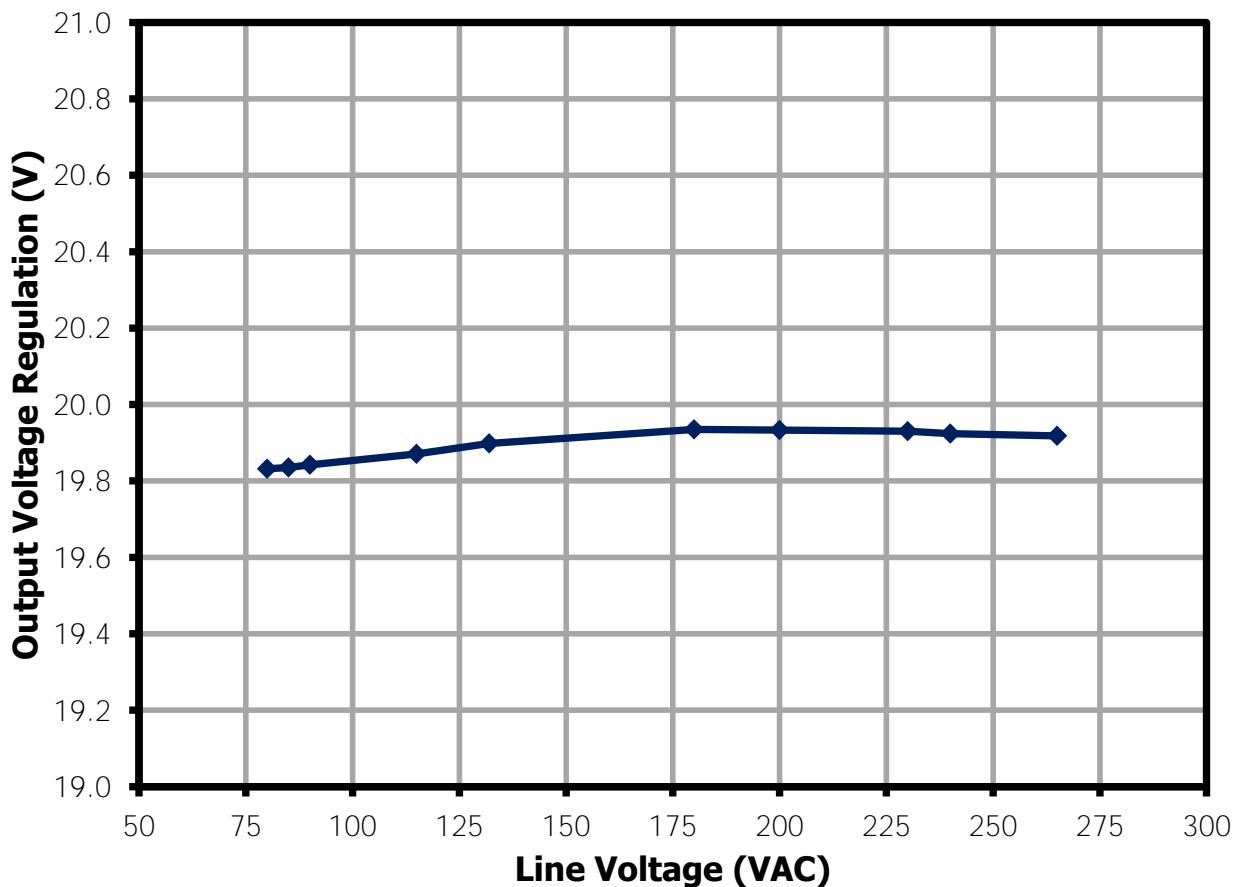


Figure 11 – Output Voltage vs. Input Line Voltage at Full load, Room Temperature.



9.4.2 Load Regulation

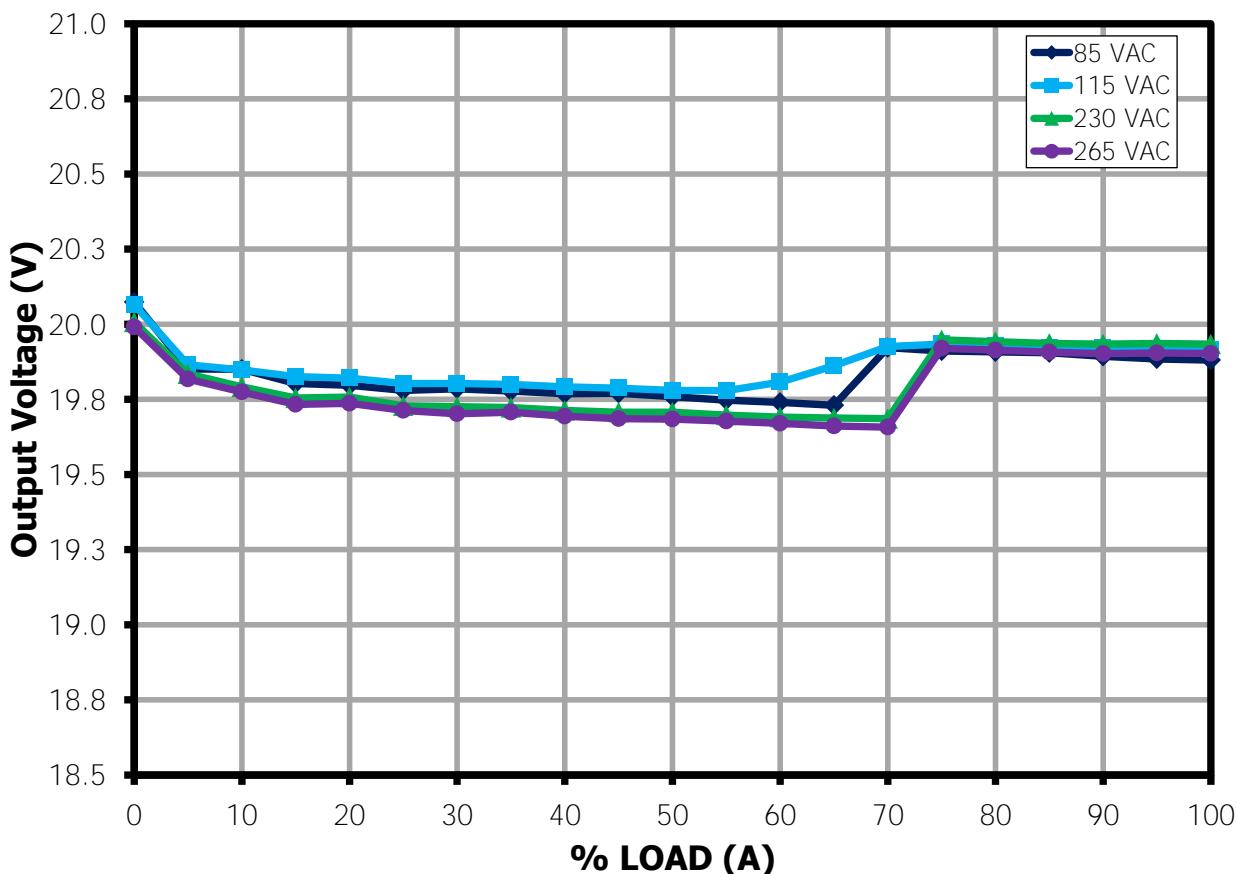


Figure 12 – Output Voltage vs. Varying load, Room Temperature.



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10 Output Ripple Measurement

10.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 $\mu\text{F}/50\text{ V}$ ceramic type and one (1) 1 $\mu\text{F}/50\text{ V}$ aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).



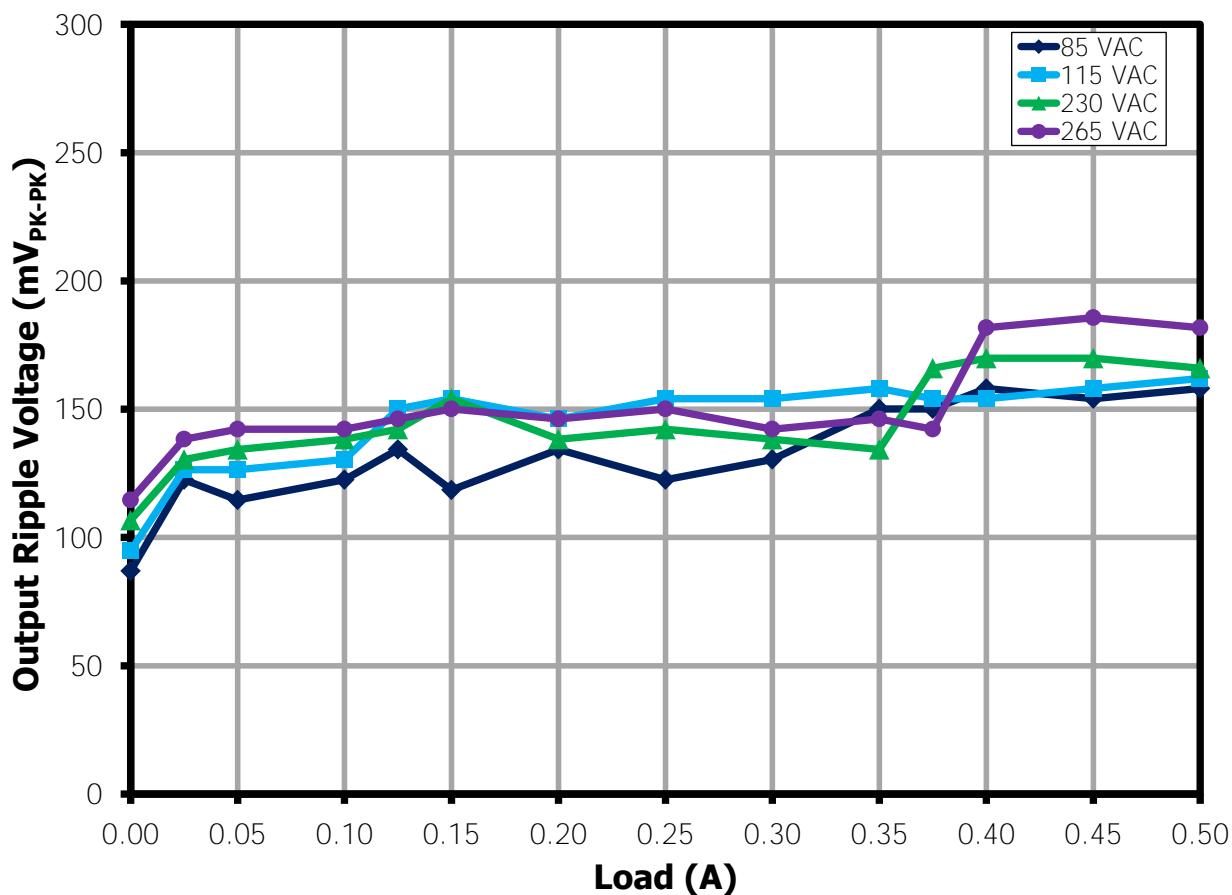
Figure 13 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)



Figure 14 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter.
(Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

10.1.1 Measurement Results

10.1.1.1 Output Ripple Graph from 0% to 100%

**Figure 15 –** Output Ripple Voltage at 10 W.

85 V RIPPLE (mV _{PK-PK})	115 V RIPPLE (mV _{PK-PK})	230 V RIPPLE (mV _{PK-PK})	265 V RIPPLE (mV _{PK-PK})
158.10	162.06	166.01	181.82

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10.1.2 Output Ripple Voltage Waveforms

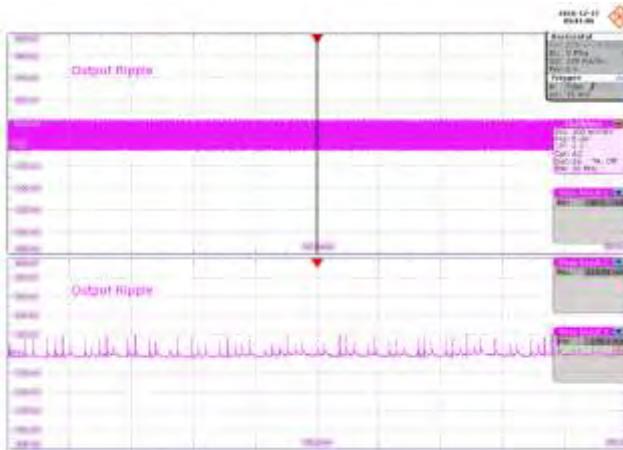


Figure 16 – 85 VAC Input.

Condition: 20 V – 500 mA.
 V_{RIPPLE} , 100 mV / div., 100 ms / div.
 Zoom: 100 μ s / div.

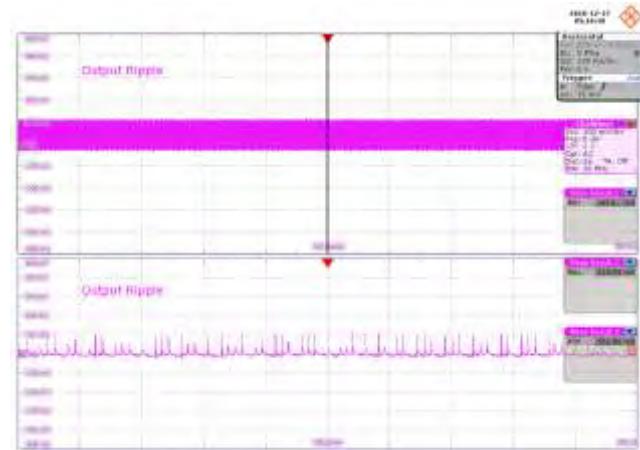


Figure 17 – 115 VAC Input.

Condition: 20 V – 500 mA.
 V_{RIPPLE} , 100 mV / div., 100 ms / div.
 Zoom: 100 μ s / div.

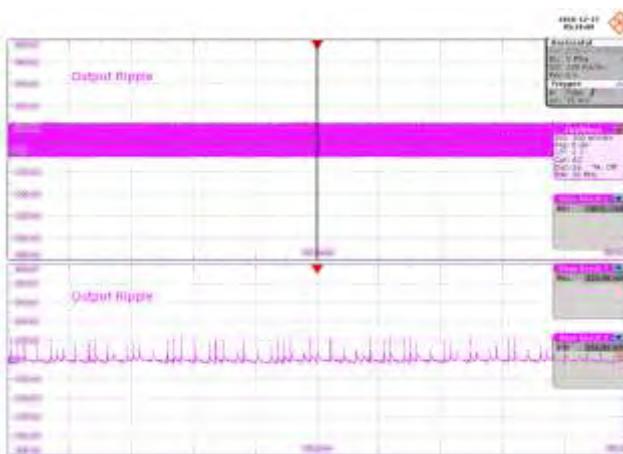


Figure 18 – 230 VAC Input.

Condition: 20 V – 500 mA.
 V_{RIPPLE} , 100 mV / div., 100 ms / div.
 Zoom: 100 μ s / div.

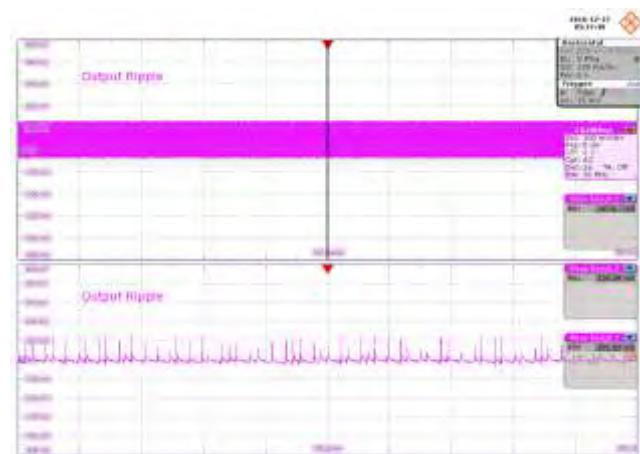


Figure 19 – 265 VAC Input.

Condition: 20 V – 500 mA.
 V_{RIPPLE} , 100 mV / div., 100 ms / div.
 Zoom: 100 μ s / div.



11 Waveforms

11.1 Output Load Transient Response

Results were taken at the output terminal which is the typical specified measurement condition for embedded power supply. The +20 V output is step load from 50% to 100% and 0% to 100%

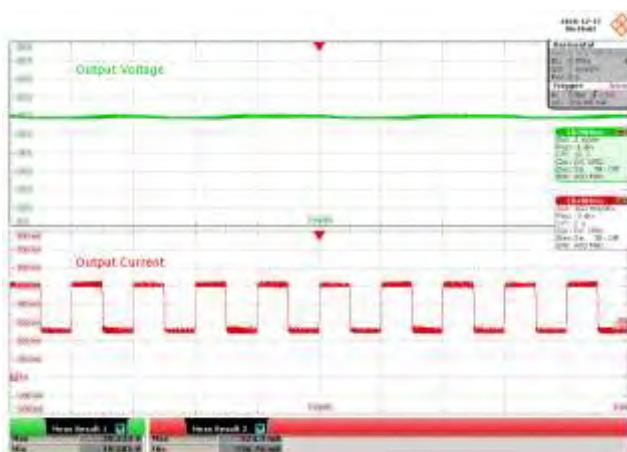


Figure 20 – 85 VAC, 50-100% Load Step.

V_{MAX} : 20.213 V.

V_{MIN} : 19.581 V.

Upper: V_{OUT} , 2 V / div., Offset: 16 V
Lower: I_{LOAD} , 100 mA / div., 1 ms / div.

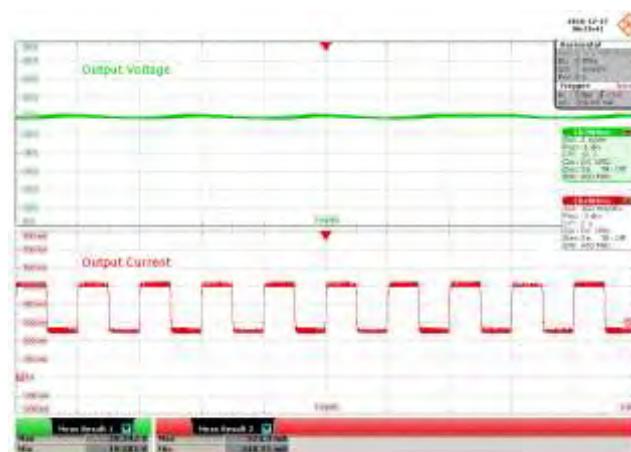


Figure 21 – 265 VAC, 50-100% Load Step.

V_{MAX} : 20.292 V.

V_{MIN} : 19.581 V.

Upper: V_{OUT} , 2 V / div., Offset: 16 V
Lower: I_{LOAD} , 100 mA / div., 1 ms / div.

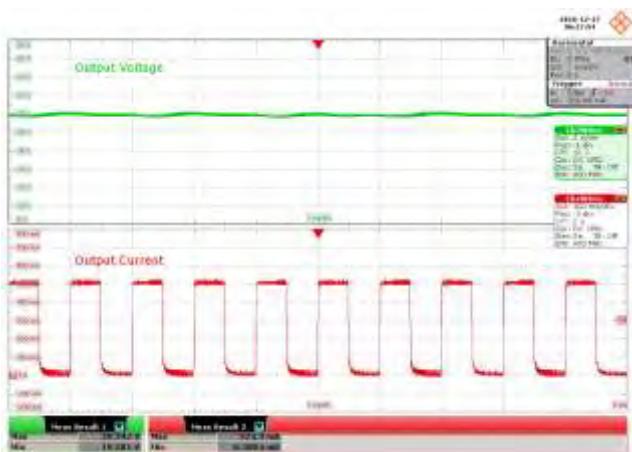


Figure 22 – 85 VAC, 0-100% Load Step.

V_{MAX} : 20.292 V.

V_{MIN} : 19.581 V.

Upper: V_{OUT} , 2 V / div., Offset: 16 V
Lower: I_{LOAD} , 100 mA / div., 1 ms / div.

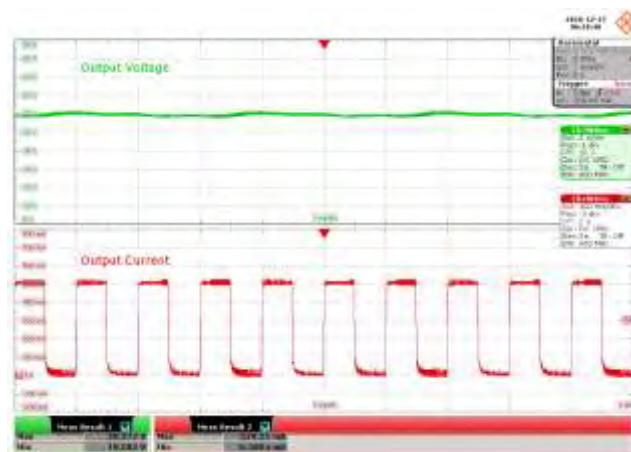


Figure 23 – 265 VAC, 0-100% Load Step.

V_{MAX} : 20.372 V.

V_{MIN} : 19.502 V.

Upper: V_{OUT} , 2 V / div., Offset: 16 V
Lower: I_{LOAD} , 100 mA / div., 1 ms / div.



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11.2 Switching Waveforms

11.2.1 Drain to Source Voltage and Current

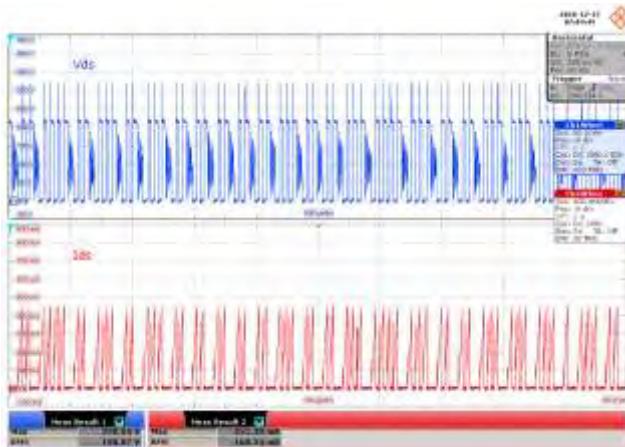


Figure 24 – 85 VAC Input.

Condition: 20 V – 500 mA.
Upper: V_{DS} , 50 V / div.
Lower: I_{DS} , 100 mA / div., 100 μ s / div.

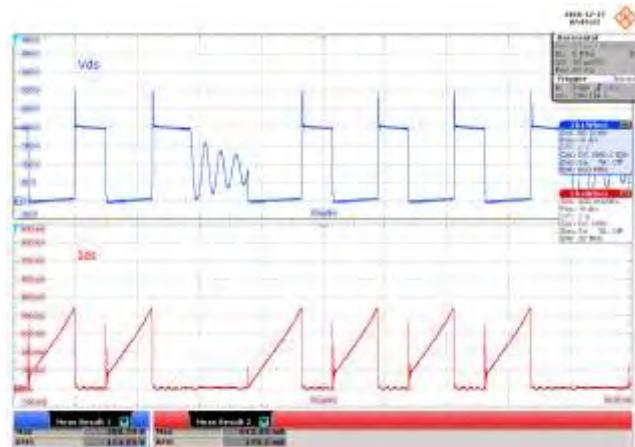


Figure 25 – 85 VAC Input.

Condition: 20 V – 500 mA.
Upper: V_{DS} , 50 V / div.
Lower: I_{DS} , 100 mA / div., 10 μ s / div.
 V_{DSMAX} : 300.79 V.
 I_{DSMAX} : 443.48 mA.

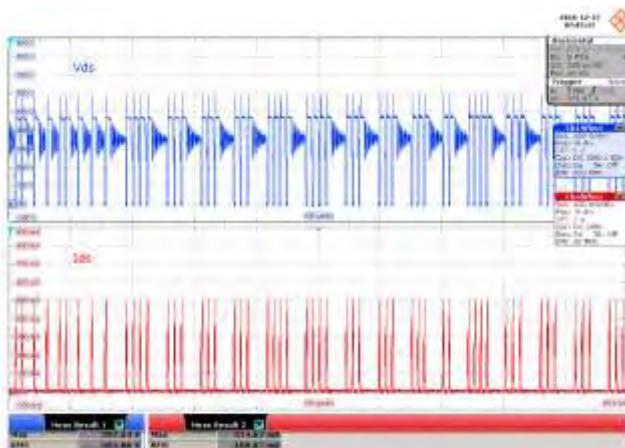


Figure 26 – 265 VAC Input.

Condition: 20 V – 500 mA.
Upper: V_{DS} , 100 V / div.
Lower: I_{DS} , 100 mA / div., 100 μ s / div.

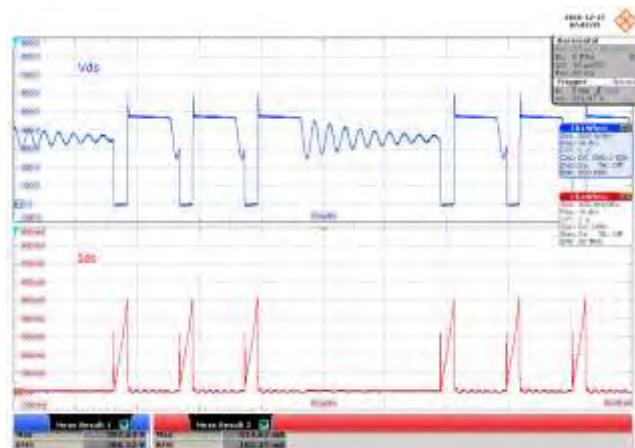


Figure 27 – 265 VAC Input.

Condition: 20 V – 500 mA.
Upper: V_{DS} , 100 V / div.
Lower: I_{DS} , 100 mA / div., 10 μ s / div.
 V_{DSMAX} : 597.63 V.
 I_{DSMAX} : 514.62 mA.

11.2.2 Freewheeling Diode

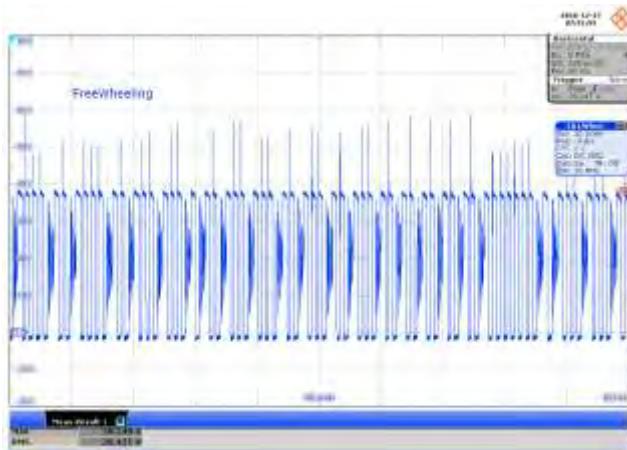


Figure 28 – 85 VAC Input.

Condition: 20 V – 500 mA.
 V_{FWL} , 10 V / div., 100 μ s / div.

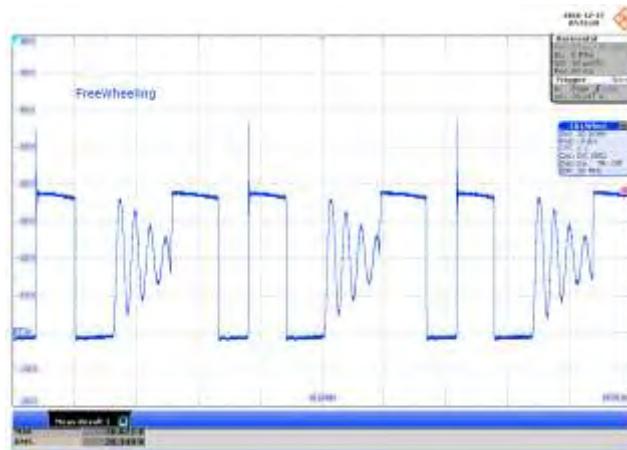


Figure 29 – 85 VAC Input.

Condition: 20 V – 500 mA.
 V_{FWL} , 10 V / div., 10 μ s / div.
 V_{FWLMAX} : 56.877 V.

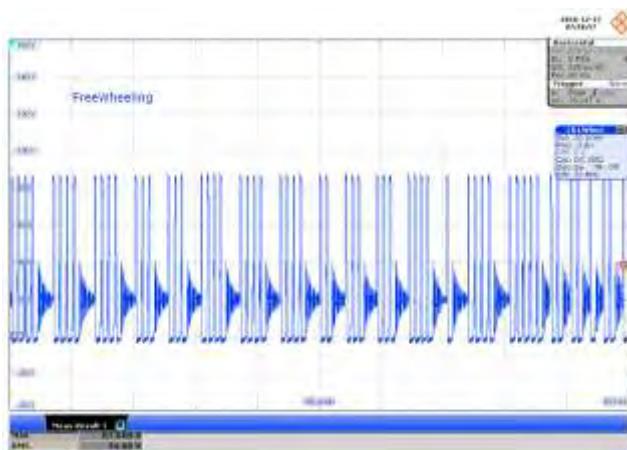


Figure 30 – 265 VAC Input.

Condition: 20 V – 500 mA.
 V_{FWL} , 20 V / div., 100 μ s / div.

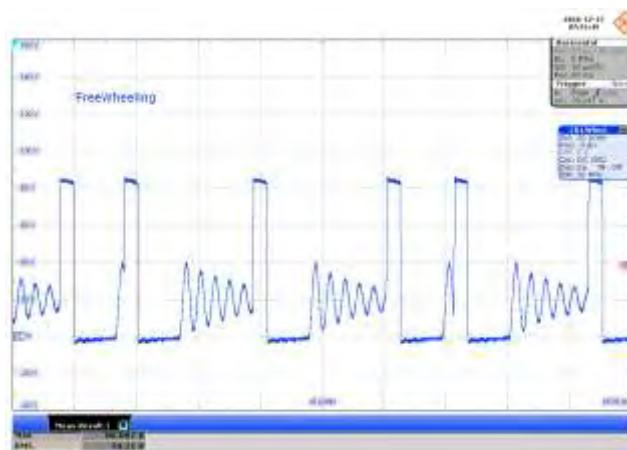


Figure 31 – 265 VAC Input.

Condition: 20 V – 500 mA.
 V_{FWL} , 20 V / div., 10 μ s / div.
 V_{FWLMAX} : 86.087 V.



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11.2.3 Start-up Waveforms

11.2.3.1 Input, Output Voltages and Output Current

Measured at the board output terminals with $40\ \Omega$ resistive load.

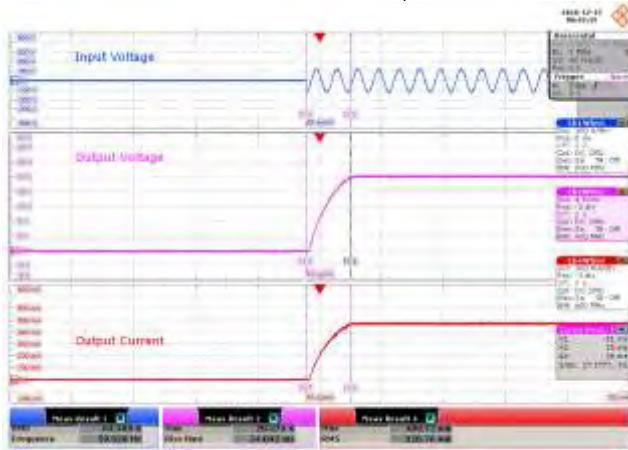


Figure 32 – 85 VAC Input.

Condition: 20 V – 500 mA.
Upper: V_{IN} , 100 V / div.
Middle: V_{OUT} , 4 V / div.
Lower: I_{OUT} , 100 mA / div., 50 ms / div.

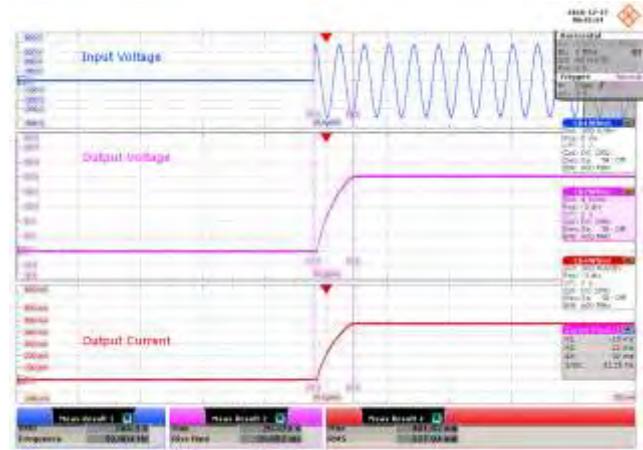


Figure 33 – 265 VAC Input.

Condition: 20 V – 500 mA.
Upper: V_{IN} , 100 V / div.
Middle: V_{OUT} , 4 V / div.
Lower: I_{OUT} , 100 mA / div., 50 ms / div.

11.2.4 Drain to Source Voltage and Current Waveforms During Start-up

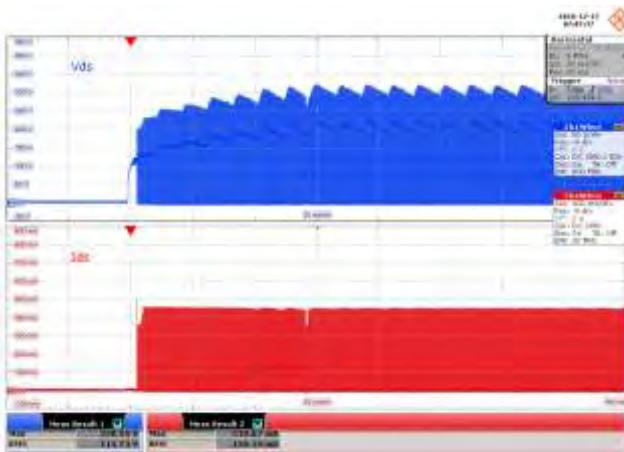


Figure 34 – 85 VAC Input.

Condition: 20 V – 500 mA.
Upper: V_{DS} , 50 V / div.
Lower: I_{DS} , 100 mA / div., 20 ms / div.

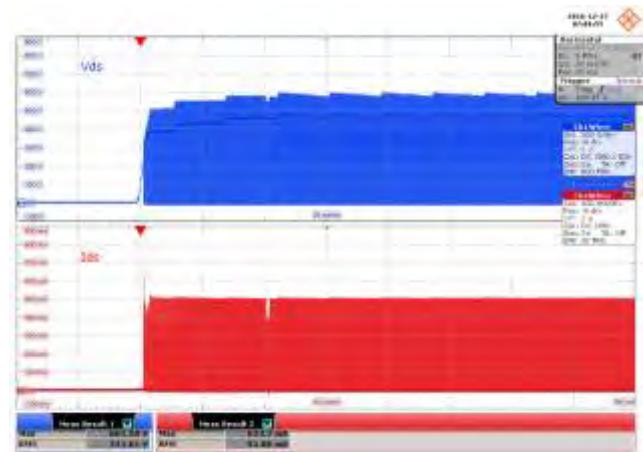


Figure 35 – 265 VAC Input.

Condition: 20 V – 500 mA.
Upper: V_{DS} , 100 V / div.
Lower: I_{DS} , 100 mA / div., 20 ms / div.

11.2.5 Output Short Auto-Restart

Short the main output and monitor I_{DS} , output voltage and output current. Auto-restart is typically <2.0 seconds.

11.2.5.1 Short During Start-Up Operation



Figure 36 – 85 VAC Input. Condition: 20 V – Shorted.
Auto-Restart: 1.495 s.
Upper: I_{DS} , 100 mA / div.
Middle: V_{OUT} , 1 V / div.
Lower: I_{OUT} , 400 mA / div., 500 ms / div.

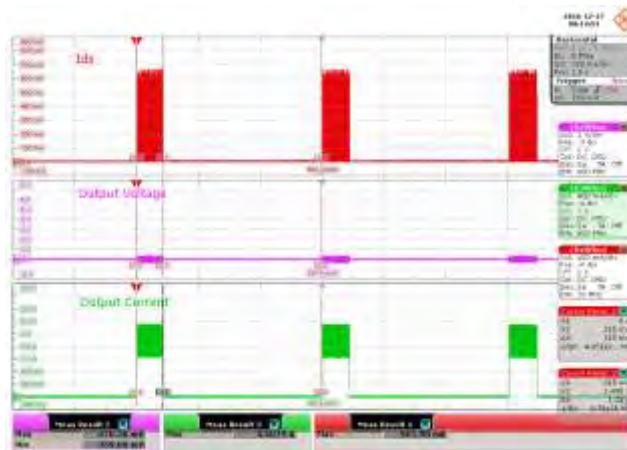


Figure 37 – 265 VAC Input. Condition: 20 V – Shorted.
Auto-Restart: 1.495 s.
Upper: I_{DS} , 100 mA / div.
Middle: V_{OUT} , 1 V / div.
Lower: I_{OUT} , 400 mA / div., 500 ms / div.

11.2.5.2 Short During Normal Operation

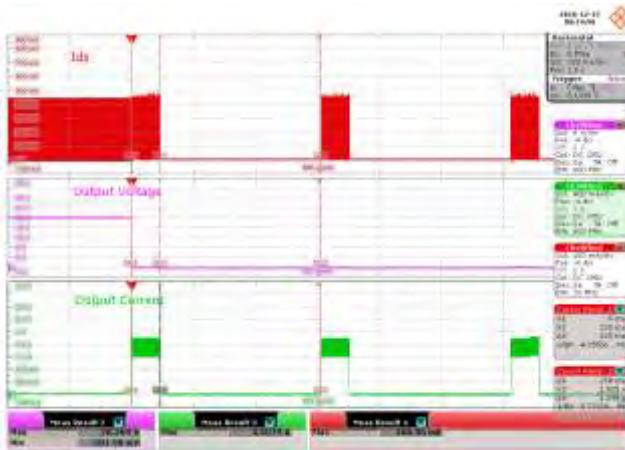


Figure 38 – 85 VAC Input. Condition: 20 V – Shorted.
Auto-Restart: 1.525 s.
Upper: I_{DS} , 100 mA / div.
Middle: V_{OUT} , 4 V / div.
Lower: I_{OUT} , 400 mA / div., 500 ms / div.



Figure 39 – 265 VAC Input. Condition: 20 V – Shorted.
Auto-Restart: 1.51 s.
Upper: I_{DS} , 100 mA / div.
Middle: V_{OUT} , 4 V / div.
Lower: I_{OUT} , 400 mA / div., 500 ms / div.



12 Thermal Performance

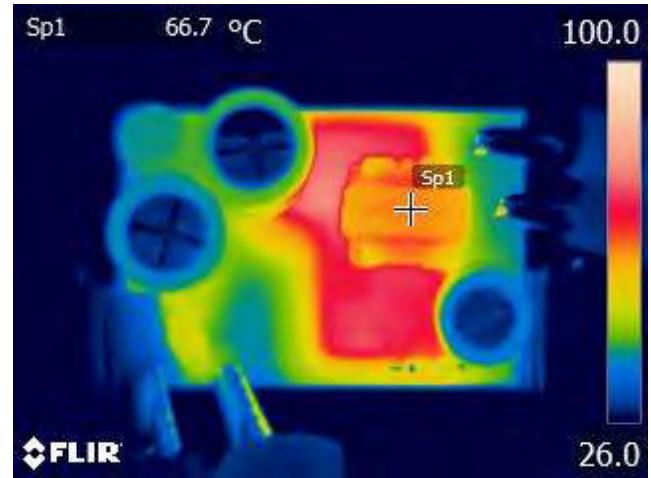
12.1 Open Case

For thermal measurement, soak the power supply first for 2 hours. It is recommended that the power supply be placed in an enclosure box to ensure a controlled environment. Add a thermocouple to monitor ambient temperature.

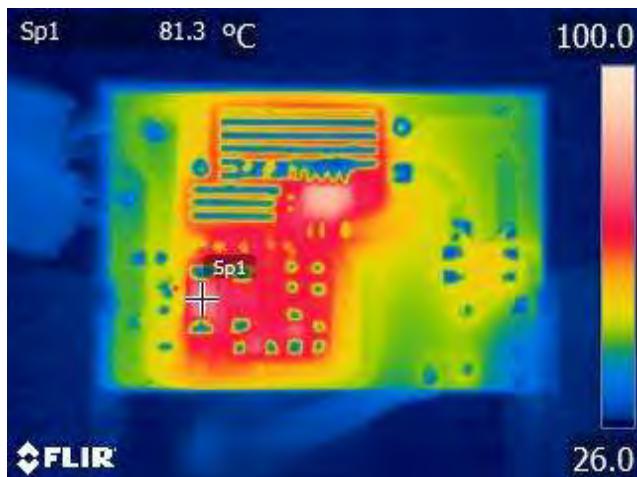
12.1.1 85 VAC at Room Temperature



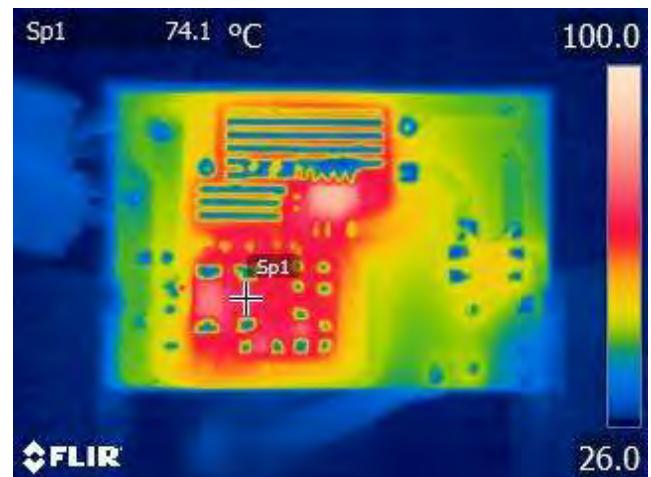
U1 – LinkSwitch-CV.
Spot Temperature – 89.2 °C.



T1 – Transformer.
Spot Temperature – 66.7 °C.



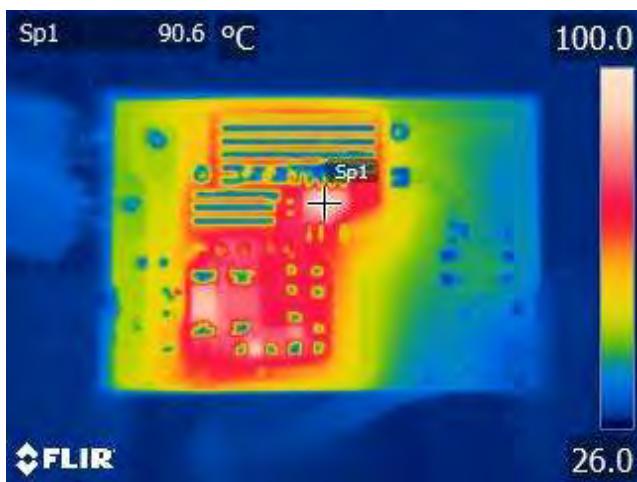
D1 – Freewheel Diode.
Spot Temperature – 81.3 °C.



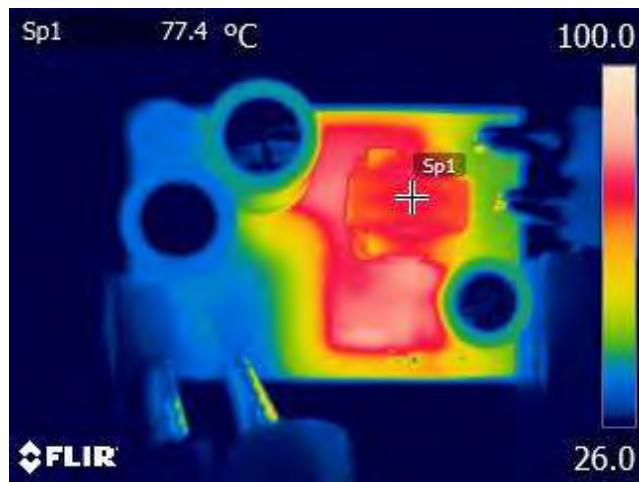
D2 – Snubber diode.
Spot Temperature – 74.1 °C.

Figure 40 – Measured Temperature at 10 W with an Ambient Temperature of 26.0 °C.

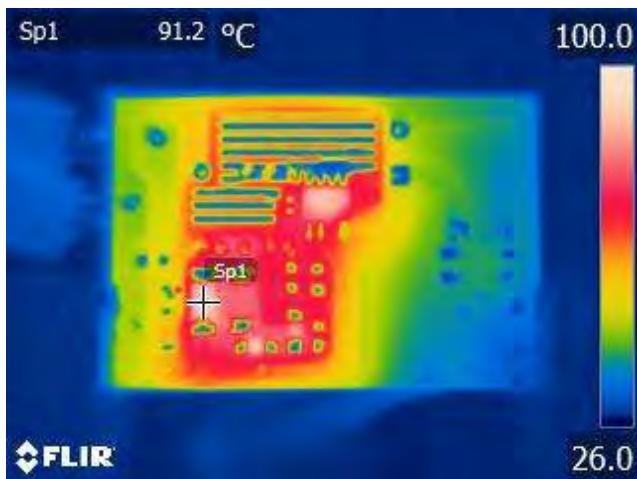
12.1.2 265 VAC at Room Temperature



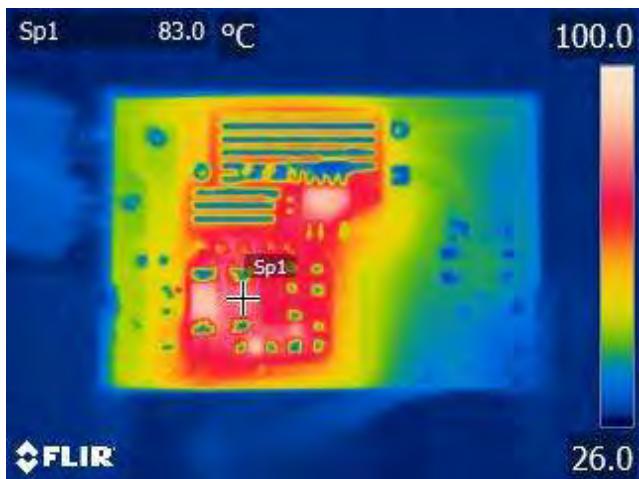
U1 – LinkSwitch-CV.
Spot Temperature – 90.6 °C.



T1 – Transformer.
Spot Temperature – 77.4 °C.



D1 – Freewheel Diode.
Spot Temperature – 91.2 °C.



D2 – Snubber diode.
Spot Temperature – 83.0 °C.

Figure 41 – Measured Temperature at 10 W with an Ambient Temperature of 26.0 °C.



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13 Conducted EMI

13.1 Test Set-up Equipment

13.1.1 Equipment and Load Used

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Hioki 3322 power meter Hi-tester.
4. Chroma measurement test fixture.

13.1.2 Test Set-up

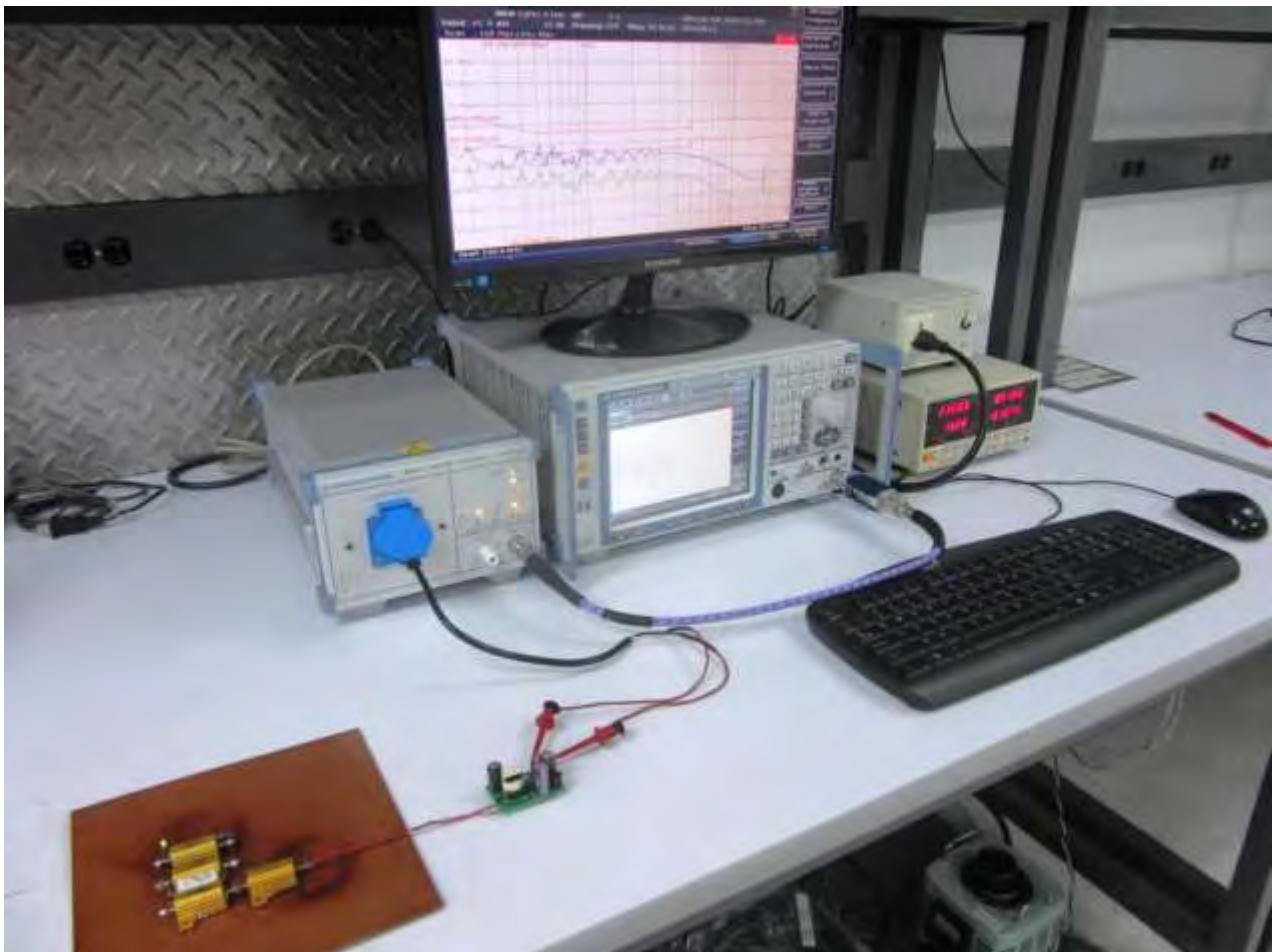


Figure 42 – EMI Test Set-up.

13.2 Floating Output (QP / AV)

13.2.1 115 VAC



Figure 43 – Floating Negative Output at 115 VAC, Line.



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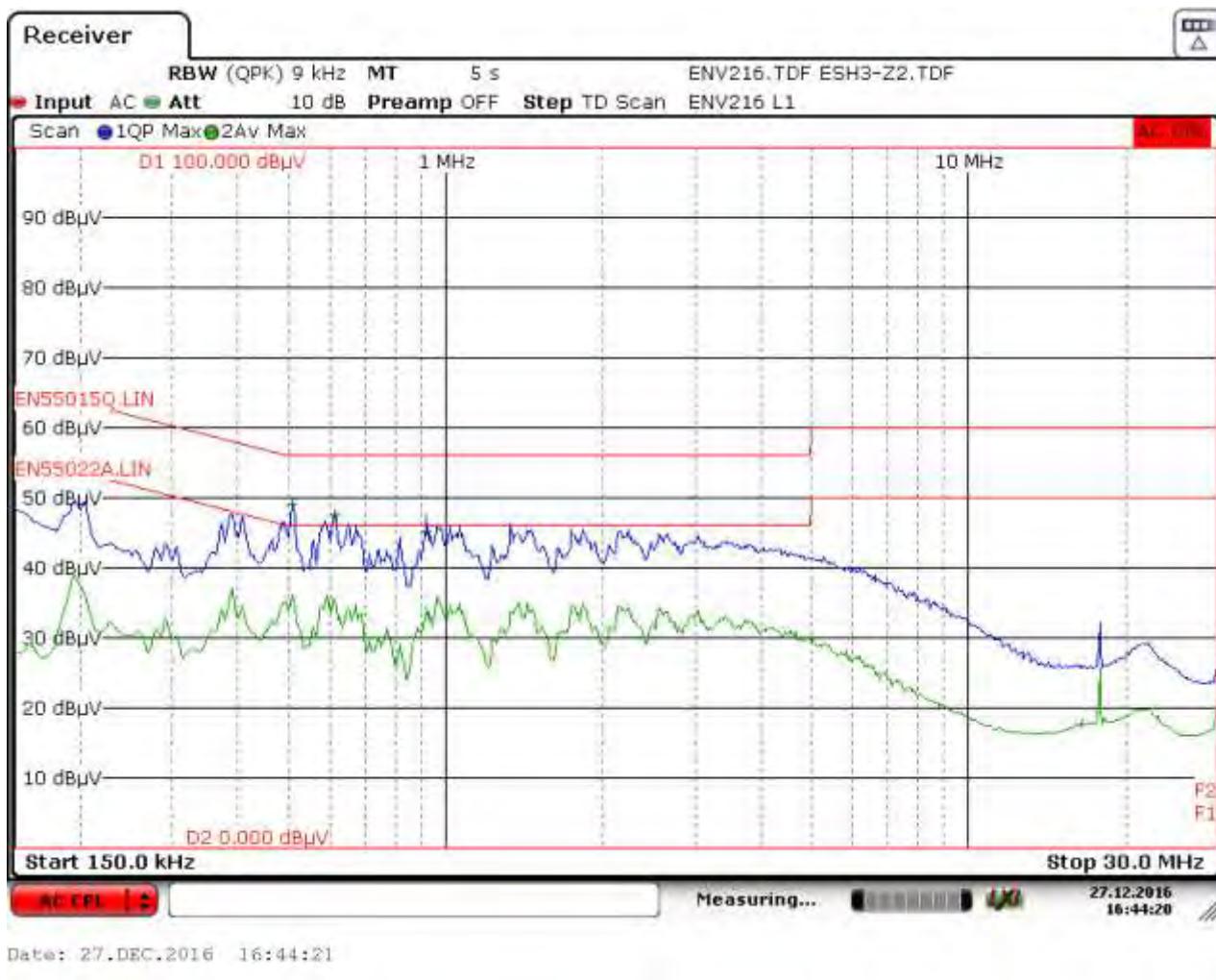
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Figure 44 – Floating Negative Output at 115 VAC, Neutral.

13.2.2 230 VAC

**Figure 45** – Floating Negative Output at 230 VAC, Line.**Power Integrations, Inc.**Tel: +1 408 414 9200 Fax: +1 408 414 9201
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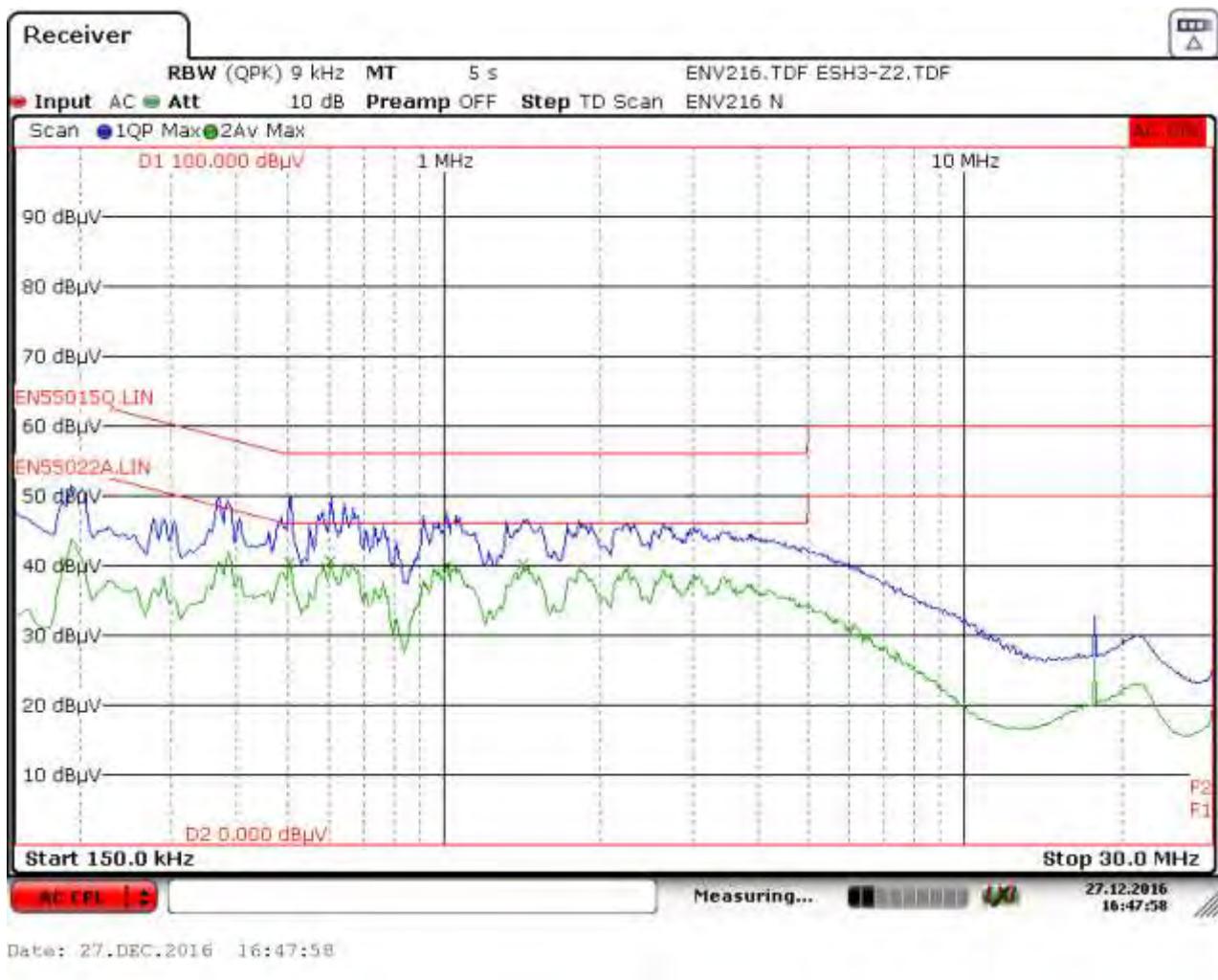


Figure 46 – Floating Negative Output at 230 VAC, Neutral.

Test condition: 10 W (20 V full load, 40 Ω resistive load)

14 Surge Test (IEC 61000-4-5)

The unit was subjected to ± 1000 V, differential surge using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

Ring Wave Voltage (kV)	Phase Angle (°)	Generator Impedance (Ω)	Injection Location	Number of Strikes	Test Result
+1	0	2	L to N	10	PASS
+1	90	2	L to N	10	PASS
+1	180	2	L to N	10	PASS
+1	270	2	L to N	10	PASS
-1	0	2	L to N	10	PASS
-1	90	2	L to N	10	PASS
-1	180	2	L to N	10	PASS
-1	270	2	L to N	10	PASS



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15 Revision History

Date	Author	Revision	Description & Changes	Reviewed
10-Jan-17	CC	1.0	Initial Release	Mktg & Apps



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