Title	***Reference Design Report for a 50 W 3-Phase Inverter Using BridgeSwitch™ BRD1260C***
Specification	270 VDC – 365 VDC Input; 50 W Continuous Inverter Output Power, 0.22 A Continuous Motor RMS Current
Application	High-Voltage Brushless DC (BLDC) Motor for Fan Application
Author	Applications Engineering Department
Document No.	RDR-851
Date	February 4, 2020
Revision	1.0

Summary and Features

- BridgeSwitch – high-voltage half-bridge motor driver
  - Integrated 600 V FREDFETs with ultra-soft, fast recovery diodes
- Three-phase inverter design for high-voltage BLDC fan applications up to 50 W
- Fully self-biased operation on the BridgeSwitch devices with an on-board external bias option
- Instantaneous phase current output signal on each BridgeSwitch device
- Single wire status update communication bus
- External system sensing input
- Integrated high-side and low-side cycle-by-cycle current limit on each BridgeSwitch devices
- Device over-temperature protection
- High-voltage bus monitor with four undervoltage threshold and one overvoltage threshold
- PCB size customized for inverter fan designs – 88 mm diameter round shaped PCB in double-sided layout
- Enhanced PCB clearance / creepage >2.2 mm
- No external heat sink
- Supports trapezoidal and sinusoidal commutation control schemes

Power Integrations, Inc.
5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 (408) 414-9200 Fax: +1 (408) 414-9201
www.power.com

Table of Contents

Important Note:
During operation, the design example board is subject to hazards including high voltages, rotating parts, bare wires, and hot surfaces. Energized DC bus capacitors require time to discharge after DC input disconnection.

All testing should use an isolation transformer to provide the DC input to the board.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

1 Introduction

This document is an engineering report describing a 3-phase inverter reference design board based on the BridgeSwitch motor driver IC that targets high-voltage BLDC fan applications. The inverter board drives a 3-phase BLDC fan motor up to 0.22 A_{RMS} motor current with >93% efficiency without using external heat sink. The design incorporates a complete inverter stage with a control input interface to facilitate various control schemes with the addition of a system sensing input, instantaneous phase current output signals from each BridgesSwitch device, a status communication bus output and an optional input for device external-bias operation.

The inverter stage is implemented using three fully integrated BridgeSwitch (BRD1260C) devices in a small footprint surface mount InSOP-24C package with exposed pads that enable heat sinking through PCB.

This document contains the inverter specifications, circuit schematic, bill of materials, printed circuit board layout, the inverter performance, inverter manual and the bench test setup.

Performance data of the board is collected with the inverter operating in a sine wave drive control scheme operating at 20 kHz PWM frequency. For this purpose, the on-board control input connector interfaces to an external sinusoidal motor driver IC.

Figure 1 – Populated Circuit Board Photograph.

2 Inverter Specification

The table below provides the electrical specification of the 3-phase inverter design. The results section provides actual performance data.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	270	310	365	V	High-Voltage DC Bus.
Power	P_{IN}		53		W	
Output						
Power	P_{OUT}		50		W	Inverter Output.
Motor Current	$I_{MOT(RMS)}$		0.22		A	Continuous RMS Current.
	$I_{MOT(PK)}$			0.70	A	Peak Current.
Motor Output Speed	ω		1800		RPM	Motor Speed at 50 W Inverter Output.
PWM Carrier Frequency	F_{PWM}		20		kHz	Sinusoidal Control PWM Frequency.
Efficiency						
Full load	ζ		95		%	50 W Output in Self-Supplied Operation .
Environmental						
Ambient Temperature	T_{AMB}	-20	25	65	°C	Free Convection
Device Case Temperature	$T_{PACKAGE}$			100	°C	0.22 A_{RMS} Motor Current in Self-Supplied Operation with BridgeSwitch BRD1260C .
DC Bus Sensing[1]						
OV Threshold	V_{OV}		422		V	Reported Through Status Communication Bus.
1st UV Threshold	V_{UV100}		247		V	
2nd UV Threshold	V_{UV85}		212		V	
3rd UV Threshold	V_{UV60}		177		V	
4th UV Threshold	V_{UV55}		142		V	
Overcurrent Protection[2]						
Internal HS / LS FREDFET Over-current Threshold	I_{OC}		0.7		A	BridgeSwitch BRD1260C Default Current Limit

Notes:
[1] Externally programmable through SM pin sensing resistor
[2] Externally programmable through XL/XH pin resistors (0.7 A default current limit at 44.2 kΩ)

Table 1 – Inverter Specification.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

3 Schematic

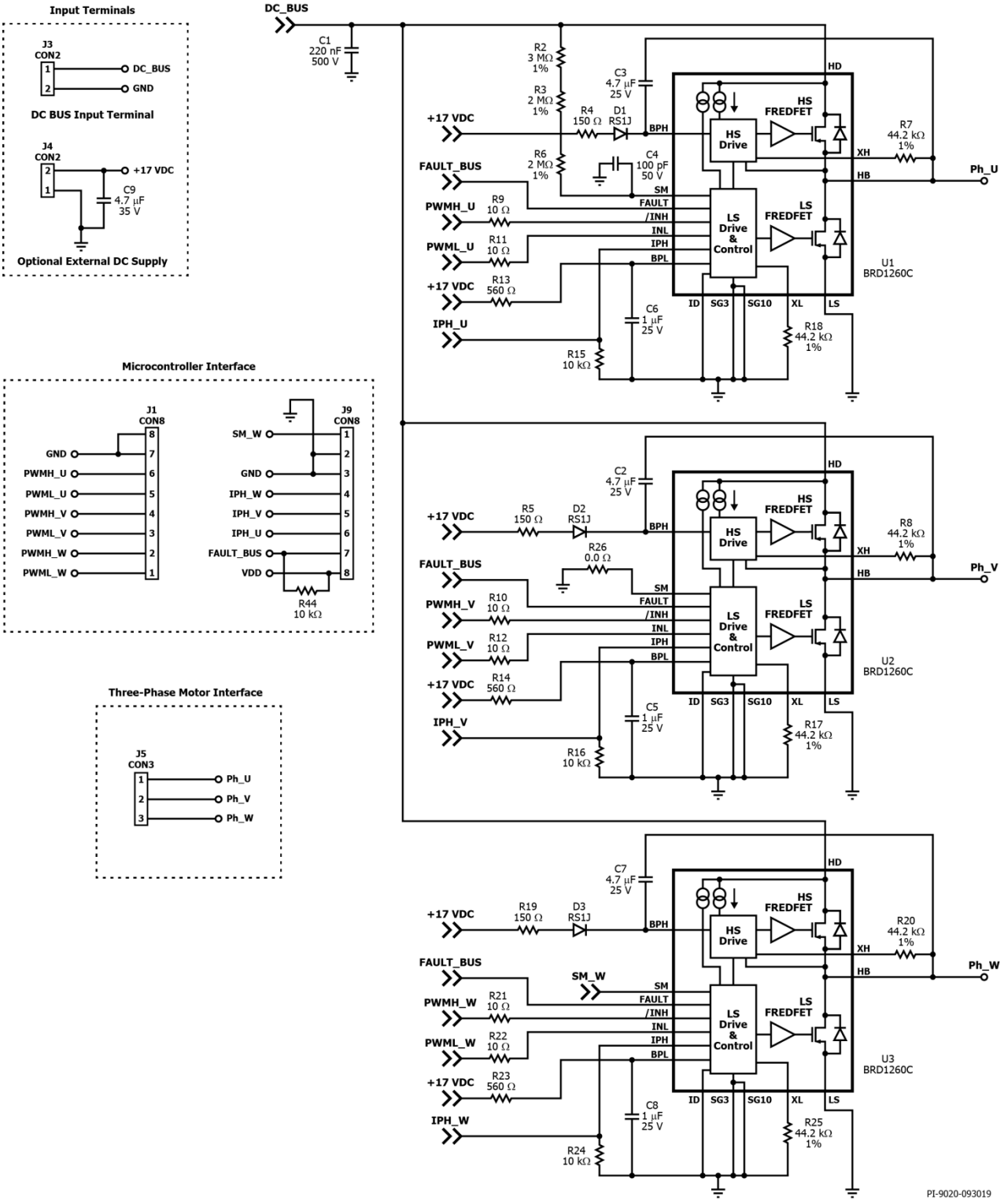

Figure 2 – BridgeSwitch 3-Phase Inverter Power Stage Schematic.

4 Circuit Description

The schematic in Figure 2 shows a 3-phase inverter employing three BRD1260C devices. The circuit enables driving a high-voltage, 3-phase brushless DC (BLDC) motor from a rectified AC input voltage. The signal control interface allows driving the inverter with various control schemes such as six-step and sinusoidal control. BridgeSwitch integrates two N-channel 600 V rated power FREDFETs, gate drivers and controllers into a low profile surface mount package IC. The power FREDFETs feature ultra-soft, fast recovery diodes ideally suited for hard switched inverter drives. Both drivers are fully self-supplied eliminating the need for an external power supply for the design. An optional device power supply input allows external bias operation for applications that require a very low inverter no load input power or operate at elevated ambient temperatures.

BridgeSwitch has device internal fault protection and system-level monitoring. Internal fault protection includes cycle-by-cycle current limit for both FREDFETs and two-level thermal overload protection. System level monitoring includes high-voltage DC bus sensing with multi-level under-voltage thresholds and one overvoltage threshold as well as driving external sensors such as a thermistor for system temperature monitoring. This design example employs a DC bus sensing on one device and provides a system sense input on another device. Half-bridge phase current (low-side FREDFET instantaneous current) information is provided through its instantaneous phase current output IPH pin. A single-wire open-drain bus communicates all detected fault or status change conditions to the system microcontroller. The system sense input, instantaneous phase current output, status communication bus, and the inverter control inputs are available through the board interface connectors.

4.1 *High-Voltage Input*

The high-voltage DC input connects to the input terminal J3. Capacitor C1 provides decoupling of the high-voltage DC bus local to the BridgeSwitch devices U1, U2 and U3.

4.2 *Three-phase Inverter Stage*

The three BridgeSwitch devices U1, U2, and U3 form the 3-phase inverter.

4.2.1 Self-Supply Operation

Capacitors C6, C5, and C8 provide self-supply decoupling for the integrated low-side controller and gate driver. Internal high-voltage current sources recharge them as soon as the voltage level starts to dip. Capacitors C3, C2, and C7 provide self-supply decoupling for the integrated high-side controller and gate driver. Internal high-voltage current sources recharge them whenever the half-bridge point of the respective device drops to the low-side source voltage level (i.e. the low-side FREDFET turns on).

4.2.2 Control Inputs

Control input signals PWMH_U, PWML_U, PWMH_V, PWML_V, PWMH_W, and PWML_W control the switching state of the integrated high side and low side power FREDFETs.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

These control input signals interface to the system microcontroller on pin 1 to 6 of connector J1. Series gate resistors R9, R11, R10, R12, R21, and R22 are placed to maintain the PWM outputs signal integrity.

4.2.3 Cycle-by-Cycle Current Limit

Resistors R18, R7, R17, R8, R25, and R20 set the cycle-by-cycle current limit level for the integrated low-side and high-side power FREDFETs. The selected value of 44.2 kΩ sets it to 100% of the default level or 0.7 A with BRD1260C.

4.2.4 Instantaneous Phase Current Information

Each BridgeSwitch device provides instantaneous phase current information of the low-side power FREDFET Drain to Source current through its IPH pin output across resistors R15, R16, and R24 respectively. With BRD1260C, the IPH pin output gain is 400 μA/A, which translates into a 2.8 V signal for a 0.7 A Drain current with the selected value of 10 kΩ. The output voltage signals are available on the pin 5, 6 and 7 on the connector J9 for the three half-bridge legs.

4.2.5 System Undervoltage and Overvoltage Monitoring and Protection

BridgeSwitch U1 monitors the DC bus voltage through resistors R2, R3, and R6. Their combined resistance of 7 MΩ sets the undervoltage thresholds to 247 V, 212 V, 177 V, and 142 V. The set bus overvoltage threshold is 422 V. Capacitor C4 provides optionally high frequency noise decoupling at the SM pin. The FAULT pin reports any detected bus voltage fault condition to the system MCU via the status communication bus.

4.2.6 External System Sense Input

BridgeSwitch U3 provides a system sense input via its SM pin, which can be connected externally, for example to an external thermistor as a system temperature sense. The FAULT pin reports any detected fault condition (the current threshold on SM pin was reached) to the system MCU via the status communication bus. The system sense input is available on the pin 1 of connector J9.

4.2.7 Status Communication Bus

Each BridgeSwitch will report any detected internal and system fault through the status communication bus located on pin 7 of connector J9. All three FAULT pins are tied together in a single wire bus using a pull-up resistor (i.e. 10 kΩ) to VDD supply. The pull-up supply (VDD) for the open-drain fault output is available on the pin 8 of connector J9.

4.2.8 Device ID

Each BridgeSwitch device assigns itself a unique device ID by configuring its ID pin connection: device U1 ID pin shorted to SG (80 μs), device U2 ID pin floating (60 μs t_{ID}), and device U3 ID pin connected to BPL pin (40 μs t_{ID}). The device ID supports status communication bus arbitration and enables communicating the physical location of a detected fault to the system microcontroller.

4.3 *Microcontroller Interface*

Connector J1 interfaces the three-phase inverter stage to the system microcontroller for the PWM inputs (PWMH_U, PWML_U, PWMH_V, PWML_V, PWMH_W and PWML_W). Connector J9 exposes the IPH outputs (IPH_U, IPH_V and IPH_W), system sense input (SM_W), status communication bus (FAULT_BUS), and the pull-up supply (VDD). Signal ground (GND) connects to pins 7 and 8 of J1 connector or to the pins 2 and 3 of J9 connector.

4.4 *External Device Supply*

The circuit also provides an external bias option to supply each of the BridgeSwitch devices from a single input rail (17 VDC recommended) through J4 connector. Capacitor C9 provides local decoupling of the external supply. Resistors R13, R14, and R23 limits the external supply current on the BPL pin of the respective BridgeSwitch devices. These resistors should be depopulated when operating in self-supply mode to prevent BPL voltage threshold interactions. Resistors R4, R5, and R19 limits the external supply current on the BPH pin of the respective BridgeSwitch devices. While diodes D1, D2, and D3 decouple the input supply rail from the BPH pin whenever a high-voltage is present on the half-bridge point of the respective devices (i.e. the high-side FREDET turns on).

4.5 *Three-Phase Output Connector*

The outputs of the inverter connect to each phase of the high-voltage BLDC motor respectively through the interface connector J5.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

5 Printed Circuit Board Layout

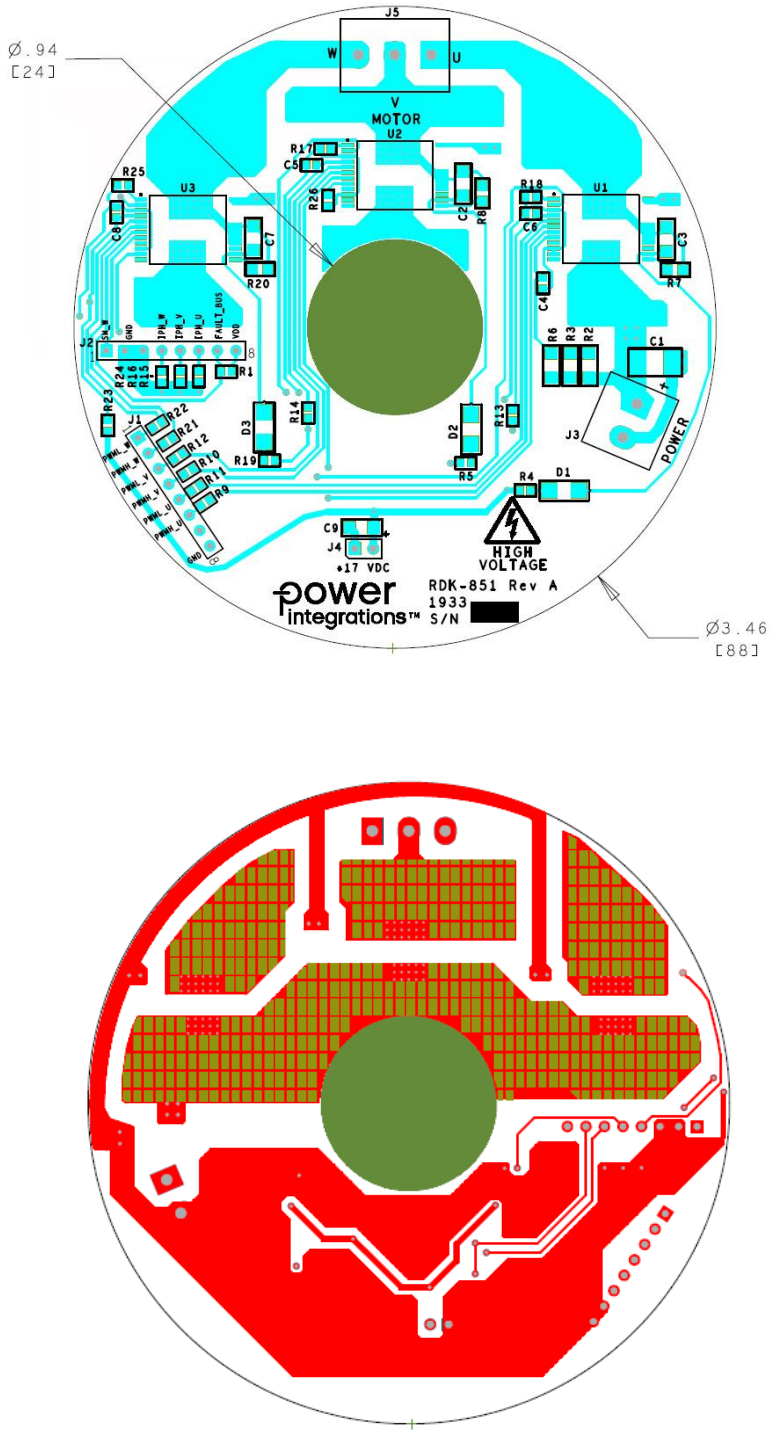

Figure 3 – Printed Circuit Board Layout Top and Bottom View.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	C1	220 nF, 500 V, Ceramic, X7R, 1812	C1812C224KCRACTU	Kemet
2	3	C2, C3, C7	4.7 μF, ±10%, 25 V, Ceramic, X7R, 1206	GCM31CR71E475KA55L	Murata
3	1	C4	100 pF 50 V, Ceramic, NP0, 0603	CC0603JRNPO9BN101	Yageo
4	3	C5, C6, C8	1 μF, ±10%, 25 V, Ceramic, X7R, 0603	CGA3E1X7R1E105K080AE	TDK
5	1	C9	4.7 μF, 35 V, Ceramic, X5R, 1206	C3216X5R1V475M085AB	TDK
6	3	D1, D2, D3	600 V, 1 A, Fast Recovery, 250 ns, SMA	RS1J-13-F	Diodes, Inc.
7	2	J1, J9	8 Position (1 x 8) header, 0.1 pitch, Vertical, Au	P9101-08-D32-1	Protectron
8	1	J3	2 Position (1 x 2) header, 5 mm (0.196) pitch, Vertical, Screw - Rising Cage Clamp	1715022	Phoenix Contact
9	1	J4	2 Position (1 x 2) header, 0.1 pitch, Vertical	22-28-4020	Molex
10	1	J5	3 Position (1 x 3) header, 5 mm (0.196) pitch, Vertical, Screw - Rising Cage Clamp	1715035	Phoenix Contact
11	1	R2	RES, 3 MΩ, 1%, 1/4 W, Thick Film, 1206	KTR18EZPF3004	Rohm Semi
12	2	R3, R6	RES, 2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
13	3	R4, R5, R19	RES, 150 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ151V	Panasonic
14	3	R7, R8, R20	RES, 44.2 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4422V	Panasonic
15	6	R9, R10, R11, R12, R21, R22	RES, 10 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ100V	Panasonic
16	3	R13, R14, R23	RES, 560 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ561V	Panasonic
17	3	R15, R16, R24	RES, 10 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1002V	Panasonic
18	3	R17, R18, R25	RES, 44.2 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF4422V	Panasonic
19	1	R26	RES, 0 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEY0R00V	Panasonic
20	1	R44	RES, 10 kΩ, 5%, 1/10 W, 0603	ERJ-3GEYJ103V	Panasonic
21	3	U1, U2, U3	BridgeSwitch, Full Featured, Max. BLDC Motor Current 0.22 A(RMS)	BRD1260C	Power Integrations

Table 2 – Bill of Materials.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

7 Performance Data

This section presents waveform plots and performance data gathered on the RDR-851 with the test setup mentioned in the section 8.5. The performance data presented is collected with the inverter operating in a sinusoidal commutation scheme at 20 kHz PWM frequency. The inverter operates self-supplied unless noted otherwise. The HV bus voltage level is 310 VDC. Optional external supply operation uses a 17 VDC external DC supply provided to the inverter board via input connector, J4. All measurements were performed at room ambient temperature.

7.1 *Start-up Operation*

Figure 4 and 5 show the inverter start-up waveforms captured on one BridgeSwitch device (U1). Figure 4 depicts the low-side and high-side BYPASS pin voltages of one BrigeSwitch device during start-up. Figure 5 depicts the motor phase current, PWM control signals (INL and \INH) and the half-bridge voltage captured on device U1.

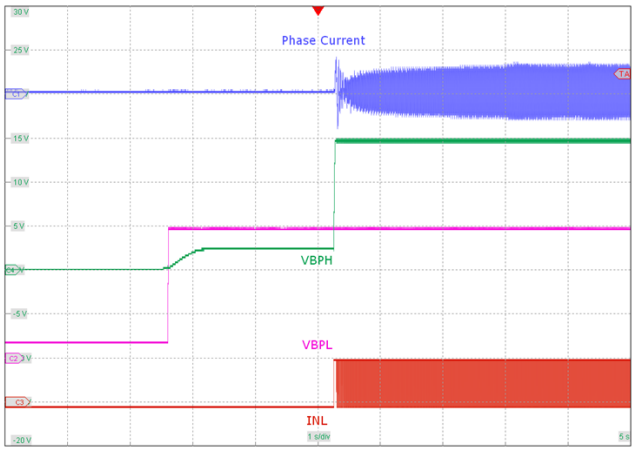

Figure 4 – BPL and BPH-pin Voltages at Start-Up
First: I_{PHASE} , 500 mA / div.
Second: V_{BPH}, 5 V / div.
Third: V_{BPL}, 5 V / div.
Fourth: V_{INL}, 5 V / div.
Time Scale: 1 s / div.

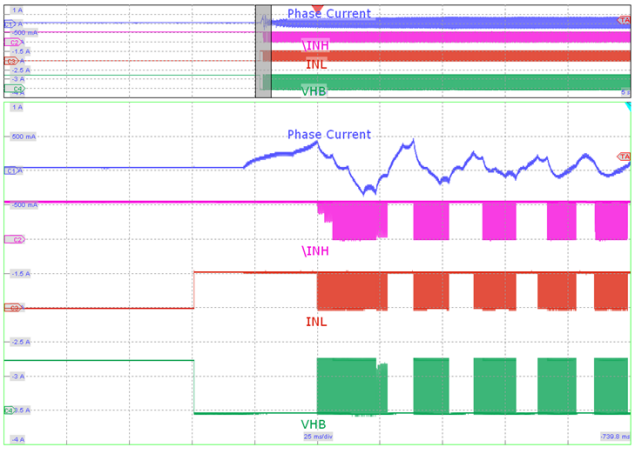

Figure 5 – Motor Start-up Waveforms
First: I_{PHASE} , 500 mA / div.
Second: $V_{/INH}$, 5 V / div.
Third: V_{INL}, 5 V / div.
Fourth: V_{HB}, 200 V / div.
Time Scale: 25 ms / div.

7.2 ***Steady-State Operation***

Figure 6 to 9 depict the motor three-phase currents and half-bridge voltage signals during steady state operation.

7.2.1 Phase Currents During Steady-State

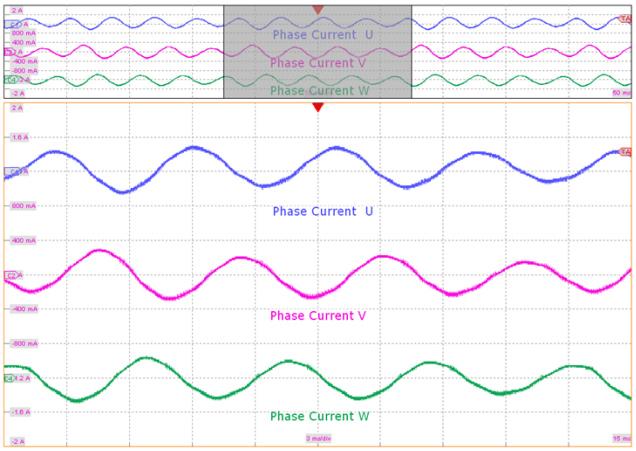

Figure 6 – At 0.15 A Motor RMS Current.
$I_{MOTOR, RMS(U)}$: 147 mA.
$I_{MOTOR, RMS(V)}$: 151 mA.
$I_{MOTOR, RMS(W)}$: 150 mA.
Upper: $I_{MOTOR(U)}$, 400 mA / div.
Middle: $I_{MOTOR(V)}$, 400 mA / div.
Lower: $I_{MOTOR(W)}$, 400 mA / div.
Time Scale: 3 ms / div.

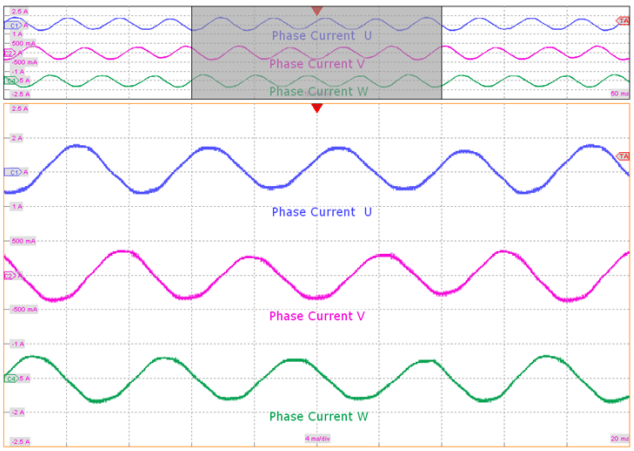

Figure 7 – At 0.22 A Motor RMS Current.
$I_{MOTOR, RMS(U)}$: 217 mA.
$I_{MOTOR, RMS(V)}$: 221 mA.
$I_{MOTOR, RMS(W)}$: 219 mA.
Upper: $I_{MOTOR(U)}$, 500 mA / div.
Middle: $I_{MOTOR(V)}$, 500 mA / div.
Lower: $I_{MOTOR(W)}$, 500 mA / div.
Time Scale: 4 ms / div.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

7.2.2 Half-Bridge Voltage Signals During Steady-State

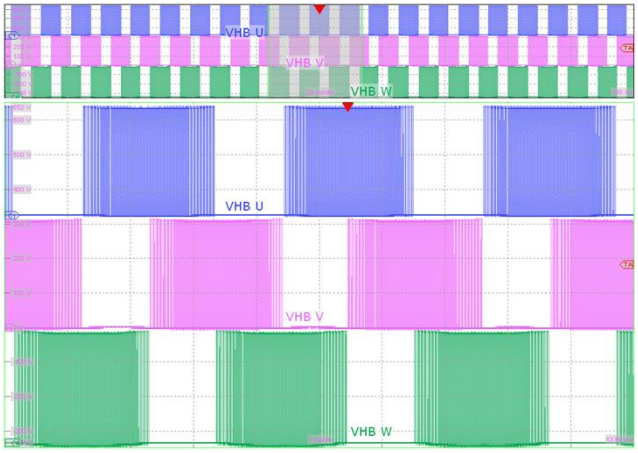

Figure 8 – At 0.15 A_{RMS} at 1800 RPM.
Upper: $V_{HB(U)}$, 100 V / div.
Middle: $V_{HB(V)}$, 100 V / div.
Lower: $V_{HB(W)}$, 100 V / div.
Time Scale: 3 ms / div.

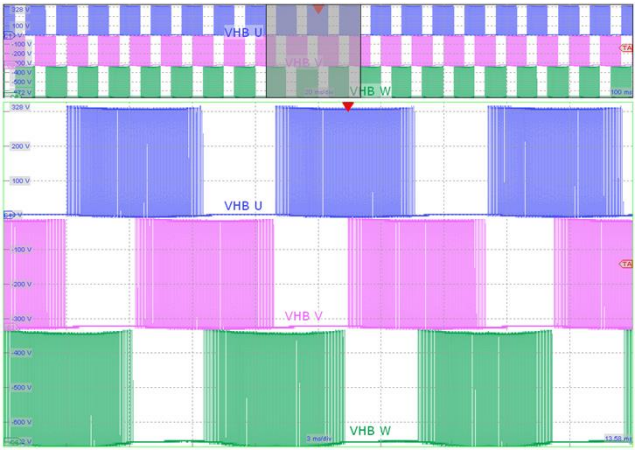

Figure 9 – At 0.22 A_{RMS} at 1800 RPM.
Upper: $V_{HB(U)}$, 100 V / div.
Middle: $V_{HB(V)}$, 100 V / div.
Lower: $V_{HB(W)}$, 100 V / div.
Time Scale: 3 ms / div.

7.2.3 /INH and INL Input Signals During Steady-State

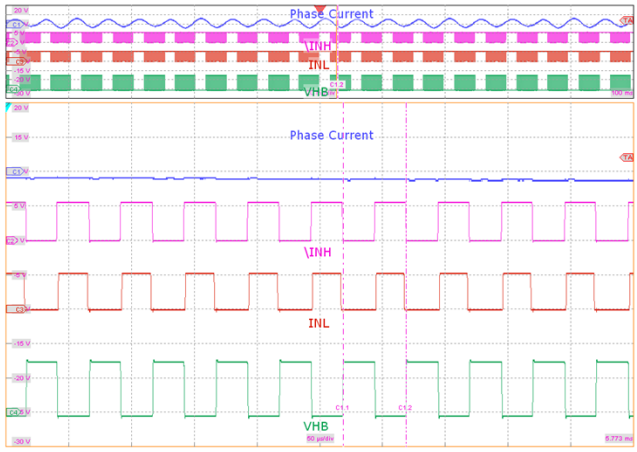

Figure 10 – At 0.15 A_{RMS} at 1800 RPM.
Upper: $V_{/INH}$, 5 V / div.
Middle: V_{INL}, 5 V / div.
Lower: V_{HB}, 200 V / div.
Time Scale: 50 µs / div.

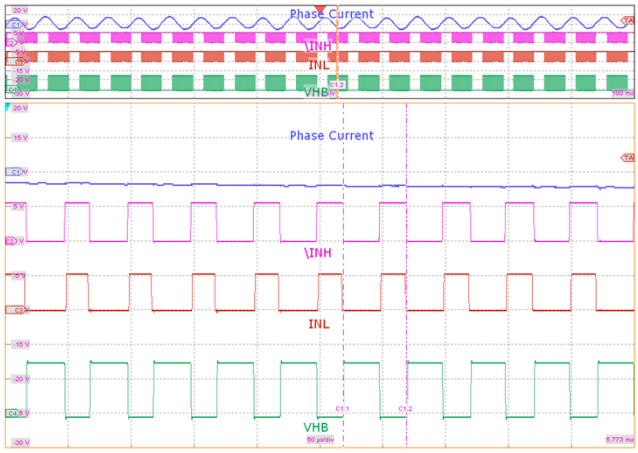

Figure 11 – At 0.22 A_{RMS} at 1800 RPM.
Upper: $V_{/INH}$, 5 V / div.
Middle: V_{INL}, 5 V / div.
Lower: V_{HB}, 200 V / div.
Time Scale: 50 µs / div.

7.2.4 BYPASS Pin Voltage Signals During Steady-State

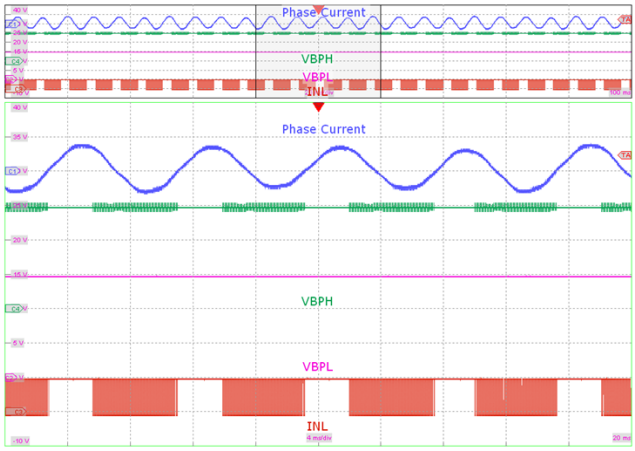

Figure 12 – At 0.15 A Motor RMS Current.
First: I_{MOTOR}, 400 mA / div.
Second: V_{BPH}, 5 V / div.
Third: V_{BPL}, 5 V / div.
Fourth: V_{INL}, 5 V / div.
Time Scale: 4 ms / div.

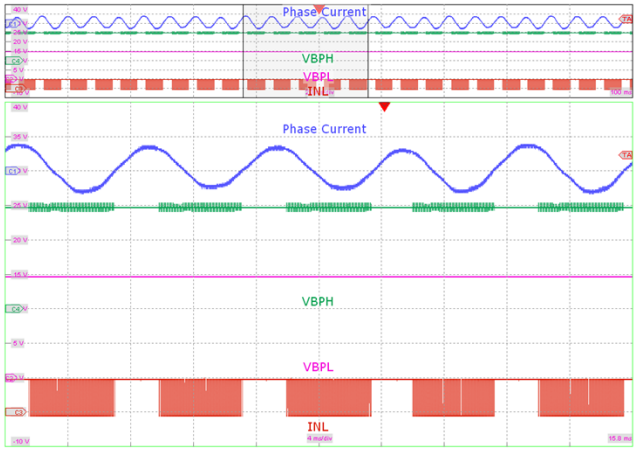

Figure 13 – At 0.22 A Motor RMS Current.
First: I_{MOTOR}, 500 mA / div.
Second: V_{BPH}, 5 V / div.
Third: V_{BPL}, 5 V / div.
Fourth: V_{INL}, 5 V / div.
Time Scale: 4 ms / div.

7.2.5 Phase Current Information Signal (IPH)

Figure 14 to Figure 15 depict the phase current waveform of device U1 and the corresponding phase current output signal available on pin 5 of connector J9.

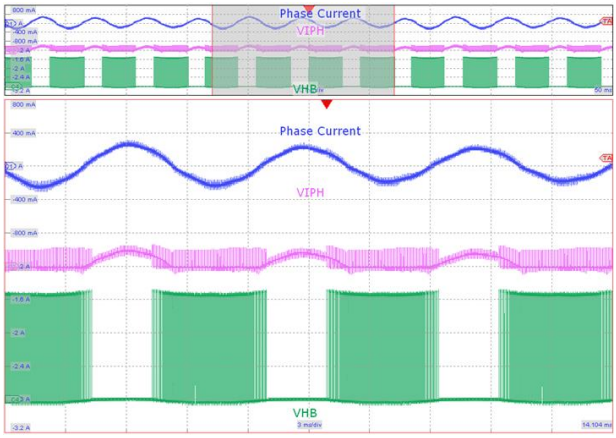

Figure 14 – At 0.15 A Motor RMS Current.
First: I_{MOTOR}, 400 mA / div.
Second: V_{IPH}, 2 V / div.
Third: V_{HB}, 100 V / div.
Time Scale: 3 ms / div.

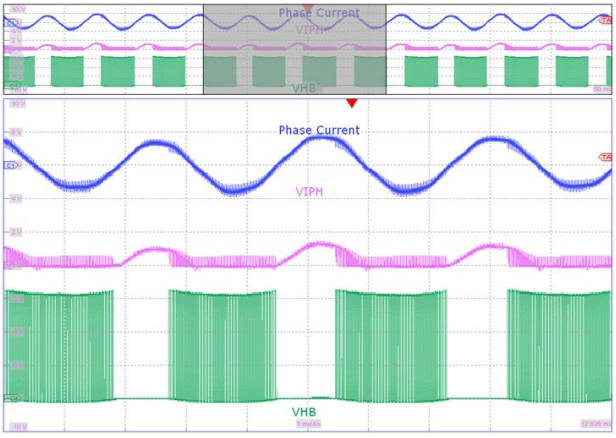

Figure 15 – At 0.22 A Motor RMS Current.
First: I_{MOTOR}, 500 mA / div.
Second: V_{IPH}, 2 V / div.
Third: V_{BPL}, 100 V / div.
Time Scale: 3 ms / div.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

7.2.6 FREDFET Drain-voltage Slew Rate at Full Load

Figure 16 and Figure 17 depict low-side FREDFET Drain voltage slew rates at turn-on and turn-off, respectively.

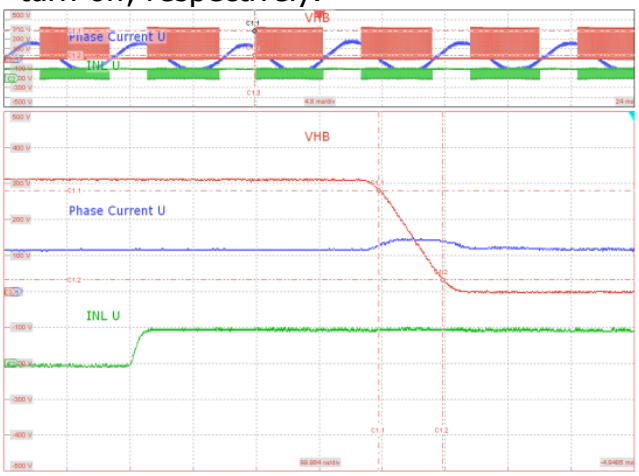

Figure 16 – Steady-State – 1800 RPM, 0.22 A_{RMS}.
Low-Side FREDFET Turn-Off.
Turn-On Voltage Slew Rate: 2.4 V / ns.
Upper: $I_{PHASE\ U}$, 200 mA / div.
Middle: V_{HB-LS}, 100 V / div.
Lower: /INH Input, 5 V / div.
Zoom: 100 ns / div.

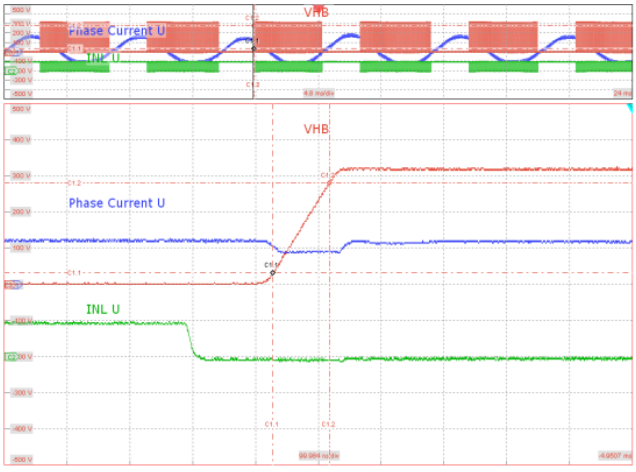

Figure 17 – Steady-State – 1800 RPM, 0.22 A_{RMS}.
Low-Side FREDFET Turn-Off.
Turn-Off Voltage Slew Rate: 2.8 V / ns.
Upper: $I_{PHASE\ U}$, 200 mA / div.
Middle: V_{HB-LS}, 100 V / div.
Lower: /INH Input, 5 V / div.
Zoom: 100 ns / div.

7.3 *Thermal Performance*

Figure 18 and Figure 19 depict the open case board thermal scan of BridgeSwitch devices (U1, U2, U3) in self-supply operation at 0.15 A and 0.22 A motor RMS current respectively at room ambient temperature.

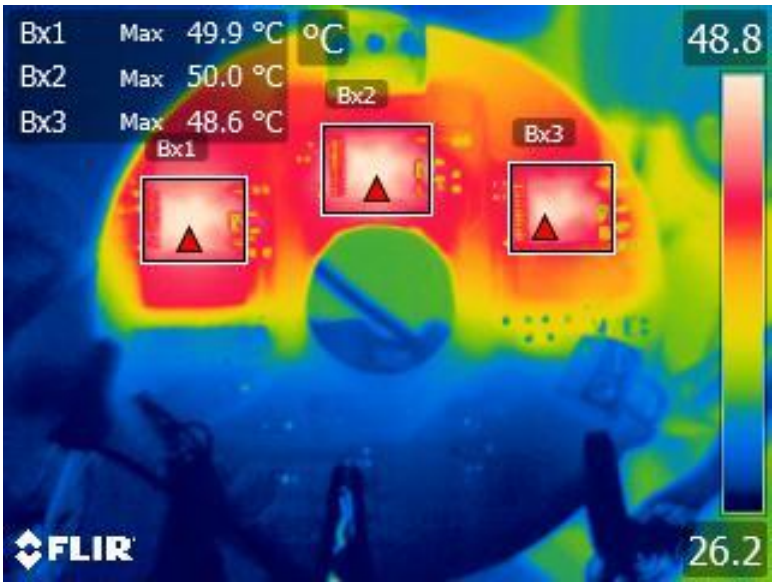

Figure 18 – Thermal Scan at 0.15 A Motor RMS Current in Self-Supply Operation.

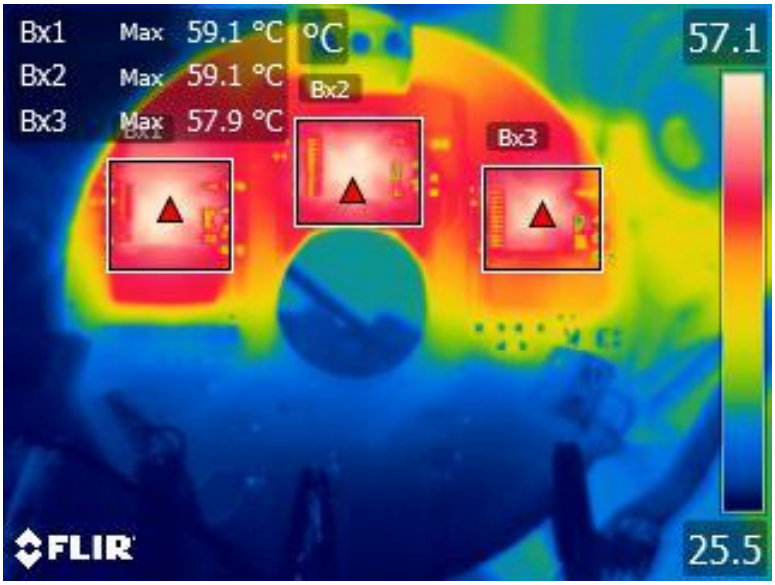

Figure 19 – Thermal Scan at 0.22 A Motor RMS Current in Self-Supply Operation.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

Figure 20 and Figure 21 depict the open case board thermal scan of BridgeSwitch devices (U1, U2, U3) while supplied externally (17 VDC applied to external DC input connector, J4) at 0.15 A and 0.22 A motor RMS current respectively at room ambient temperature.

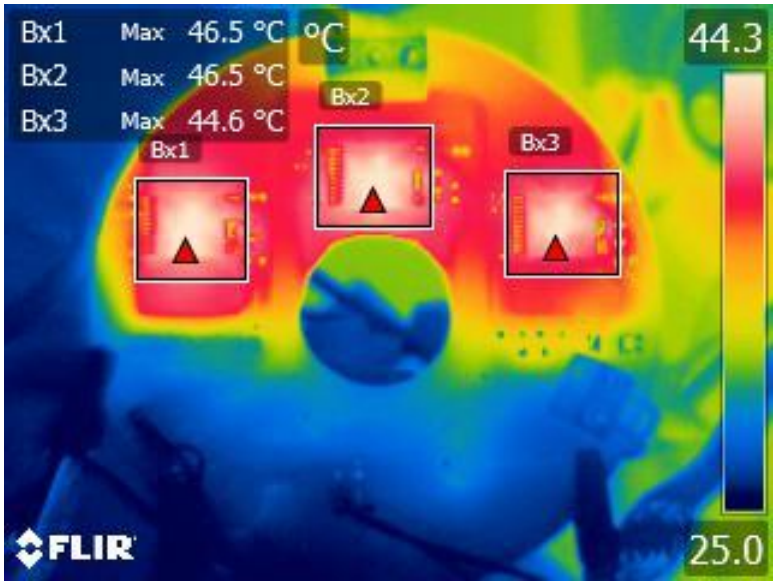

Figure 20 – Thermal Scan at 0.15 A Motor RMS Current in External-Supply Operation.

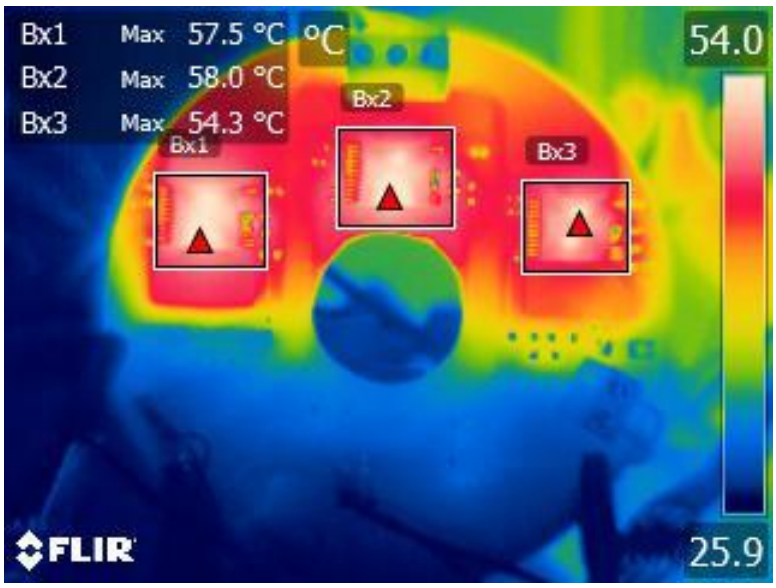

Figure 21 – Thermal Scan at 0.22 A Motor RMS Current in External-Supply Operation.

Figure 22 summarizes the device average case temperature rise above ambient with the inverter operating in self-supply and external supply mode at 310 V DC bus input, sinusoidal control at 20 kHz PWM frequency.

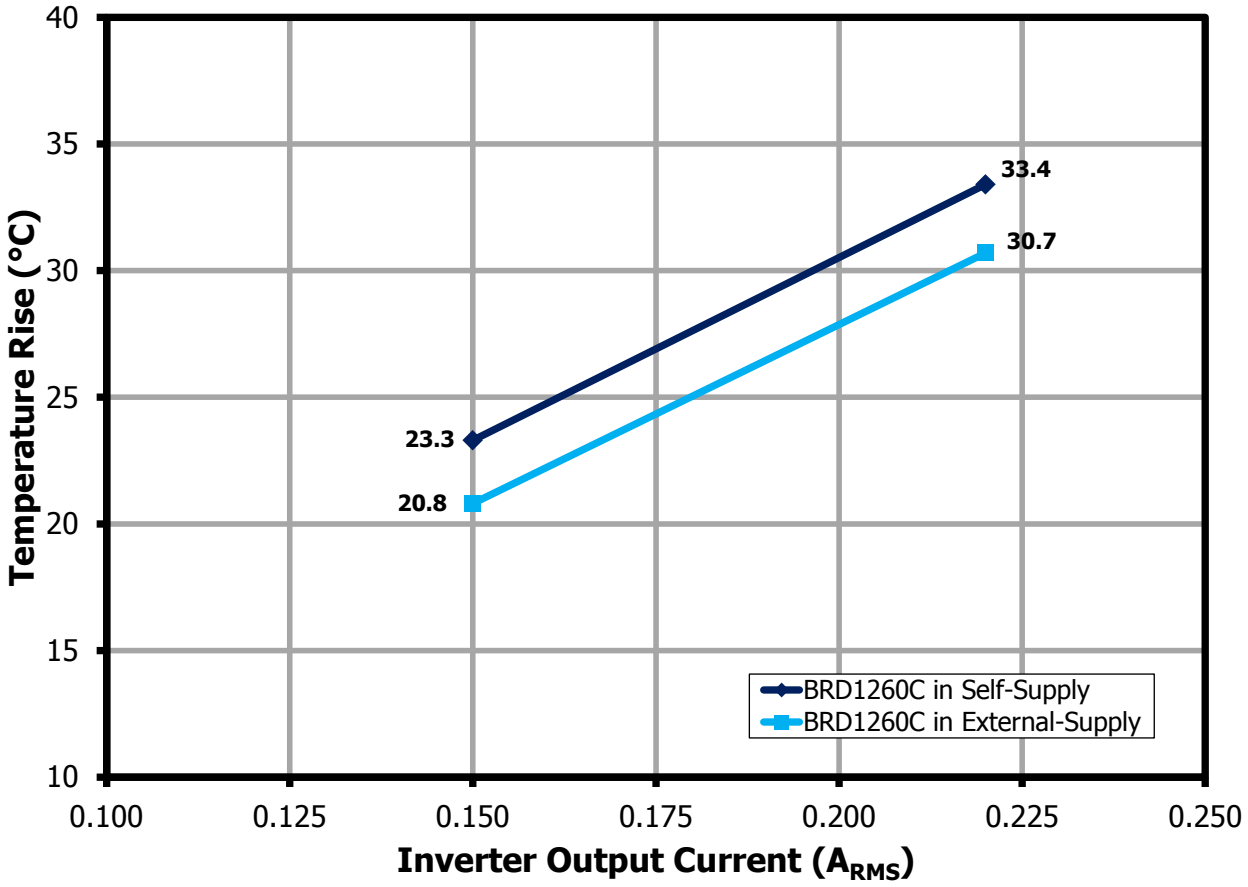

Figure 22 – Device Average Case Temperature Rise.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

7.4 *No-Load Power Consumption*

Figure 23 depicts the inverter no-load input power consumption measured across the input line voltage with the inverter operating in self-supply and external supply mode.

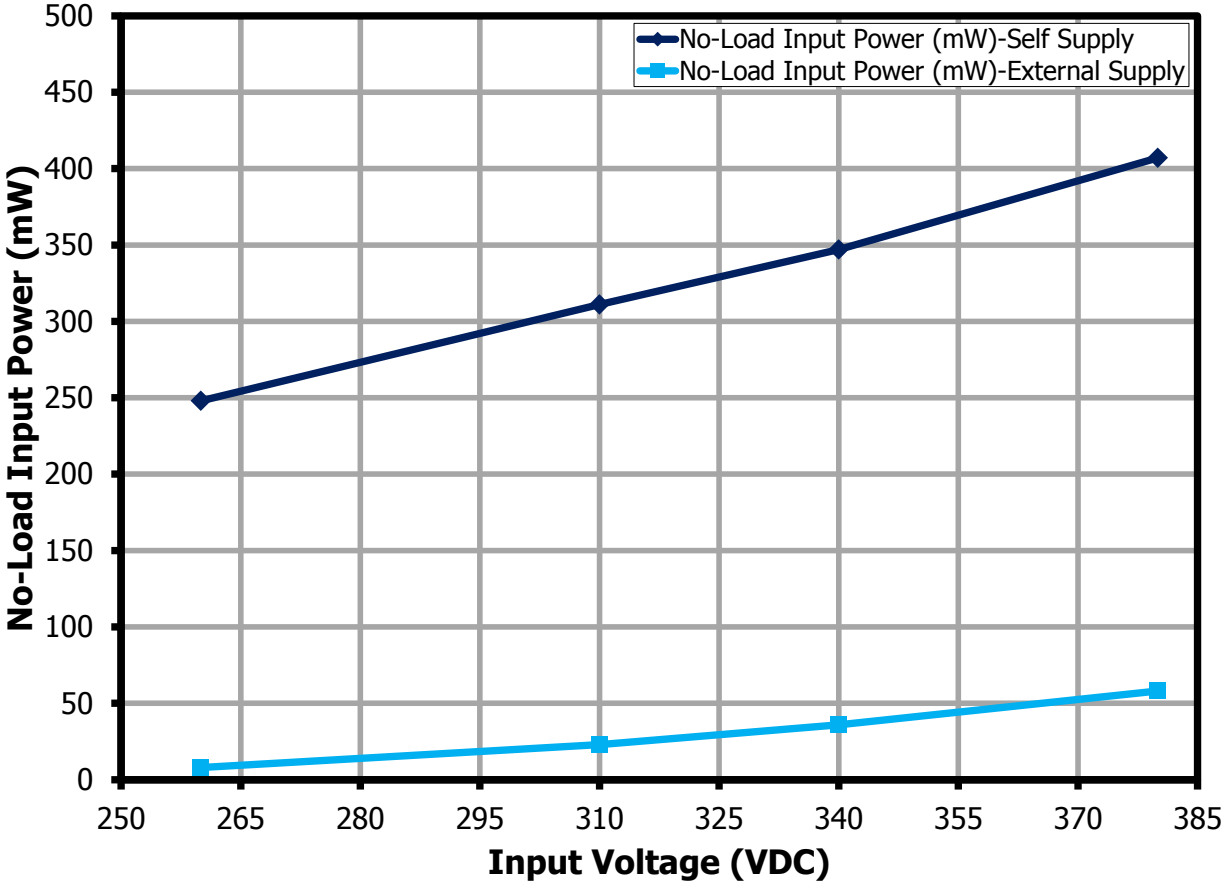

Figure 23 – No-Load Input Power.

7.5 *Efficiency*

Figure 24 depicts the inverter efficiency versus output power. Output power is measured by varying motor speed with a constant torque load applied to the motor at 0.22 A_{RMS} motor current. Table 3 and 4 shows the efficiency data described in this graph.

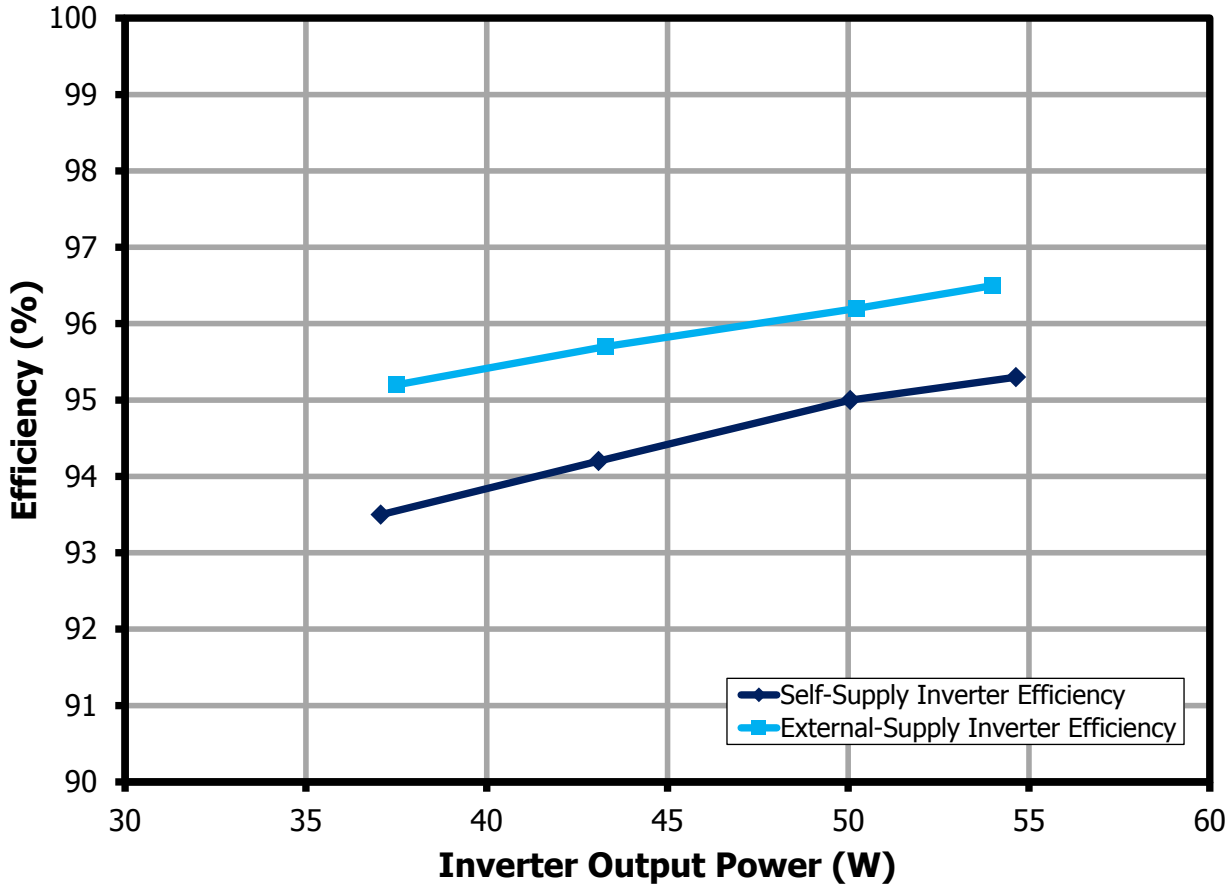

Figure 24 – Inverter Efficiency.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

Table 3 provides the efficiency data with the inverter operating in self-supply mode.

Input DC Voltage (V)	Speed (RPM)	DC Input Power (W)	Motor RMS Current Phase U (A)	Motor RMS Current Phase V (A)	Motor RMS Current Phase W (A)	Inverter Output Power (W)	Inverter Efficiency (%)
310	1255	39.66	0.220	0.220	0.220	37.07	93.5
310	1500	45.74	0.220	0.230	0.220	43.10	94.2
310	1830	52.71	0.220	0.230	0.220	50.06	95.0
310	2010	57.36	0.230	0.230	0.230	54.64	95.3

Table 3 – Self-supply Inverter Efficiency Data.

Table 4 provides the efficiency data with the inverter operating in external-supply mode.

Input DC Voltage (V)	Speed (RPM)	DC Input Power (W)	Motor RMS Current Phase U (A)	Motor RMS Current Phase V (A)	Motor RMS Current Phase W (A)	Inverter Output Power (W)	Inverter Efficiency (%)
310	1245	39.43	0.220	0.220	0.220	37.52	95.2
310	1500	45.25	0.220	0.230	0.220	43.30	95.7
310	1825	52.22	0.220	0.230	0.220	50.24	96.2
310	2040	55.96	0.220	0.220	0.220	54.01	96.5

Table 4 – External-supply Inverter Efficiency Data.

7.6 *Device and System Level Protection and Monitoring*

This section demonstrates the device integrated and system-level protection and monitoring feature. Each device communicates its status including device or system level fault through the status communication bus (FAULT bus). The status communication bus is available through pin 7 of connector J9 (open-drain pin that connects to an external VDD pull-up supply).

7.6.1 Device Level Protection

Figure 25 and Figure 26 depict the integrated current limit function at device U3 (phase W) and the associated status update reported on the FAULT bus.

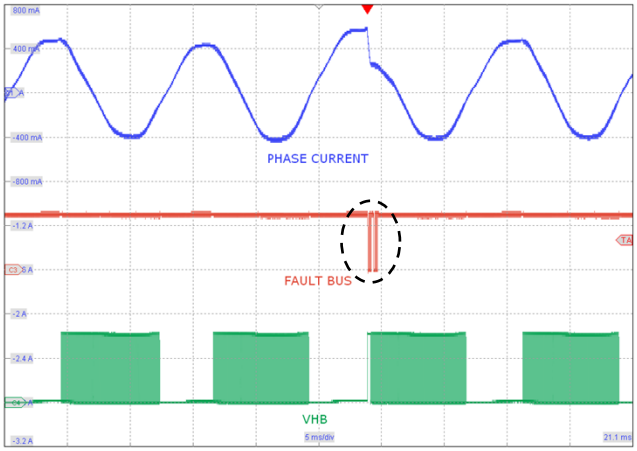

Figure 25 – Over-current - Motor Overload.
Peak Motor Current: 0.7 A R_{XL}: 44.2 kΩ.
Upper: $I_{PHASE\ W}$, 400 mA / div.
Middle: V_{FAULT}, 4 V / div.
Lower: V_{HB}, 200 V / div.
Time Scale: 5 ms / div.

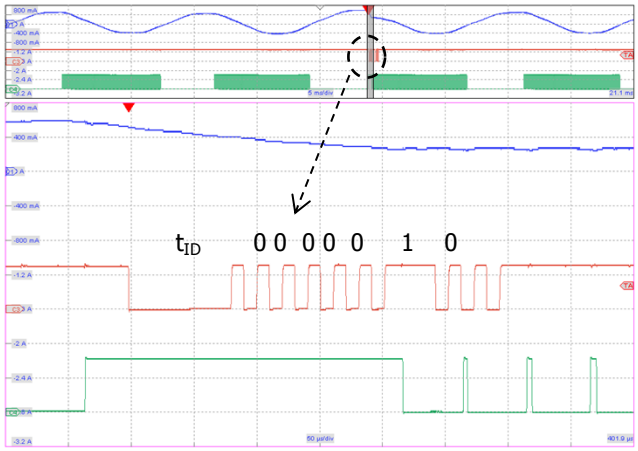

Figure 26 – LS FET Over-current Fault Status.
Status Update: 000 00 1 0 (LS OC)
Upper: $I_{PHASE\ W}$, 400 mA / div.
Middle: V_{FAULT}, 4 V / div.
Lower: V_{HB}, 200 V / div., 5 ms / div.
Zoom: 50 µs / div.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

Figure 27 and 28 depict the low-side FREDFET over-temperature warning (OTW) and shutdown (OTP) function and the associated status update reported on the FAULT bus. A localized external heat source applied to the device package forced the temperature rise.

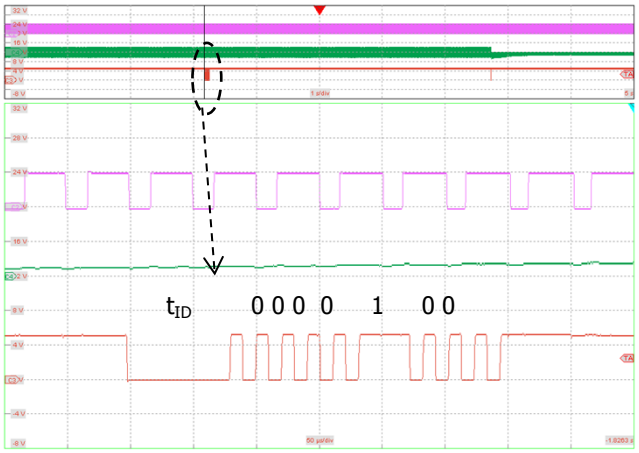

Figure 27 – Temperature Warning, Phase U.
Status Update: 000 01 0 0 (OTW).
Upper: INL Input, 5 V / div.
Middle: $I_{PHASE\ U}$, 500 mA / div.
Lower: V_{FAULT}, 4 V / div., 1 s / div.
Zoom: 50 μs / div.

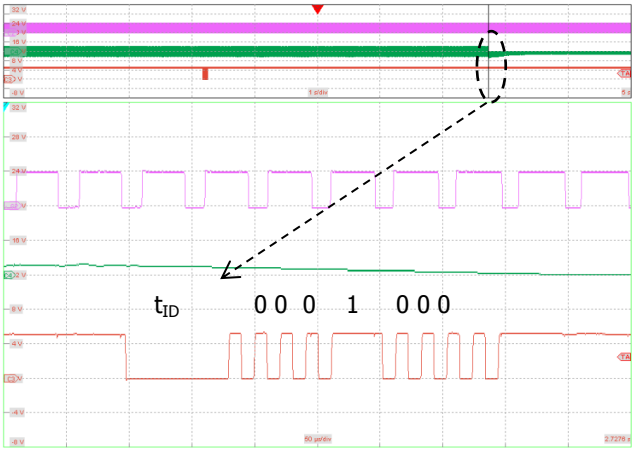

Figure 28 – Thermal Shutdown, Phase U.
Status Update: 000 10 0 0 (OTP).
Upper: INL Input, 5 V / div.
Middle: $I_{PHASE\ W}$, 500 mA / div.
Lower: V_{FAULT}, 4 V / div., 1 s / div.
Zoom: 50 μs / div.

7.6.2 System Level Monitoring

The test results shown in Figures 29 to 32 demonstrate the integrated HV bus UV monitoring function and status reporting through the status communication bus. Device U1 (Phase U) senses the DC input voltage. The input voltage slew rate for all bus monitoring tests is 5 V / ms.

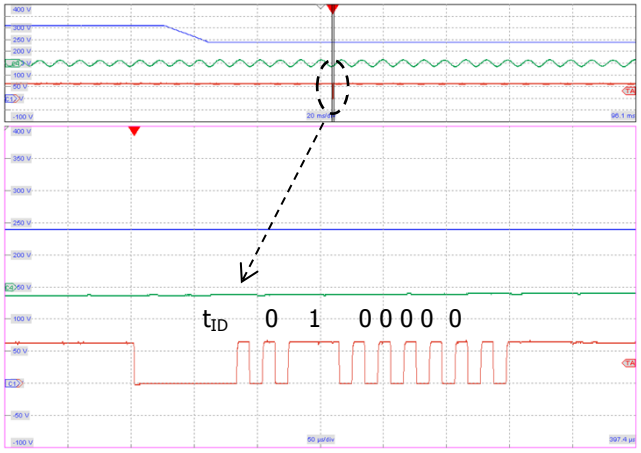

Figure 29 – Bus Sensing - Brown-out.
Bus Voltage Drop 340 to 240 VDC.
Status Update: 010 00 0 0 (UV100).
Upper: V_{BUS}, 50 V / div.
Middle: 1 A / div.
Lower: V_{FAULT}, 4 V / div., 20 ms / div.
Zoom: 50 µs / div.

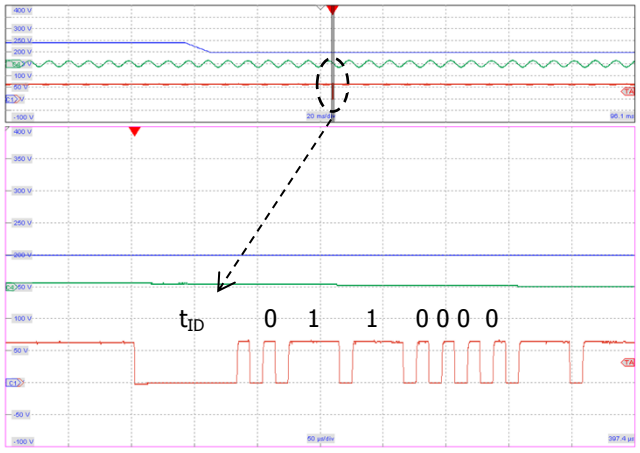

Figure 30 – Bus Sensing - Brown-out.
Bus Voltage Drop 240 to 200 VDC.
Status Update: 011 00 0 0 (UV85).
Upper: V_{BUS}, 50 V / div.
Middle: 1 A / div.
Lower: V_{FAULT}, 4 V / div., 20 ms / div.
Zoom: 50 µs / div.

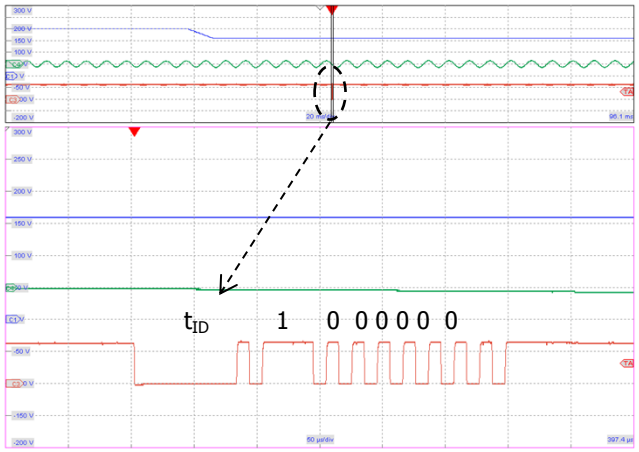

Figure 31 – Bus Sensing - Brown-out.
Bus Voltage Drop 200 to 160 VDC.
Status Update: 100 00 0 0 (UV70).
Upper: V_{BUS}, 100 V / div.
Middle: 1 A / div.
Lower: V_{FAULT}, 2 V / div., 20 ms / div.
Zoom: 50 µs / div.

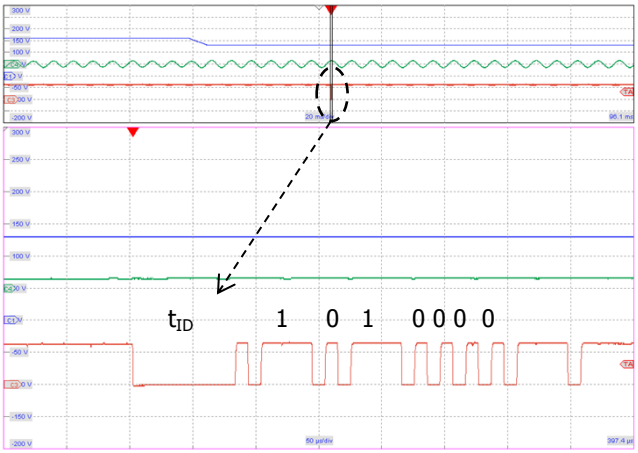

Figure 32 – Bus Sensing - Brown-out.
Bus Voltage Drop 160 to 130 VDC.
Status Update: 101 00 0 0 (UV55).
Upper: V_{BUS}, 50 V / div.
Middle: 1 A / div.
Lower: V_{FAULT}, 2 V / div., 20 ms / div.
Zoom: 50 µs / div.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

Figure 33 and Figure 34 illustrate the HV bus OV monitoring feature. Device U1 (Phase U) stops switching and reports the OV fault condition as soon as the bus voltage exceeds the set OV threshold (422 V with 7 MΩ). Switching resumes after the bus voltage level drops again below the detection threshold minus the hysteresis.

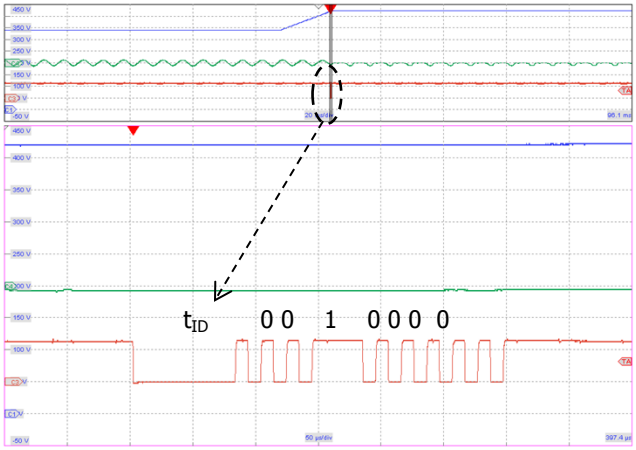

Figure 33 – Bus Sensing - OV Threshold Fault.
Bus Voltage Rise 340 to 430 VDC.
Status Update: 001 00 0 0 (OV).
Upper: V_{BUS}, 50 V / div.
Middle: $I_{PHASE\ U}$, 1 A / div.
Lower: V_{FAULT}, 4 / div., 20 ms / div.
Zoom: 50 μs / div.

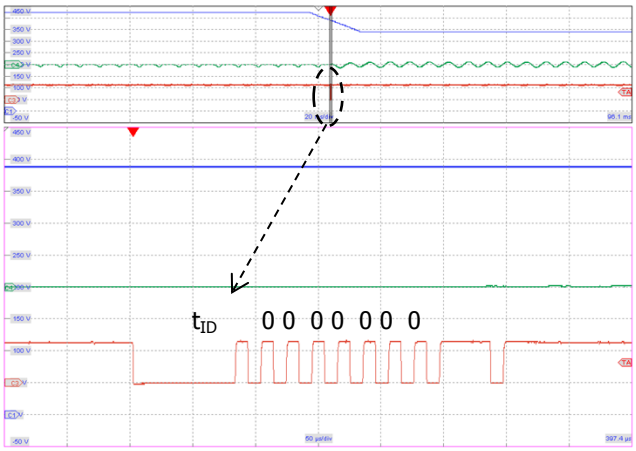

Figure 34 – Bus Sensing - OV Threshold Cleared.
Bus Voltage Drop 430 to 340 VDC.
Status Update: 000 00 0 0 (OV Cleared).
Upper: V_{BUS}, 50 V / div.
Middle: $I_{PHASE\ U}$, 1 mA / div.
Lower: V_{FAULT}, 4 / div., 20 ms / div.
Zoom: 50 μs / div.

Figure 35 and Figure 36 illustrate the system-level temperature monitoring function via the external system sense input, SM_W (pin 1 of connector J9). For this test, the system temperature is sensed though an external NTC thermistor connected to the pin. Figure 35 shows the status reporting when the system over-temperature threshold was reached while Figure 36 shows the status reporting when the over-temperature was removed.

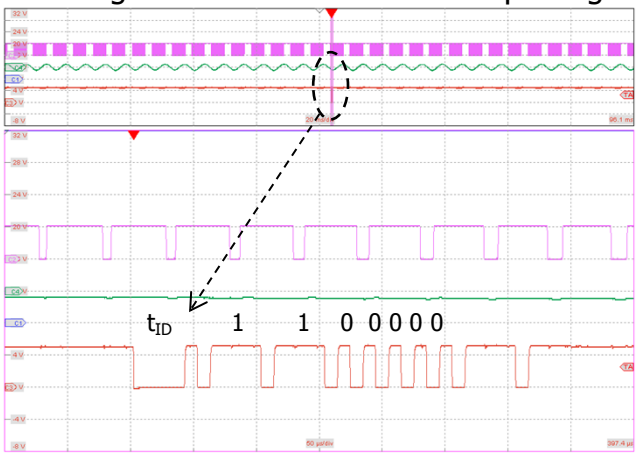

Figure 35 – External Temperature Fault Detected.
Status Update: 011 00 0 0 (System OT)
Upper: INL Input, 5 V / div.
Middle: $I_{PHASE\ W}$, 500 mA / div.
Lower: V_{FAULT}, 4 V / div., 20 ms / div.
Zoom: 50 µs / div.

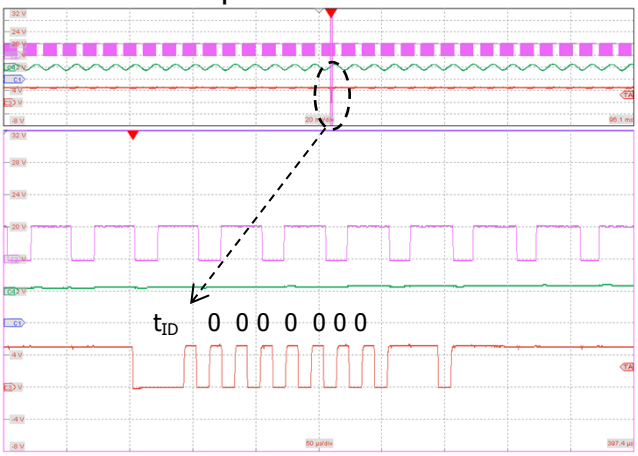

Figure 36 – External Temperature Fault Cleared.
Status Update: 000 00 0 0 (Fault Clear).
Upper: INL Input, 5 V / div.
Middle: $I_{PHASE\ W}$, 500 mA / div.
Lower: V_{FAULT}, 4 V / div., 20 ms / div.
Zoom: 50 µs / div.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

7.7 *Abnormal Motor Operation Tests*

This paragraph provides results during abnormal operation tests for appliances with motors as described in IEC 60335-1 (Safety of household and similar electrical appliances). The tests include:

- Operation under stalled motor conditions
- Operation with one motor winding disconnected
- Running overload test

The test results demonstrate the integrated protection features of the BridgeSwitch under such abnormal operations. The motor operates at 50 W and 1800 RPM at 310 Vdc rated voltage for all test cases except for the overload test.

7.7.1 Operation Under Stalled (Motor) Conditions

Figure 37 and Figure 38 depict the motor phase currents and overcurrent fault flag on Phase U when doing startup with a motor stalled condition. The inverter is continuously supplied for a period of 10 minutes at the rated voltage at this condition. The motor controller attempts an inverter re-start every 2 seconds with corresponding overcurrent faults. The FAULT bus reports them simultaneously. The motor is non-operational during the test with no device or motor damage during or after this test.

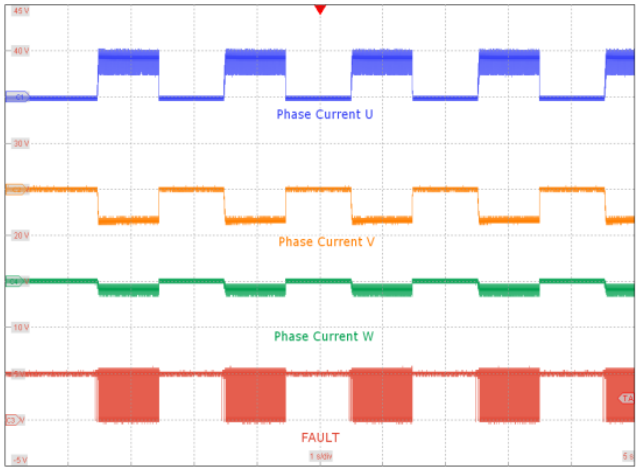

Figure 37 – Motor Stalled at Start-up Condition.
First: $I_{PHASE\ U}$, 700 mA / div.
Second: $I_{PHASE\ V}$, 700 mA / div.
Third: $I_{PHASE\ W}$, 700 mA / div.
Fourth: V_{FAULT}, 5 V / div., 1 s / div.

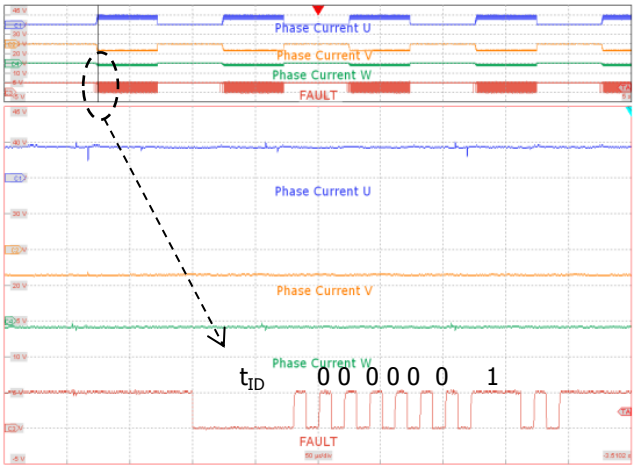

Figure 38 – Fault Flag: 000 00 0 1.
High-side Overcurrent, Phase U.
First: $I_{PHASE\ U}$, 700 mA / div.
Second: $I_{PHASE\ V}$, 700 mA / div.
Third: $I_{PHASE\ W}$, 700 mA / div.
Fourth: V_{FAULT}, 5 V / div., 1 s / div.
Zoom: 50 µs / div.

Figure 39 and 40 depict the motor phase currents and fault flags when the motor is stalled during running operation. The inverter is continuously supplied for a period of 10 minutes at the rated voltage at this condition. BridgeSwitch reports over-current fault conditions, and the motor is non-operational with no device or motor damage during the test or after the fault is removed.

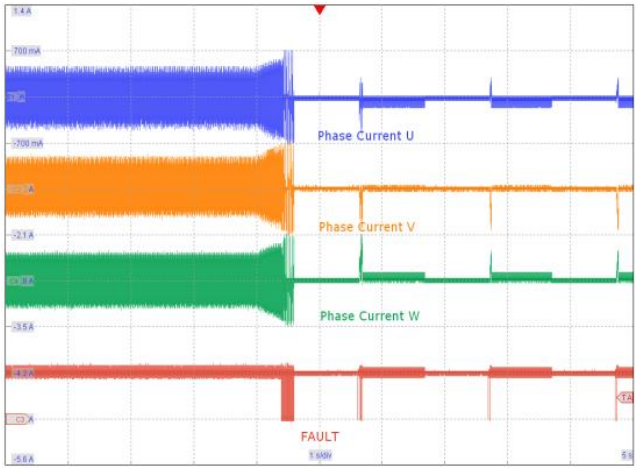

Figure 39 – Motor Stalled at Running Condition.
Multiple Overcurrent Flags Reported.
First: $I_{PHASE\ U}$, 700 mA / div.
Second: $I_{PHASE\ V}$, 700 mA / div.
Third: $I_{PHASE\ W}$, 700 mA / div.
Fourth: V_{FAULT}, 5 V / div., 1 s / div.

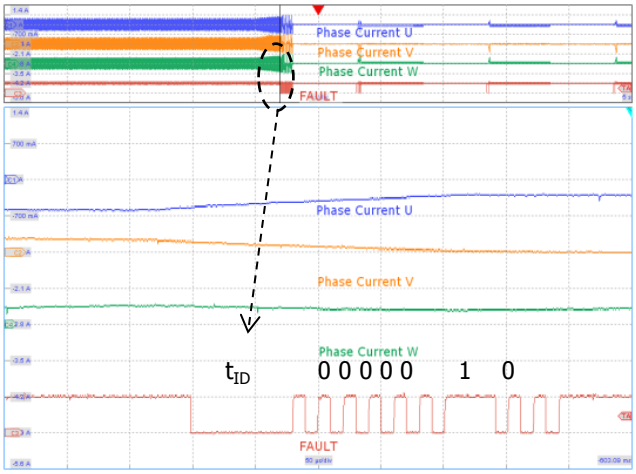

Figure 40 – First Fault Flag: 000 00 1 0.
Low-side overcurrent, Phase U.
First: $I_{PHASE\ U}$, 700 mA / div.
Second: $I_{PHASE\ V}$, 700 mA / div.
Third: $I_{PHASE\ W}$, 700 mA / div.
Fourth: V_{FAULT}, 5 V / div., 1 s / div.
Zoom: 50 µs / div.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

7.7.2 Operation with One Motor Winding Disconnected

Figure 41 and 42 depict the motor phase currents and fault flag during operation with one motor winding disconnected.

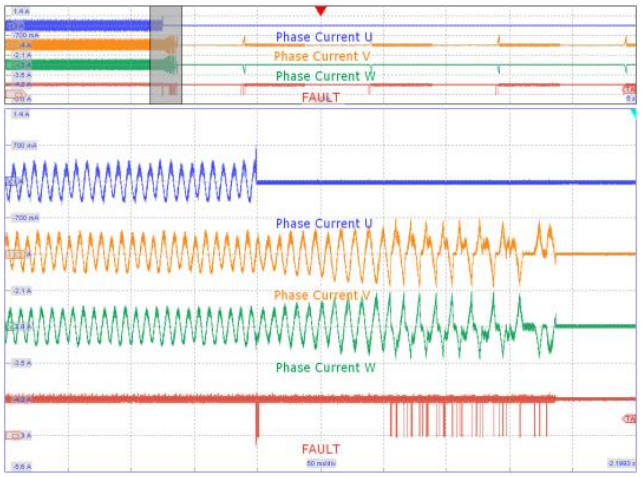

Figure 41 – Phase U Winding Disconnected.
First: $I_{PHASE\ U}$, 700 mA / div.
Second: $I_{PHASE\ V}$, 700 mA / div.
Third: $I_{PHASE\ W}$, 700 mA / div.
Fourth: V_{FAULT}, 5 V / div., 50 ms / div.

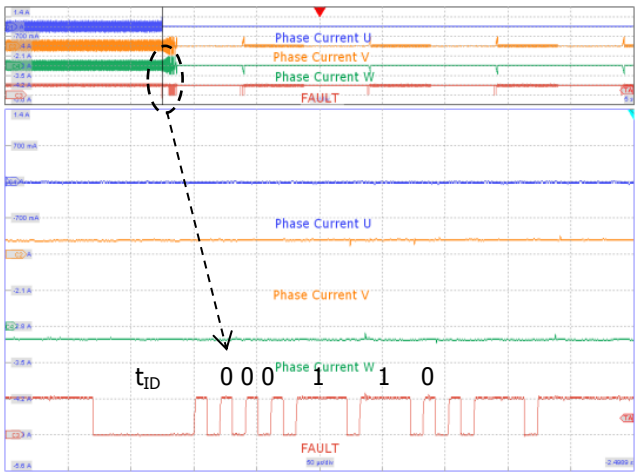

Figure 42 – Fault Flag: 000 11 0 0.
High-side Driver Not Ready, Phase U.
First: $I_{PHASE\ U}$, 700 mA / div.
Second: $I_{PHASE\ V}$, 700 mA / div.
Third: $I_{PHASE\ W}$, 700 mA / div.
Fourth: V_{FAULT}, 5 V / div., 1 s / div.
Zoom: 50 µs / div.

The device reports first a high-side driver not ready on Phase U device after the winding disconnection on Phase U and followed by multiple overcurrent status updates from the other two phases (device V and W) respectively . The motor operates abnormally before completely stalling with no device or motor damage.

Figure 43 and Figure 44 depicts the overcurrent status report on Phase V and Phase W device respectively following the Phase U winding disconnection.

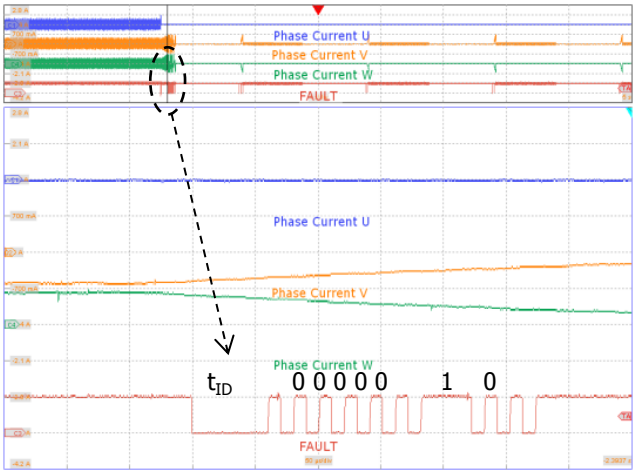

Figure 43 – Phase V Overcurrent Fault Flag.
Low-side Overcurrent, Phase V.
First: $I_{PHASE\ U}$, 700 mA / div.
Second: $I_{PHASE\ V}$, 700 mA / div.
Third: $I_{PHASE\ W}$, 700 mA / div.
Fourth: V_{FAULT}, 5 V / div., 1 s / div.
Zoom: 50 µs / div.

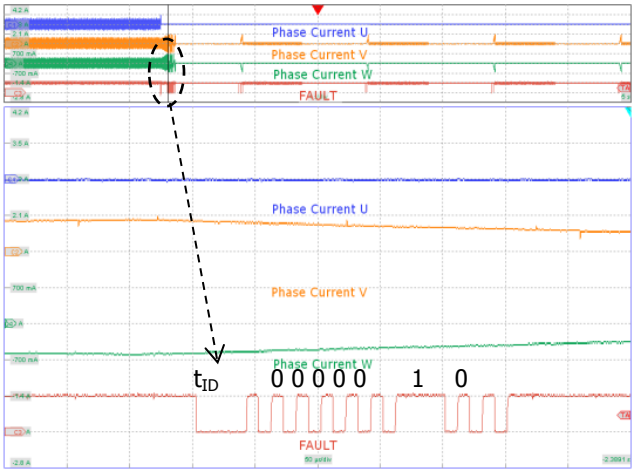

Figure 44 – Phase W Overcurrent Fault Flag.
Low-side Overcurrent, Phase W.
First: $I_{PHASE\ U}$, 700 mA / div.
Second: $I_{PHASE\ V}$, 700 mA / div.
Third: $I_{PHASE\ W}$, 700 mA / div.
Fourth: V_{FAULT}, 5 V / div., 1 s / div.
Zoom: 50 µs / div.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

7.7.3 Running Overload Test

Figure 45 and Figure 46 depict the motor phase currents and status update flag during a running overload fault condition. During this test, the motor load is increased such that the current through the motor windings increases by 10% and until steady conditions are established. The load is then increased again and the test repeats until the BridgeSwitch protection engages or the motor stalls.

With the motor stalled condition, the inverter is supplied continuously for a period of 10 minutes at the rated voltage. Every device reports status updates and the motor is non-operational with no device or motor damage.

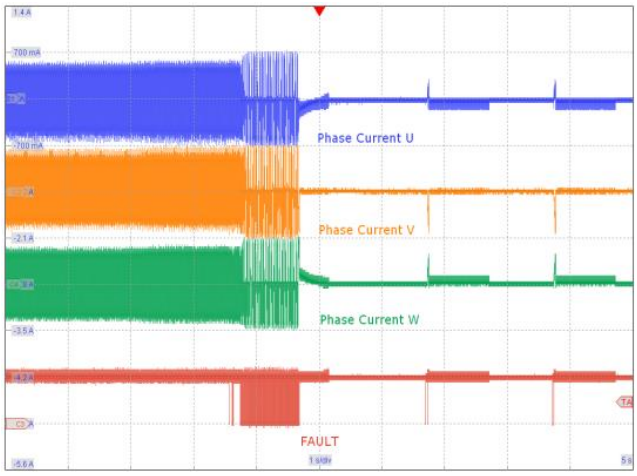

Figure 45 – Running Overload Test >120 W.
First: $I_{PHASE\ U}$, 700 mA / div.
Second: $I_{PHASE\ V}$, 700 mA / div.
Third: $I_{PHASE\ W}$, 700 mA / div.
Fourth: V_{FAULT}, 5 V / div., 1 s / div.

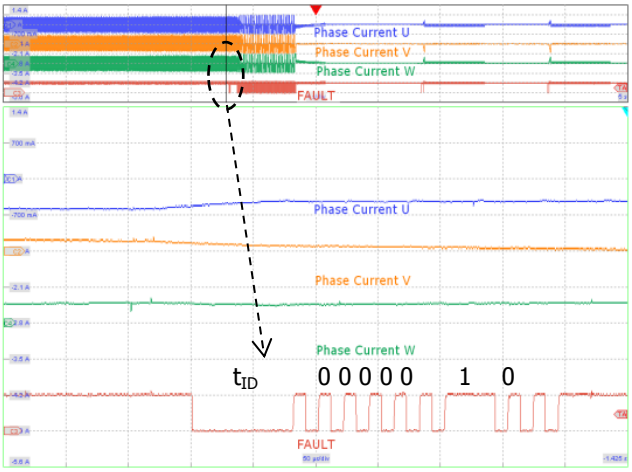

Figure 46 – First Fault Flag: 000 00 1 0.
Low-side Overcurrent, Phase U.
First: $I_{PHASE\ U}$, 700 mA / div.
Second: $I_{PHASE\ V}$, 700 mA / div.
Third: $I_{PHASE\ W}$, 700 mA / div.
Fourth: V_{FAULT}, 5 V / div., 1 s / div.
Zoom: 50 µs / div.

8 Appendix

8.1 *Inverter Circuit Board Manual*

Figure 47 shows locations and functions of all connectors to and from the inverter board.

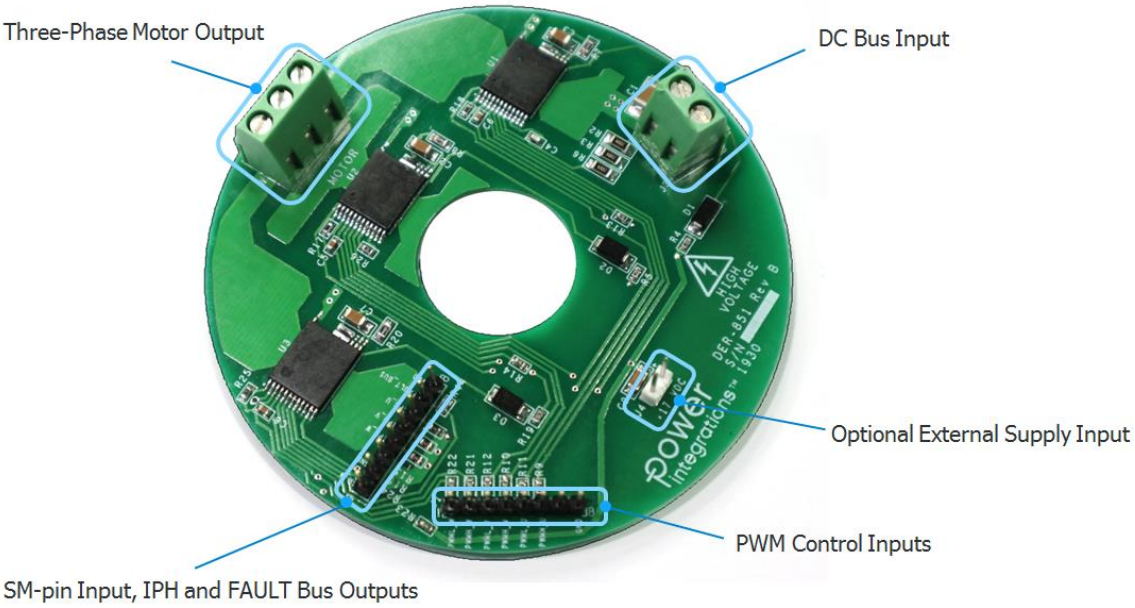

Figure 47 – RDK-851 Connections (Top View).

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

8.1.1 Inverter Connectors and Pin Assignments

The high-voltage DC bus connects to the inverter through a two a two-position terminal block, J3. The positive input should connect to the terminal besides the local decoupling capacitor C1.

The three-phase motor outputs connect to the inverter through a three-position terminal block, J5. Each terminal position is labeled U, V, and W, on the board, which identifies each phase output of device U1, U2, and U3 respectively.

The inverter board permits optional external supply operation from a single-rail +17 V DC supply. The external supply input connects to the inverter through a two-position header connector, J4. The positive input should connect to the terminal besides the "+" label on-board. Figure 48 depicts physical dimension of connector J4.

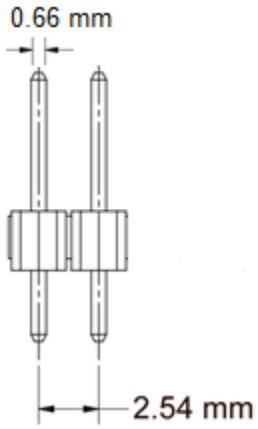

Figure 48 – External Supply Input Connector (J4).

Control input signals, SM-W pin input, instantaneous phase current and status communication bus signals connect to the test system through a two 8-position header breakaway connectors J1, and J9. Figure 49 depicts physical dimensions and pin numbers.

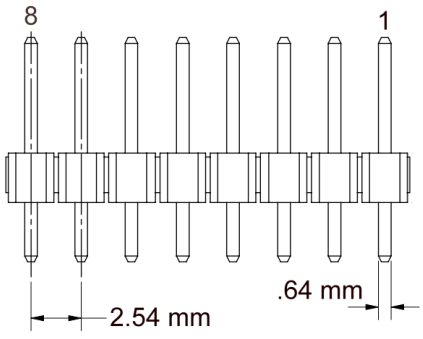

Figure 49 – Control Input and System Input / Output Signals (J1, J9).

Table 5 lists the input signals on the control input connector, J1.

Pin No.	Signal	Type	Comments
1	PWML_W	Input	Gate drive signal for low-side power FREDFET of Phase W (U3) device, active high, 3.3 V or 5 V CMOS compatible
2	PWMH_W	Input	Gate drive signal for high-side power FREDFET of Phase W (U3) device, active low, 3.3 V or 5 V CMOS compatible
3	PWML_V	Input	Gate drive signal for low-side power FREDFET of Phase V (U2) device, active high, 3.3 V or 5 V CMOS compatible
4	PWMH_V	Input	Gate drive signal for high-side power FREDFET of Phase V (U2) device, active low, 3.3 V or 5 V CMOS compatible
5	PWML_U	Input	Gate drive signal for low-side power FREDFET of Phase U (U1) device, active high, 3.3 V or 5 V CMOS compatible
6	PWMH_U	Input	Gate drive signal for high-side power FREDFET of Phase U (U1) device, active low, 3.3 V or 5 V CMOS compatible
7	GND	n/a	Reference for connector input and output signals and system microcontroller
8	GND	n/a	Reference for connector input and output signals and system microcontroller

Table 5 – Control Input Signals Pin Assignments

Table 6 lists all input and output signals on the system (inverter board) input/output signal connector, J9.

Pin No.	Signal	Type	Comments
1	SM_W	Input	External input for system sensing (i.e. can be connected to external thermistor for system temperature monitor via status communication bus)
2	GND	n/a	Reference for connector input and output signals and system microcontroller
3	GND	n/a	Reference for connector input and output signals and system microcontroller
4	IPH_W	Output	Voltage signal proportional to instantaneous phase low-side FREDFET Drain current of Phase W (U3), 1 V per 0.25 A Drain current signal ratio
5	IPH_V	Output	Voltage signal proportional to instantaneous phase low-side FREDFET Drain current of Phase V (U2), 1 V per 0.25 A Drain current signal ratio
6	IPH_U	Output	Voltage signal proportional to instantaneous phase low-side FREDFET Drain current of Phase U (U1), 1 V per 0.25 A Drain current signal ratio
7	FAULT_BUS	Input/Output	Single wire, bi-directional communication bus (open-Drain architecture)
8	VDD	Input	Pull-up supply for communication bus, 3.3 V ±5% or 5 V ±5% compatible

Table 6 – System Input / Output Signals Pin Assignment.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

8.2 *Status Word Encoding*

The 7-bit word followed by a parity bit encodes the status communication bus information. Table 7 summarizes encoding of various status updates the device may communicate to the system micro-controller. The status word consists of five blocks with status changes grouped together that cannot occur at the same time. This enables simultaneous reporting of multiple status updates to the system micro-controller without having to take care about fault priorities and a fault-reporting queue.

The last row (7-bit word “000 00 0 0”) encodes Device Ready status and is used to communicate a successful power-up sequence to the system, communicated when a certain fault is cleared and sent it to acknowledge a status request the system MCU in case no fault is present.

FAULT	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6
HV bus OV	0	0	1				
HV bus UV 100%	0	1	0				
HV bus UV 85%	0	1	1				
HV bus UV 70%	1	0	0				
HV bus UV 55%	1	0	1				
System thermal fault	1	1	0				
LS Driver not ready[1]	1	1	1				
LS FET thermal warning				0	1		
LS FET thermal shutdown				1	0		
HS Driver not ready[2]				1	1		
LS FET over-current						1	
HS FET over-current							1
Device Ready (no faults)	0	0	0	0	0	0	0

Notes:
1. Includes XL-pin open/short circuit fault, IPH pin to XL pin short circuit, and trim bit corruption
2. Includes HS-to-LS communication loss, V_{BPH} or internal 5 V rail out of range, and XH pin open/short-circuit fault

Table 7 – Status Word Encoding.

8.3 *Test Bench Set-up*

Figure 50 depicts the test bench used to gather the performance data presented in this report. It consists of:

- RD-851 Inverter Board using BridgeSwitch BRD1260C IC
- 310 VDC, 8 poles BLDC motor (Foshan Lepuda PLD-39-8-1)
- Sinusoidal motor controller (PT2505 IC- sine wave drive hall sensor based IC)- mounted on the motor with hall sensors
- Electro-mechanics hysteresis brake (HB-103)
- Motor brake controller (ICS-2000)
- Programmable high-voltage power source (Keysight 6313B)
- DC power supply (Topward 6303A)
- Three-Phase Power Analyzer (WT1806E)
- Oscilloscope (Rohde & Schwarz RTO-2004 4-channel 600 MHz oscilloscope with Bandwidth set to 1 MHz)

Figure 50 – Test Bench Set-up.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

8.4 *Inverter Output Power Measurement*

3-phase inverter output power P_{OUT} and efficiency measurements apply the "two wattmeter" method illustrated in Figure 51 below.

$$P_{OUT} = P_{CH1} + P_{CH2}$$

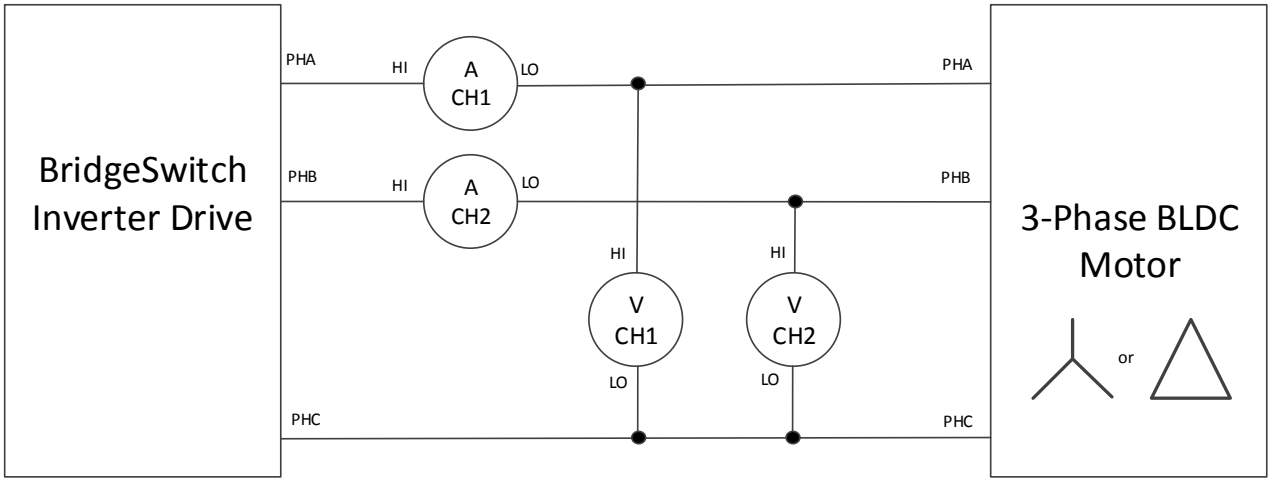

Figure 51 – Inverter Output Power Measurement.

8.5 *Current Capability vs. Ambient Temperature*

The figure below depicts the continuous RMS current capability of the RDK-851 example design running sinusoidal control at 20 kHz operation at 310 V DC bus voltage. The plots show two derating curves with three BRD1260C devices operating either self-supplied or externally supplied at the respective BPL- and BPH-pins. Each curve details the available continuous RMS current at different board ambient temperatures with a package temperature of 100 °C (average of all three devices).

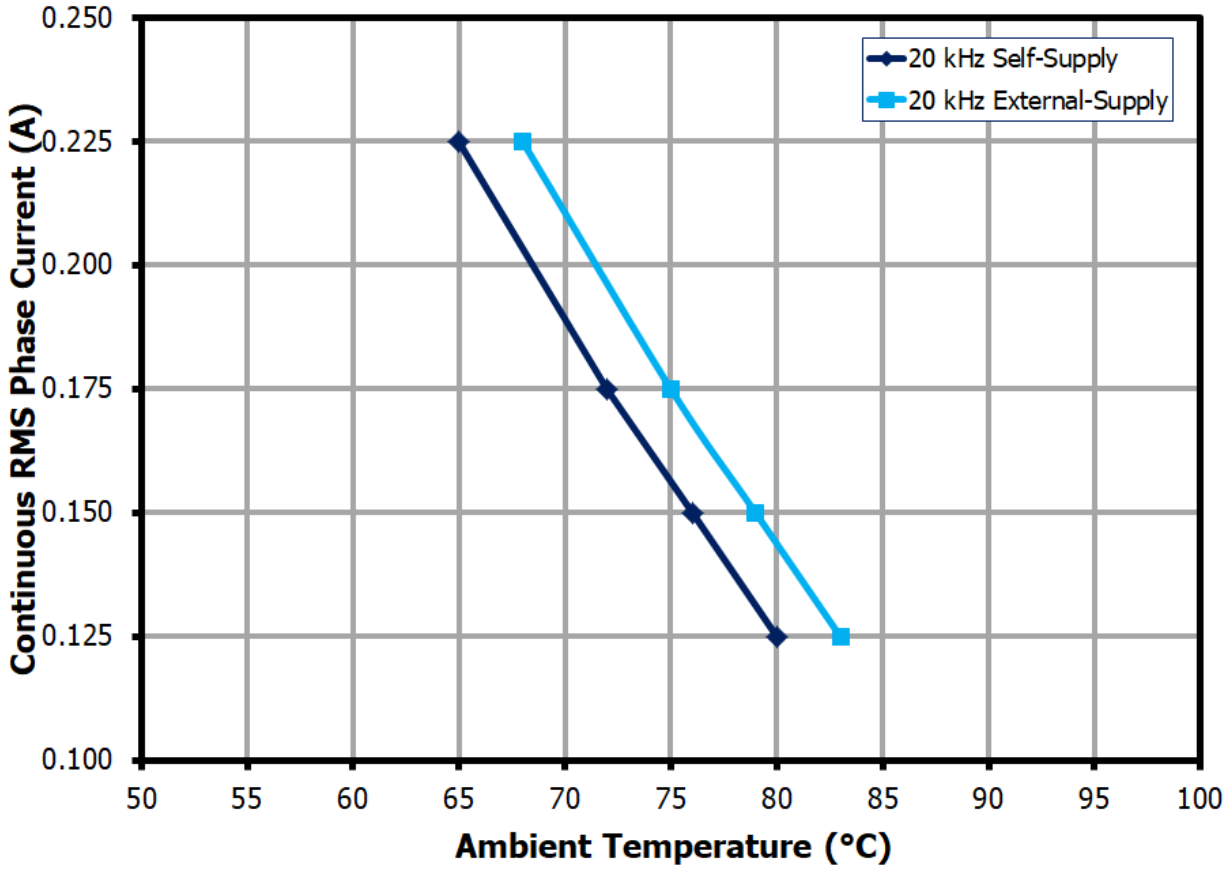

Figure 52 – Current Capability vs. Ambient Temperature (Max. 100 °C Package Temperature).

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

9 Revision History

Date	Author	Revision	Description & Changes	Reviewed
02-Feb-20	JHP	1.0	Initial Release.	Apps and Mktg

For the latest updates, visit our website: www.power.com

Reference Designs are technical proposals concerning how to use Power Integrations' gate drivers in particular applications and/or with certain power modules. These proposals are "as is" and are not subject to any qualification process. The suitability, implementation and qualification are the sole responsibility of the end user. The statements, technical information and recommendations contained herein are believed to be accurate as of the date hereof. All parameters, numbers, values and other technical data included in the technical information were calculated and determined to our best knowledge in accordance with the relevant technical norms (if any). They may base on assumptions or operational conditions that do not necessarily apply in general. We exclude any representation or warranty, express or implied, in relation to the accuracy or completeness of the statements, technical information and recommendations contained herein. No responsibility is accepted for the accuracy or sufficiency of any of the statements, technical information, recommendations or opinions communicated and any liability for any direct, indirect or consequential loss or damage suffered by any person arising therefrom is expressly disclaimed.

Power Integrations reserves the right to make changes to its products at any time to improve reliability or manufacturability. Power Integrations does not assume any liability arising from the use of any device or circuit described herein. POWER INTEGRATIONS MAKES NO WARRANTY HEREIN AND SPECIFICALLY DISCLAIMS ALL WARRANTIES INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF THIRD PARTY RIGHTS.

Patent Information
The products and applications illustrated herein (including transformer construction and circuits' external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at http://www.power.com/ip.htm.

Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Worldwide: +1-65-635-64480
Americas: +1-408-414-9621
e-mail: usasales@power.com

CHINA (SHANGHAI)
Rm 2410, Charity Plaza, No. 88,
North Caoxi Road,
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasales@power.com

CHINA (SHENZHEN)
17/F, Hivac Building, No. 2, Keji
Nan 8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
e-mail: chinasales@power.com

GERMANY (AC-DC/LED Sales)
Einsteinring 24
85609 Dornach/Aschheim
Germany
Tel: +49-89-5527-39100
e-mail: eurosales@power.com

GERMANY (Gate Driver Sales)
HellwegForum 1
59469 Ense
Germany
Tel: +49-2938-64-39990
e-mail: igbt-driver.sales@
power.com

INDIA
#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
e-mail: indiasales@power.com

ITALY
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI) Italy
Phone: +39-024-550-8701
e-mail: eurosales@power.com

JAPAN
Yusen Shin-Yokohama 1-chome Bldg.
1-7-9, Shin-Yokohama, Kohoku-ku
Yokohama-shi,
Kanagawa 222-0033 Japan
Phone: +81-45-471-1021
e-mail: japansales@power.com

KOREA
RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

SINGAPORE
51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
e-mail: singaporesales@power.com

TAIWAN
5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
e-mail: taiwansales@power.com

UK
Building 5, Suite 21
The Westbrook Centre
Milton Road
Cambridge
CB4 1YG
Phone: +44 (0) 7823-557484
e-mail: eurosales@power.com