

Title	<i>Reference Design Report for a 65 W USB PD 3.0 Power Supply with 3.3 V – 21 V / 3 A PPS Output Using InnoSwitch™ 4-Pro PowiGaN™ INN4373F-H341, ClampZero™ CPZ1075M and Injoinic IP2726S Controller</i>
Specification	90 VAC – 265 VAC Input; 5 V / 3 A, 9 V / 3 A, 12 V / 3 A, 15 V / 3 A, 20 V / 3.25 A, or 3.3 V – 21 V / 3 A PPS Output
Application	USB PD / PPS Power Adapter
Author	Applications Engineering Department
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Summary and Features

- InnoSwitch4-Pro: Digitally Controllable Off-line CV/CC ZVS Flyback Integrated Switcher IC with 750V PowiGaN, Active Clamp Drive and Synchronous Rectification
 - Comprehensive protection features with telemetry for power supply status and fault monitoring
- Meets DOE6 and CoC v5 2016 Average Efficiency requirements with at least 3.0% pass margin
 - 5 V Output: 91.35% at 115 VAC (9.52% margin); 90.18% at 230 VAC (8.34% margin)
 - 9 V Output: 92.18% at 115 VAC (4.88% margin); 92.17% at 230 VAC (4.88% margin)
 - 12 V Output: 92.29% at 115 VAC (3.99% margin); 92.71% at 230 VAC (4.41% margin)
 - 15 V Output: 92.32% at 115 VAC (3.47% margin); 93.07% at 230 VAC (4.22% margin)
 - 20 V Output: 92.37% at 115 VAC (3.37% margin); 93.43% at 230 VAC (4.43% margin)
- Meets CoC v5 2016 10% Load Efficiency requirements with high margin (>7.01%) for all PDOs
- <25 mW no-load input power at 230 VAC
- Meets CISPR22 / EN55022 Class B conducted EMI with high margin
 - >6dB margin at worst case condition (15 V / 3 A, 230 VAC)
- High power density: 15.2 W / inch³ without enclosure (2.44" x 2.1" x 0.83" form factor)
- Low component count: 78 total

Power Integrations

5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

PATENT INFORMATION

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Table of Contents

1	Introduction	7
2	Power Supply Specification	9
3	Schematic.....	11
4	Circuit Description	12
4.1	Input Rectifier and EMI Filter.....	12
4.2	InnoSwitch4-Pro IC Primary	12
4.3	InnoSwitch4-Pro IC Secondary	13
4.4	USB Type-C and PD Interface.....	14
5	PCB Layout	16
6	Bill of Materials	17
6.1	Electrical Parts.....	17
6.2	Mechanical Parts.....	18
7	Common Mode Choke Specifications (L1).....	19
7.1	Electrical Diagram.....	19
7.2	Electrical Specifications	19
7.3	Material List	19
7.4	Winding Instructions	19
8	Transformer Specification (T1).....	20
8.1	Electrical Diagram.....	20
8.2	Electrical Specifications	20
8.3	Transformer Build Diagram	21
8.4	Material List	21
8.5	Winding Instructions.....	22
9	Transformer Design Spreadsheet	31
10	Performance Data	35
10.1	No-Load Input Power.....	35
10.2	Full Load Efficiency (On-board).....	36
10.3	Average and 10% Load Efficiency.....	36
10.3.1	Efficiency Requirements	36
10.3.2	Efficiency Performance Summary (On Board).....	36
10.3.3	Average and 10% Load Efficiency Measurements.....	37
10.3.3.1	Output: 5 V / 3.0 A.....	37
10.3.3.2	Output: 9 V / 3.0 A.....	37
10.3.3.3	Output: 12 V / 3.0 A.....	38
10.3.3.4	Output: 15 V / 3.0 A.....	38
10.3.3.5	Output: 20 V / 3.25 A	39
10.4	Efficiency Across Line at 100% Load (On Board)	40
10.5	Efficiency Across Load (On Board)	41
10.5.1	Output: 5 V / 3.0 A	41
10.5.2	Output: 9 V / 3.0 A	42
10.5.3	Output: 12 V / 3.0 A	43
10.5.4	Output: 15 V / 3.0 A	44
10.5.5	Output: 20 V / 3.25 A.....	45



10.6	Load Regulation (On Board)	46
10.6.1	Output: 5 V / 3.0 A	46
10.6.2	Output: 9 V / 3.0 A	47
10.6.3	Output: 12 V / 3.0 A	48
10.6.4	Output: 15 V / 3.0 A	49
10.6.5	Output: 20 V / 3.25 A.....	50
10.7	Line Regulation (On Board)	51
10.7.1	Output: 5 V / 3.0 A	51
10.7.2	Output: 9 V / 3.0 A	52
10.7.3	Output: 12 V / 3.0 A	53
10.7.4	Output: 15 V / 3.0 A	54
10.7.5	Output: 20 V / 3.25 A.....	55
11	Thermal Performance.....	56
11.1	Thermal Performance in Open Case, Room Temperature	56
11.1.1	Output: 20 V / 3.25 A (90 VAC)	56
11.1.2	Output: 20 V / 3.25 A (265 VAC).....	57
12	Waveforms.....	58
12.1	Start-up Waveforms.....	58
12.1.1	Input Voltage, Output Voltage and Current.....	58
12.1.2	Primary Drain Voltage and Current.....	59
12.1.3	SR FET Drain Voltage and Gate Voltage.....	59
12.2	Primary Drain Voltage and Current (Steady-State)	60
12.2.1	Output: 5 V / 3 A	60
12.2.2	Output: 9 V / 3 A	60
12.2.3	Output: 12 V / 3 A	61
12.2.4	Output: 15 V / 3 A	61
12.2.5	Output: 20 V / 3.25 A.....	62
12.3	SR FET Drain Voltage (Steady-State)	63
12.3.1	Output: 5 V / 3 A	63
12.3.2	Output: 9 V / 3 A.....	63
12.3.3	Output: 12 V / 3 A	64
12.3.4	Output: 15 V / 3 A	64
12.3.5	Output: 20 V / 3.25 A.....	65
12.4	Primary and SR FET Drain Voltage and Current (during Output Voltage Transition)	66
12.4.1	Primary Drain Voltage and Current, 3.3 V to 21 V PPS Transition	66
12.4.2	SR FET Drain Voltage, 3.3 V to 21 V Transition	67
12.4.3	SR FET Drain Voltage, Downward Vout Transition	67
12.5	Load Transient Response	68
12.5.1	Output: 5 V / 3 A.....	68
12.5.2	Output: 9 V / 3 A	68
12.5.3	Output: 12 V / 3 A	69
12.5.4	Output: 15 V / 3 A	69
12.5.5	Output: 20 V / 3.25 A.....	70



12.6	Output Ripple Measurements.....	71
12.6.1	Ripple Measurement Technique	71
12.6.2	Output Voltage Ripple Waveforms.....	72
12.6.2.1	Output: 5 V / 3 A	72
12.6.2.2	Output: 9 V / 3 A	72
12.6.2.3	Output: 12 V / 3 A.....	73
12.6.2.4	Output: 15 V / 3 A.....	73
12.6.2.5	Output: 20 V / 3.25 A.....	74
12.6.3	Output Voltage Ripple Amplitude vs. Load	75
12.6.3.1	Output: 5 V / 3 A	75
12.6.3.2	Output: 9 V / 3 A	76
12.6.3.3	Output: 12 V / 3 A.....	77
12.6.3.4	Output: 15 V / 3 A.....	78
12.6.3.5	Output: 20 V / 3.25 A	79
13	CV/CC Profile	80
13.1	Output: 21 V / 3 A PPS Request, PDO6	80
14	Voltage Step and Current Limit Test using QuadraMAX and Total Phase Analyzer	81
14.1	Voltage Step Test (VST).....	81
14.2	Current Limit Test (CLT)	82
15	Conducted EMI	83
15.1	Floating Ground (QPK / AV).....	83
15.1.1	Output: 5 V / 3 A	83
15.1.2	Output: 9 V / 3 A	84
15.1.3	Output: 12 V / 3 A	85
15.1.4	Output: 15 V / 3 A	86
15.1.5	Output: 20 V / 3.25 A.....	87
16	Surge	88
16.1	Differential Mode Surge (L1 to L2), 230 VAC Input	88
16.2	Common Mode Surge (L1, L2 to PE), 230 VAC Input.....	88
16.3	Common Mode Surge (L1 to PE), 230 VAC Input	88
16.4	Common Mode Surge (L2 to PE), 230 VAC Input	89
17	Electrostatic Discharge	90
17.1	VOUT and GND ESD Performance.....	90
17.1.1	Air Discharge, End of Cable, 230 VAC Input.....	91
17.1.2	Air Discharge, On-board, 230 VAC Input.....	92
17.1.3	Contact Discharge, End of Cable, 230 VAC Input.....	93
17.1.4	Contact Discharge, On the Board, 230 VAC Input.....	93
17.2	CC1 and CC2 ESD Performance	94
17.2.1	Air Discharge, On the board, 230 VAC Input	95
17.2.2	Air Discharge, End of cable, 230 VAC Input	96
17.2.3	Contact Discharge, On the board, 230 VAC Input.....	97
17.2.4	Contact Discharge, End of Cable, 230 VAC Input.....	97
18	Revision History	98



Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.



1 Introduction

This engineering report describes a 65 W USB PD 3.0 power supply using InnoSwitch4-Pro INN4373F-H341 and ClampZero CPZ1075M. The USB PD controller is an Injoinic IP2726S, and the USB PD source capabilities of the power supply are listed below.

- PDO1: 5 V / 3 A (Fixed Supply)
- PDO2: 9 V / 3 A (Fixed Supply)
- PDO3: 12 V / 3 A (Fixed Supply)
- PDO4: 15 V / 3 A (Fixed Supply)
- PDO5: 20 V / 3.25 A (Fixed Supply)
- PDO6: 3.3 V – 21 V / 3 A (Programmable Power Supply)

This design shows the high power density and efficiency that is possible due to the high level of integration of the InnoSwitch4-Pro active clamp flyback controller providing exceptional performance.

The report contains the power supply specification, schematic diagram, printed circuit board layout, bill of materials, magnetics specifications, and performance data.

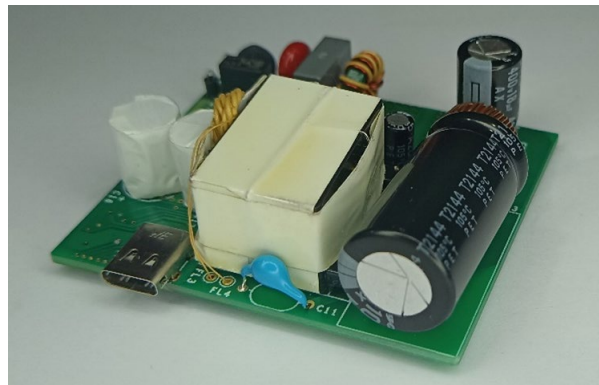


Figure 1 – Populated Circuit Board Photograph, Entire Assembly.

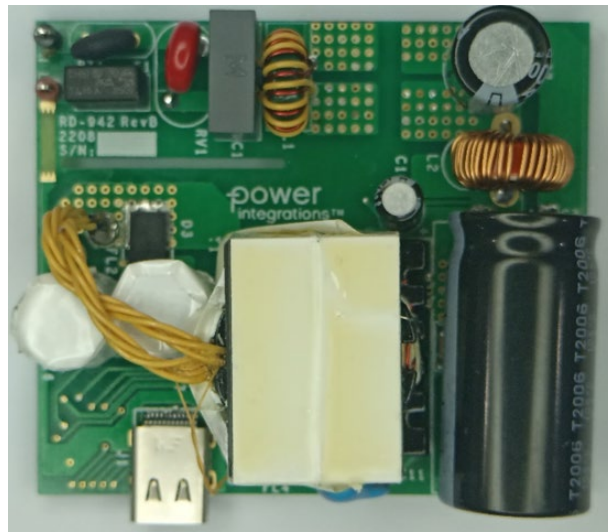
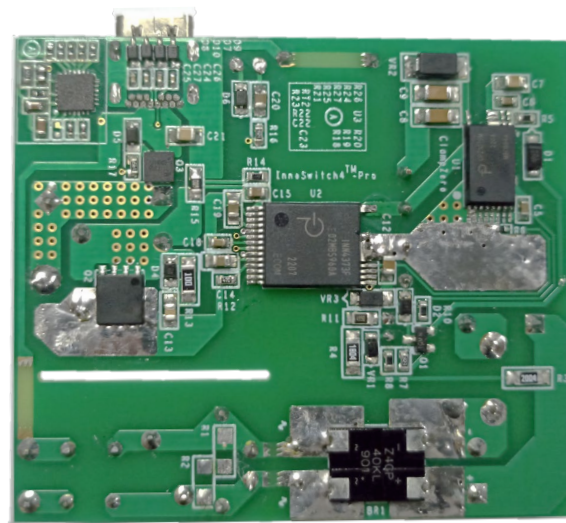


Figure 2 – Populated Circuit Board Photograph - Top.

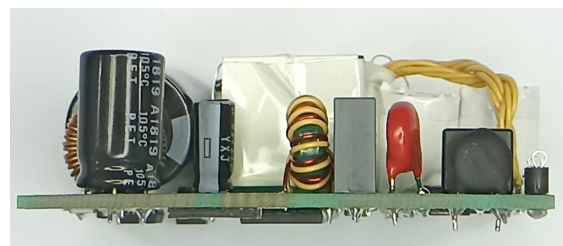


Board length: 2.44 inch



Board width:
2.1 inch

Figure 3 – Populated Circuit Board Photograph - Bottom.



Assembly height:
0.83 inch

Figure 4 – Populated Circuit Board Photograph - Side.



2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Input Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Input Frequency	f_{LINE}	47	50/60	63	Hz	
No-load Input Power				25	mW	Measured at 230 VAC
USB PD 3.0 Output: Fixed Supply PDOs						
5 V / 3 A Fixed Supply PDO1						
Output Voltage	$V_{OUT(5V)}$		5.0		V	See Note A.
Output Voltage Ripple	$V_{RIPPLE(5V)}$			125	mV	Measured at End of 100 mΩ Cable. See Note B.
Output Current	$I_{OUT(5V)}$			3.0	A	See Note C.
Average Efficiency	$\eta(5V)$	90.9			%	Average Efficiency at 115 VAC with V_{OUT} measured on the Board.
Continuous Output Power	$P_{OUT(5V)}$			15	W	
9 V / 3 A Fixed Supply PDO2						
Output Voltage	$V_{OUT(9V)}$		9.0		V	See Note A.
Output Voltage Ripple	$V_{RIPPLE(9V)}$			125	mV	Measured at End of 100 mΩ Cable. See Note B.
Output Current	$I_{OUT(9V)}$			3.0	A	See Note C.
Average Efficiency	$\eta(9V)$	91.7			%	Average Efficiency at 115 VAC with V_{OUT} measured on the Board.
Continuous Output Power	$P_{OUT(9V)}$			27	W	
12 V / 3 A Fixed Supply PDO3						
Output Voltage	$V_{OUT(12V)}$		12.0		V	See Note A.
Output Voltage Ripple	$V_{RIPPLE(12V)}$			125	mV	Measured at End of 100 mΩ Cable. See Note B.
Output Current	$I_{OUT(12V)}$			3.0	A	See Note C.
Average Efficiency	$\eta(12V)$	91.8			%	Average Efficiency at 115 VAC with V_{OUT} measured on the Board.
Continuous Output Power	$P_{OUT(12V)}$			36	W	
15 V / 3 A Fixed Supply PDO4						
Output Voltage	$V_{OUT(15V)}$		15.0		V	See Note A.
Output Voltage Ripple	$V_{RIPPLE(15V)}$			125	mV	Measured at End of 100 mΩ Cable. See Note B.
Output Current	$I_{OUT(15V)}$			3.0	A	See Note C.
Average Efficiency	$\eta(15V)$	91.8			%	Average Efficiency at 115 VAC with V_{OUT} measured on the Board.
Continuous Output Power	$P_{OUT(15V)}$			45	W	



20 V / 3.25 A Fixed Supply PDO5						
Output Voltage	$V_{OUT(20V)}$		20.0		V	See Note A.
Output Voltage Ripple	$V_{RIPPLE(20V)}$			125	mV	Measured at End of 100 mΩ Cable. See Note B.
Output Current	$I_{OUT(20V)}$			3.25	A	See Note C.
Average Efficiency	$\eta(20V)$	91.9			%	Average Efficiency at 115 VAC with VOUT measured on the Board.
Continuous Output Power	$P_{OUT(20V)}$			65	W	

Description	Symbol	Min	Typ	Max	Units	Comment
USB PD 3.0 Output: Programmable Power Supply APDOs						
3.3 V – 21 V / 3 A PPS APDO6						
Programmable Output Voltage Range	$V_{OUT(PDO6)}$	3.3		21	V	APDO Minimum and Maximum Voltage. See Note A.
Programmable Output Current Limit Range	$I_{OUT(PDO6)}$	1.0		3.0	A	See Note D.
PPS Voltage Step	$V_{STEP(PDO6)}$		20		mV	PPS Voltage Step (USB PD 3.0).
PPS Current Step	$I_{STEP(PDO6)}$		50		mA	PPS Current Step (USB PD 3.0).
Continuous Output Power	$P_{OUT(PDO6)}$			63	W	
Conducted EMI Margin		6			dB	Meets CISPR22B / EN55022B
Ambient Temperature	T_{AMB}	0		45	°C	Open Frame, Sea Level.

Note A: Output Voltage Regulation compliant with USB PD 3.0 Specifications.

B: Output Voltage Ripple measured at the end of 100 mΩ cable with the probe having decoupling capacitors 47 μF electrolytic and 100 nF ceramic in parallel.

C: Maximum Operating Current for the Fixed Supply PDO. Output Over Current Protection Threshold nominally set at 250 mA above the Operating Current requested by the USB PD Sink.

D: Output Current Limit Accuracy is within ±150 mA for Operating Current between 1 A and 3 A, or ±5% for Operating Current > 3 A; compliant with USB PD 3.0 Specifications.

Note: To use this design for a charger/adaptor with a different shape and form factor, the changes in the circuit board layout must be carefully evaluated to meet the target specifications for EMI, ESD, and Line Surge performance.



3 Schematic

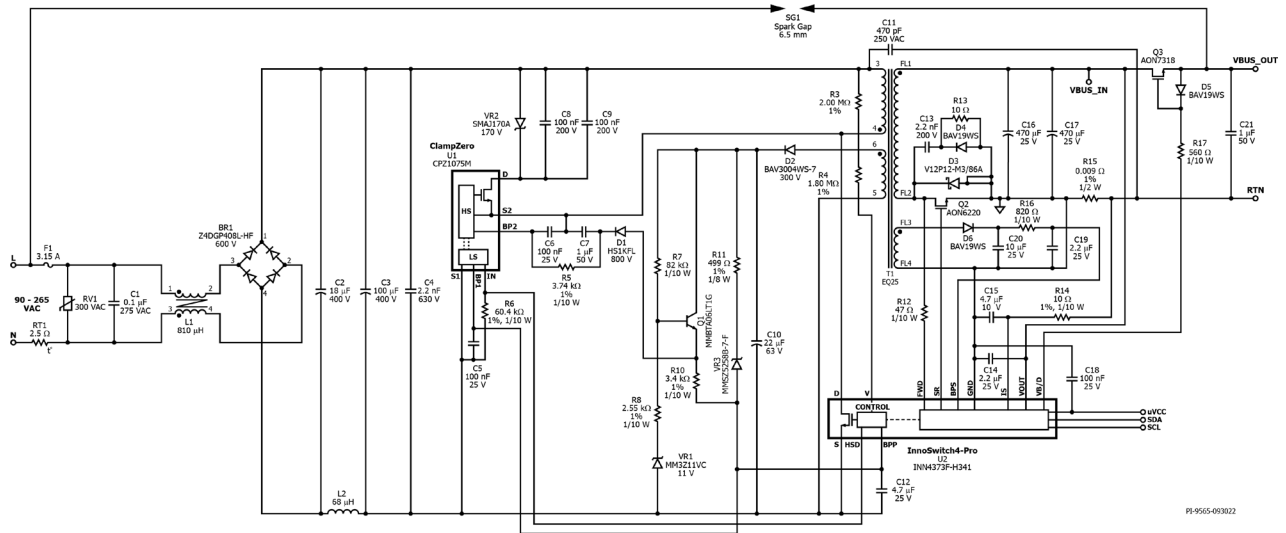


Figure 5 – DER-942 Schematic – Power Section.

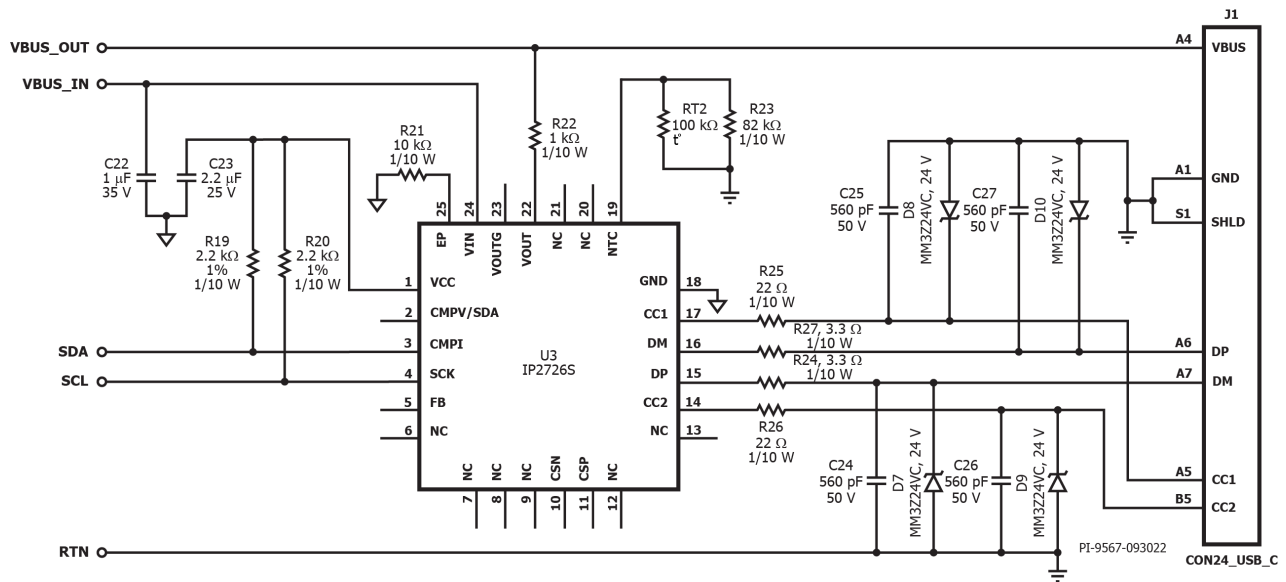


Figure 6 – DER-942 Schematic - USB PD Interface.

4 Circuit Description

4.1 *Input Rectifier and EMI Filter*

The input fuse F1 isolates the circuit and provides protection from component failure. Metal oxide varistor RV1 offers protection during line surge events by effectively clamping the input voltage seen by the power supply. Inrush thermistor RT1 limits the inrush current when the power supply is connected to the AC input. Common mode choke L1 along with Y-capacitor C11 provides common mode noise filtering while inductor L2 forms a pi filter with capacitors C2 and C3 for differential mode EMI filtering along with C1. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter capacitors C2 and C3.

4.2 *InnoSwitch4-Pro IC Primary*

One end of the transformer primary is connected to the rectified DC bus; the other is connected to the drain terminal of the switch inside the InnoSwitch4-Pro IC (U2). Resistors R3 and R4 provide input voltage sensing for protection in case of AC input undervoltage or overvoltage.

The primary clamp formed by the body diode of the ClampZero IC and capacitors C8 and C9 limits the peak drain voltage of U2 at the instant of turn-off of the switch inside U2. The energy stored in the leakage inductance of the transformer will be transferred to capacitors C8 and C9. Part of the magnetizing energy will also get transferred to C8 and C9 depending on the capacitance value used. VR2 is used to protect the InnoSwitch4-Pro from excessive drain voltages during abnormal conditions applied to the power supply. High voltage ceramic capacitor C4 is used to decouple the bulk voltage, reducing the loop area of high frequency switching currents.

When the FluxLink signal is received from the secondary-side, the InnoSwitch4-Pro IC generates an HSD (High Side Drive) signal to turn on the ClampZero device. When the ClampZero IC (U1) turns on, to achieve soft switching of the InnoSwitch4-Pro primary switch, clamp capacitors C8 and C9 start to charge the leakage inductance of the transformer in the case of CCM operation and both the leakage and the magnetizing inductance of the transformer in the case of DCM operation. A small delay is provided from the instant the high-side switch turns off to achieve zero voltage switching on the primary switch. This delay is either programmable by resistor R6 value at low-line input voltage, or a fixed 500 ns delay at high-line input voltage. The transition between programmable delay and fixed delay is based on input line voltage information at the V pin of InnoSwitch4-Pro IC.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor C12 when AC is first applied. During normal operation, the primary side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C10. Linear regulator circuit

comprises of BJT Q1, R7, R8, and Zener diode VR1 ensures sufficient current flows through R10 into the BPP pin of the InnoSwitch4-Pro and the BP1 pin of the ClampZero ICs. By injecting sufficient current into BPP and BP1 pins, the internal current source of U2 is not required to charge C12, and power consumption is minimized during no-load condition and at normal operation.

Capacitor C5 is used to provide local decoupling at the BP1 pin of IC U1. Capacitor C6 provides the decoupling for BP2 pin. Diode D1 and capacitor C7 form a bootstrap circuit to provide the bias for the high-side BP2 pin. Resistor R5 limits the current flowing into the BP2 pin.

Zener diode VR3 offers primary sensed output overvoltage protection. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at the output of the converter, the auxiliary winding voltage increases and causes breakdown of VR3 which then causes excess current to flow into the BPP pin of InnoSwitch4-Pro IC. If the current flowing into the BPP pin increases above the I_{SD} threshold, the InnoSwitch4-Pro controller will latch off and prevent any further increase in output voltage. Resistor R11 limits the current injected to BPP pin when the output overvoltage protection is triggered.

4.3 *InnoSwitch4-Pro IC Secondary*

The secondary-side of the InnoSwitch4-Pro IC provides output voltage and current sensing and a gate drive to a FET for synchronous rectification. The voltage across the transformer secondary winding is rectified by the secondary-side synchronous rectifier FET (SR FET) Q2 and filtered by capacitors C16 and C17. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via an RCD snubber, R13, C13, and D4. Diode D4 minimizes the dissipation in resistor R13. Schottky diode D3 minimizes the losses that happen during the ClampZero switch conduction period.

The gate of Q2 is turned on by secondary-side controller inside IC U2, based on the secondary winding voltage sensed via resistor R12 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the SR FET is turned off just prior to the secondary-side commanding through FluxLink a new switching cycle from the primary. In discontinuous mode of operation, the SR FET is turned off when the magnitude of the voltage drop across the SR FET falls below a threshold of approximately $V_{SR(TH)}$. Secondary-side control of the primary-side power switch avoids any possibility of cross conduction of the two switches and provides extremely reliable synchronous rectifier operation.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. For this design, a secondary bias winding circuit is used to further improve the system efficiency. Bias winding voltage is rectified by diode D6 and filtered by capacitor C20. Resistor R16 limits the current flowing to the BPS pin of U2.



Capacitor C19 connected to the BPS pin of InnoSwitch4-Pro IC provides decoupling for the internal circuitry.

The output current is sensed by monitoring the voltage drop across resistor R15. The current measurement is filtered with resistor R14 and capacitor C15, and then monitored across the IS and SECONDARY GROUND pins. An internal current sense threshold of up to approximately 32 mV configured by the USB PD controller via I²C interface is used to reduce the losses. Once the threshold is exceeded, the InnoSwitch4-Pro IC responds depending on its configuration to either maintain a fixed output current by using variable frequency and variable primary switch peak current limit control schemes to maintain a fixed output current or to shut down the power supply.

For constant current (CC) operation, when the output voltage falls below 5 V, the secondary-side controller inside InnoSwitch4-Pro IC will power itself from the secondary winding directly. During the on-time of the primary-side power switch, the forward voltage that appears across the secondary winding is used to charge the SECONDARY BYPASS pin decoupling capacitor C19 via resistor R12 and an internal regulator. This allows output current regulation to be maintained down to the minimum UV threshold. Below this level the unit enters auto-restart until the output load is reduced.

When the output current is below the CC threshold, the converter operates in constant voltage mode. The output voltage is monitored by the VOUT pin of the InnoSwitch4-Pro IC. Similar with current regulation, the output voltage is also compared to an internal voltage threshold that is set via the integrated secondary controller of the InnoSwitch4-Pro IC and the USB PD controller IC, and output voltage regulation is achieved by variable frequency and variable primary switch peak current limit control schemes. Capacitor C14 is used as decoupling capacitor for the VOUT pin.

N-channel MOSFET Q3 functions as the bus switch which connects or disconnects the output of the flyback converter from the USB Type-C receptacle. MOSFET Q3 is controlled by the VB/D pin on the InnoSwitch4-Pro IC. Diode D5 is connected across the Source and Gate terminals of Q3 and resistor R17 is connected from the Gate terminal of Q3 to the VB/D pin to provide a discharge path for the bus voltage when Q3 is turned off. Capacitor C21 is used at the output for ESD protection and output voltage ripple reduction.

4.4 *USB Type-C and PD Interface*

In this design, Injoinic IP2726S (U3) is the USB Type-C and PD controller. The IP2726S device is powered directly from the flyback output voltage VBUS_IN. USB PD protocol is communicated over either CC1 or CC2 line depending on the orientation in which USB Type-C plug is connected.

The IP2726S IC communicates with InnoSwitch4-Pro IC through the I²C interface using the SCL and SDA lines in which it sets several command registers, such as the CV, CC, VKP, OVA and UVA parameters. These parameters correspond to the output voltage,



constant output current, constant output power voltage threshold, output overvoltage threshold, and output undervoltage threshold registers of the InnoSwitch4-Pro IC, respectively. The status of the InnoSwitch4-Pro IC is read by the IP2726S IC from the telemetry registers also using the I²C interface.

Capacitor C18 is used as decoupling capacitor on uVCC pin of U2. Resistors R19 and R20 are used as pull-up resistors for SDA and SCL respectively.

Capacitor C22 is used as decoupling capacitor on VIN pin of U3 and capacitor C23 is used as decoupling capacitor on VCC pin of U3. Resistor R25, R26, C25, C26, D8 and D9 are used to protect the CC1 and CC2 lines from ESD surge events.



5 PCB Layout

Layers: Two (2)
 Board Material: FR4
 Board Thickness: 1.6 mm
 Copper Weight: 2 oz

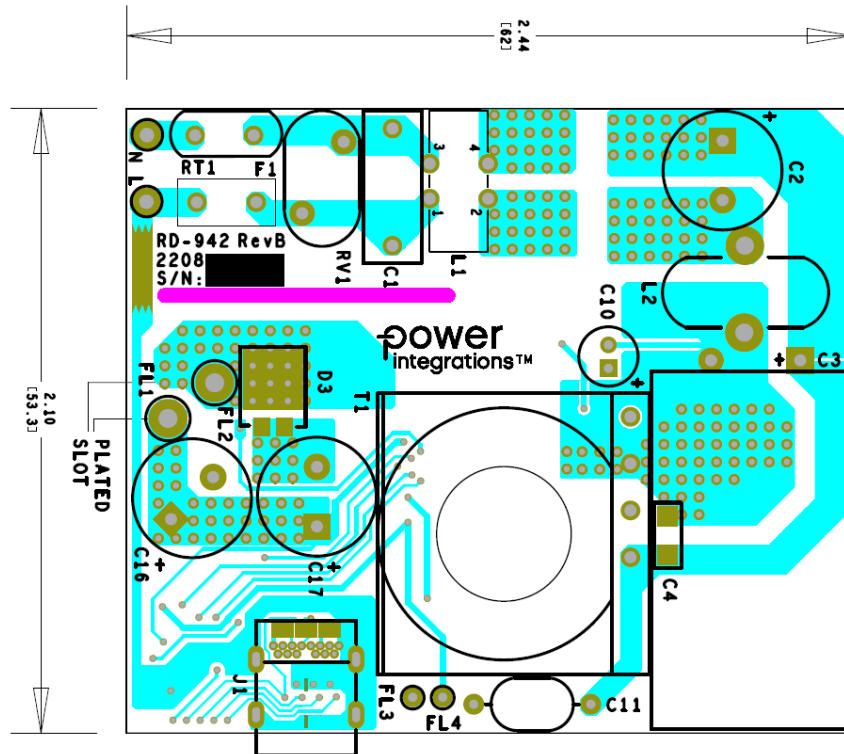


Figure 7 – DER-942 RevB PCB Layout, Top.

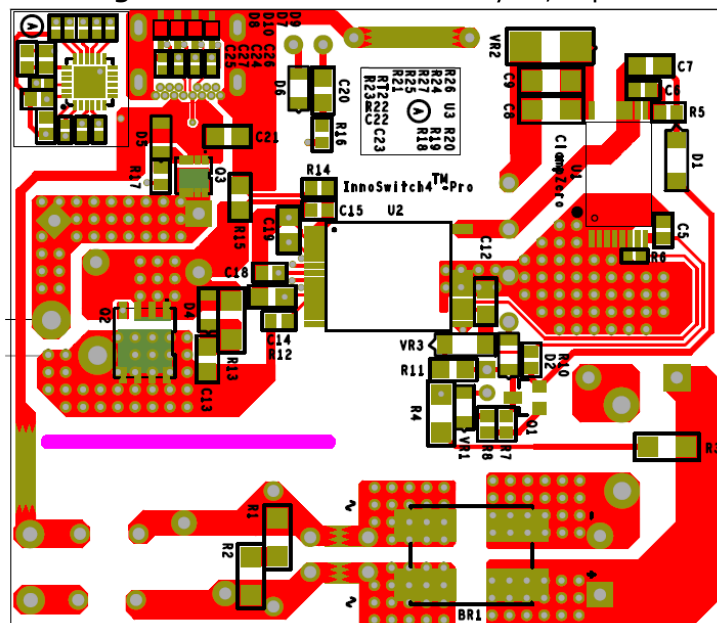


Figure 8 – DER-942 RevB PCB Layout, Bottom.



6 Bill of Materials

6.1 Electrical Parts

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	RECT BRIDGE, GP, 800 V, 4 A, Z4-D	Z4DGP408L-HF	Comchip
2	1	C1	0.1 μ F, 20%, 275 VAC, 560 VDC, X2, -40°C ~ 110°C, 5 mm W x 13 mm L x 11.1 mm H	R46KF310000P1M	KEMET
3	1	C2	18 μ F, 20%, 400 V, Electrolytic, Gen. Purpose, (10 x 16 mm), 2000 Hrs @ 105°C	400AX18MEFC10X16	Rubycon
4	1	C3	Electrolytic, 100 μ F, 400 V, Aluminum, Radial, Can, -40 °C ~ 105 °C, 12000 Hrs @ 105 °C ,(16 x 32)	400BXW100MEFR16X30	Rubycon
5	1	C4	2.2 nF, 630 V, Ceramic, X7R, 1206	C3216X7R2J222K115AA	TDK
6	3	C5 C6 C18	100 nF, 0.1 μ F, \pm 10%, 25 V, Ceramic, X7R, General Purpose, -55 °C ~ 125 °C, 0603	CL10B104KA8NFNC	Samsung
7	2	C7 C21	1 μ F, 50 V, Ceramic, X5R, 0805	08055D105KAT2A	AVX
8	2	C8 C9	100 nF, 200 V, Ceramic, X7R, 1206	C1206C104K2RACTU	Kemet
9	1	C10	22 μ F, \pm 20%, 63 V, Electrolytic, (5 x 12.5), LS 2 mm	63YXJ22M5X11	Rubycon
10	1	C11	470 pF, \pm 10%, 250 VAC, X1, Y1, Ceramic, B, Radial, Disc	DE1B3RA471KA4BN01F	Murata
11	1	C12	4.7 μ F \pm 10%, 25 V, X7R, 0805, -55 °C ~ 125 °C	TMK212AB7475KG-T	Taiyo Yuden
12	1	C13	2.2 nF, 200 V, Ceramic, X7R, 0805	08052C222KAT2A	AVX
13	2	C14 C19	2.2 μ F, \pm 10%, 25 V, Ceramic, X7R, 0805	CL21B225KAFNFNE	Samsung
14	1	C15	4.7 μ F, \pm 10%, 10 V, Ceramic, X7S, 0603, -55 °C ~ 125 °C, Low ESL	C1608X7S1A475K080AC	TDK
15	2	C16 C17	470 μ F, 25 V, \pm 20%, Al Organic Polymer, Gen. Purpose, Can, 15 m Ω , 2000 Hrs @ 105 °C	A750MS477M1EAAE015	KEMET
16	1	C20	10 μ F, \pm 10%, 25 V, Ceramic, X5R, 0805	GRM21BR61E106KA73K	Murata
17	1	C22	1 μ F, \pm 10%, 35 V, Ceramic, X7R, 0603	CGA3E1X7R1V105K080AE	TDK
18	1	C23	2.2 μ F, \pm 10%, 25 V, Ceramic, X7R, 0603, -55 to 125 °C	GRM188Z71E225KE43D	Murata
19	4	C24-C27	560 pF \pm 10% 50 V Ceramic X7R 0402	CCCC0402KRX7R9BB561	Yageo
20	1	D1	800 V, 1 A, High Efficiency Fast Recovery, SOD-123FL	HS1KFL	Taiwan Semi
21	1	D2	Diode, GEN PURP, FAST RECOVERY, 300 V, 225 mA, SOD323	BAV3004WS-7	Diodes, Inc.
22	1	D3	Diode, Schottky, 120 V, 12 A, SMT, TO-277A (SMPC)	V12P12-M3/86A	Vishay
23	3	D4-D6	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
24	4	D7-D10	Diode, ZENER, 24 V, 200 mW, SC-90, SOD-323F	MM3Z24VC	ON Semi
25	1	F1	3.15 A, 250 V, Slow, RST	RST 3.15-BULK	Belfuse
26	1	J1	Connector, "Certified", USB - C, USB 3.1, For 0.062" PCB Material, Superspeed+, Receptacle Connector, 24 Position, SMT, RA TH	632723300011	Würth
27	1	L1	810 μ H, Toroidal Common Mode Choke, custom, DER-942, wound on 32-00330-00 core.	32-00367-00 TSD-4905	Power Integrations Premier Magnetics
28	1	L2	68 μ H, Unshielded Toroidal Inductor, 2A, 55 m Ω Max, Radial, Vertical (Open)	7447033 TSD-4906	Würth Premier Magnetics
29	1	Q1	NPN, Small Signal BJT, 80 V, 0.5 A, SOT-23	MMBTA06LT1G	On Semi
30	1	Q2	MOSFET, N-CH, 100 V, 48 A (Tc), 113.5 W (Tc), DFN5X6, 8-DFN (5x6)	AON6220	Alpha & Omega Semi
31	1	Q3	N-Channel 30 V 36.5 A (Ta), 50A (Tc) 4.1 W (Ta), 39 W (Tc) SMT 8-DFN-EP (3.3x3.3), 8DFN, 8-PowerVDFN	AON7318	Alpha & Omega Semi
32	1	R3	RES, 2.00 M Ω , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
33	1	R4	RES, 1.80 M Ω , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1804V	Panasonic
34	1	R5	RES, 3.74 k Ω , 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF3741V	Panasonic
35	1	R6	RES, 60.4 k Ω , 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF6042X	Panasonic
36	2	R7 R23	RES, 82 k Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ823V	Panasonic
37	1	R8	RES, 2.55 k Ω , 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2551V	Panasonic
38	1	R10	RES, 3.4 k Ω , 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF3401V	Panasonic



39	1	R11	RES, 499 Ω , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4990V	Panasonic
40	1	R12	RES, 47 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
41	1	R13	RES, 10 Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ100V	Panasonic
42	1	R14	RES, 10 Ω , 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF10R0V	Panasonic
43	1	R15	RES, 0.009 Ω , \pm 1%, 0.5 W, 0805, Current Sense, Moisture Resistant, Metal Element	CRF0805-FZ-R009ELF	Bourns
44	1	R16	RES, 820 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ821V	Panasonic
45	1	R17	RES, 560 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ561V	Panasonic
46	2	R19 R20	RES, 2.20 k Ω , 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF2201X	Panasonic
47	1	R21	RES, 10 k Ω , 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ103X	Panasonic
48	1	R22	RES, 1 k Ω , 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ102X	Panasonic
49	2	R24 R27	RES, 3.3 Ω , 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ3R3X	Panasonic
50	2	R25 R26	RES, 22 Ω , 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ220X	Panasonic
51	1	RT1	NTC Thermistor, 2.5 Ω , 3 A	SL08 2R503	Ametherm
52	1	RT2	NTC Thermistor, 100 k Ω , 1%, 4250K, 0603	NCU18WF104F60RB	Murata
53	1	RV1	300 Vac, 25 J, 7 mm, RADIAL	V300LA4P	Littlefuse
54	1	T1	Custom, DER-942 Transformer EQ25, Lp=575uH	POL-INN058	Premier Magnetics
55	1	U1	ClampZero, MinSOP-16	CPZ1075M	Power Integrations
56	1	U2	InnoSwitch4-Pro, InSOP-T28D	INN4373F-H341	Power Integrations
57	1	U3	IC, Fast Charging Physical Layer IC for USB Interfaces	IP2726S	INJOINIC TECHNOLOGY
58	1	VR1	11 V, \pm 5%, 200 mW, SOD-323	MM3Z11VC	ON Semi
59	1	VR2	275 V Clamp 1.5 A Ipp Tvs Diode Surface Mount DO-214AC (SMA), SMAJ (DO-214AC)	SMAJ170A	Littelfuse
60	1	VR3	Diode ZENER 36 V 500 mW SOD123	MMSZ5258B-7-F	Diodes, Inc.

Note: Although there is a provision for R1, R2, and R18 in the layout, these parts are not needed and hence not assembled.

6.2 Mechanical Parts

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	L	TEST Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone Electronics
2	1	N	TEST Point, WHT, Miniature THRU-HOLE MOUNT	5002	Keystone Electronics



7 Common Mode Choke Specifications (L1)

7.1 Electrical Diagram

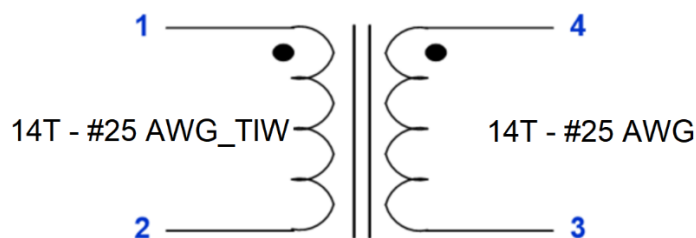


Figure 9 – Inductor Electrical Diagram.

7.2 Electrical Specifications

Parameter	Condition	Spec.
Inductance	Across pin 1 to pin 2 (or pin 4 to pin 3) with the other winding open. LCR meter Ls measurement, 100 kHz switching frequency, 1.0 V test level.	810 μ H \pm 30%
DC Resistance	Across pin 1 to pin 2 (or pin 4 to pin 3) with the other winding open.	40 m Ω (Max.)

7.3 Material List

Item	Description
[1]	Core, Ferrite Inductor Toroid, 9 mm OD x 5 mm ID x 3 mm H. AL = 4150 nH/N ² \pm 30% PI#: 32-00330-00.
[2]	Magnet Wire: #25 AWG, Triple Insulated Wire.
[3]	Magnet Wire: #25 AWG, Double Coated.
[4]	Varnish: Dolph BC-359.

7.4 Winding Instructions

Start as pin 1 for Item [2] and pin 4 for Item [3].

Wind together 14 turns to core Item [1].

Mark end of Item [2] as pin 2 and end of Item [3] as pin 3.

Cut the wires with practically short length remaining (~1 inch each) such the CMC can be easily populated into the PCB.

Varnish the CMC using Item [4].

Cut excess wire when soldering into the PCB.

8 Transformer Specification (T1)

8.1 Electrical Diagram

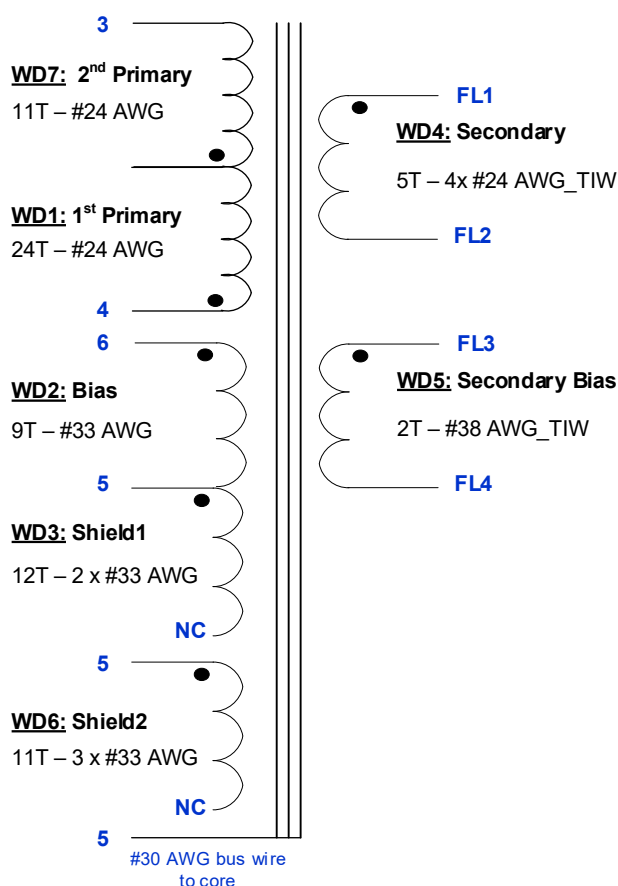


Figure 10 – Transformer Electrical Diagram.

8.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Across pin 3 to pin 4, with all other windings open. LCR meter L _s measurement, 100 kHz, 1.0 V test level.	575 μ H \pm 7%
Primary Leakage Inductance	Across pin 3 to pin 4, with FL1 and FL2 shorted. LCR meter L _s measurement, 100 kHz, 1.0 V test level.	7 μ H (Typ.)
Electrical Strength (Primary to Secondary)	Across shorted primary windings (pins 3, 4, 5, 6) to shorted secondary winding (FL1, FL2, FL3, FL4).	3000 VAC, 200 V / s ramp rate, 60 s soak

8.3 Transformer Build Diagram

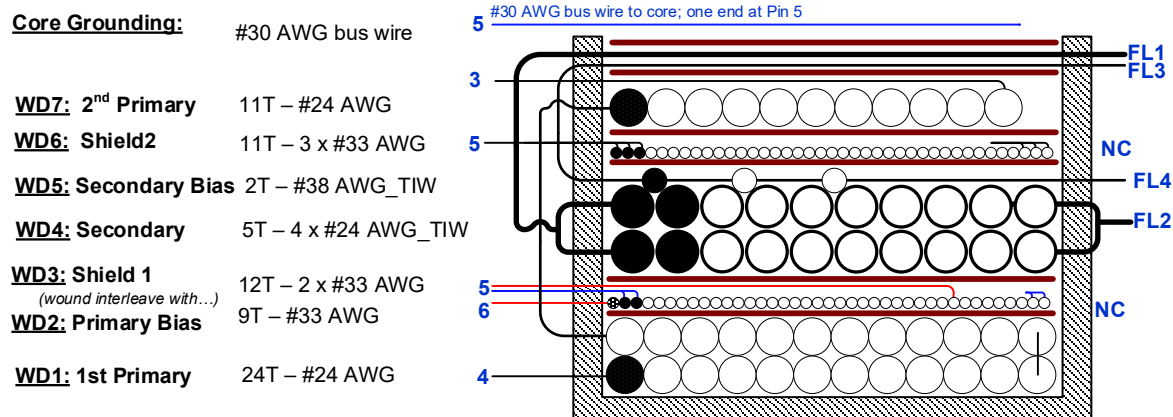

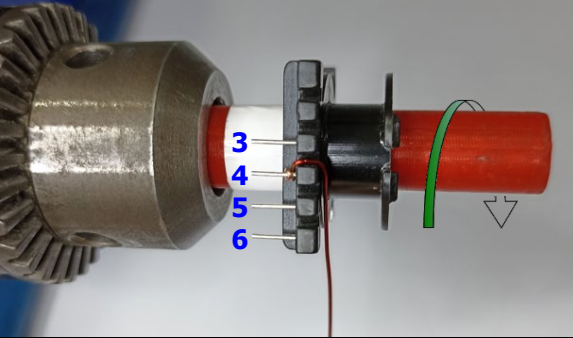
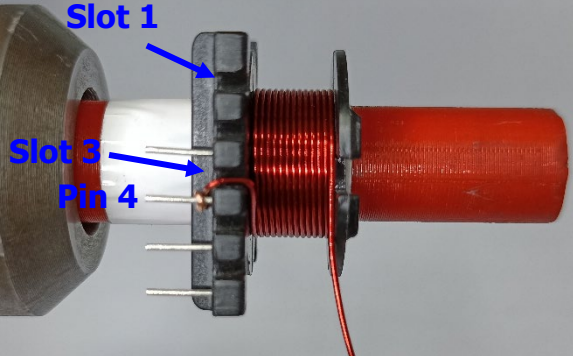


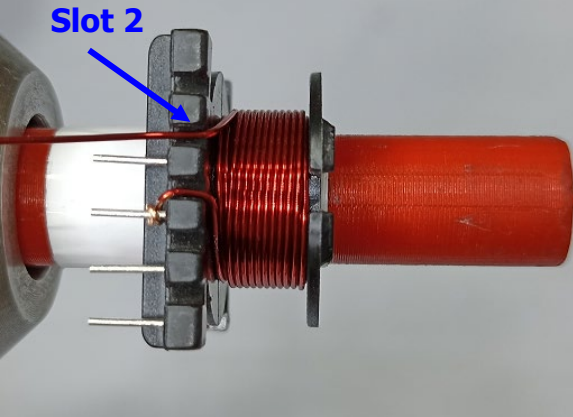
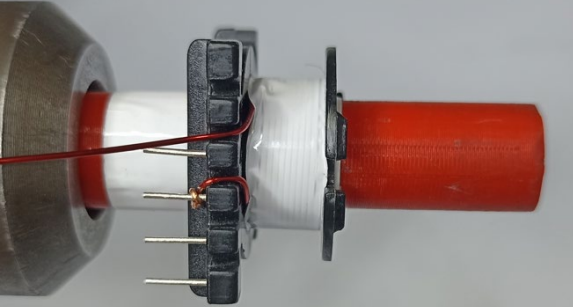
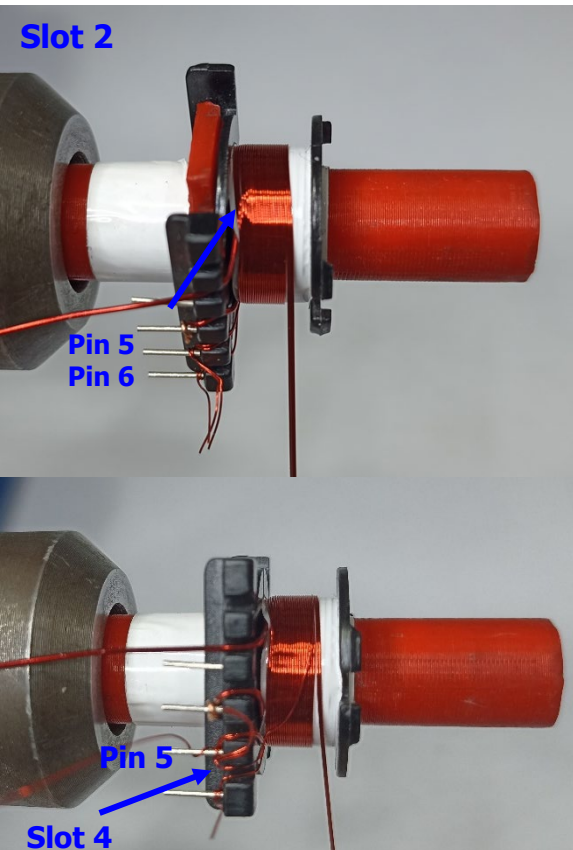
Figure 11 – Transformer Build Diagram.

8.4 Material List

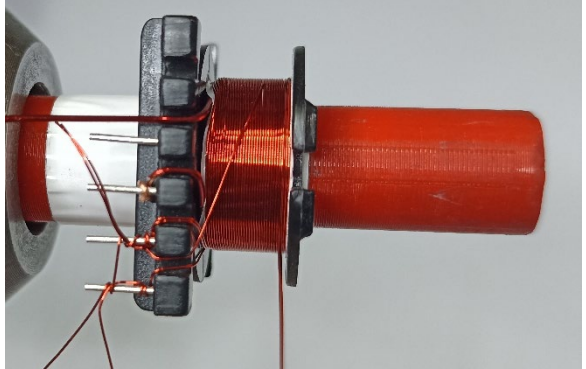
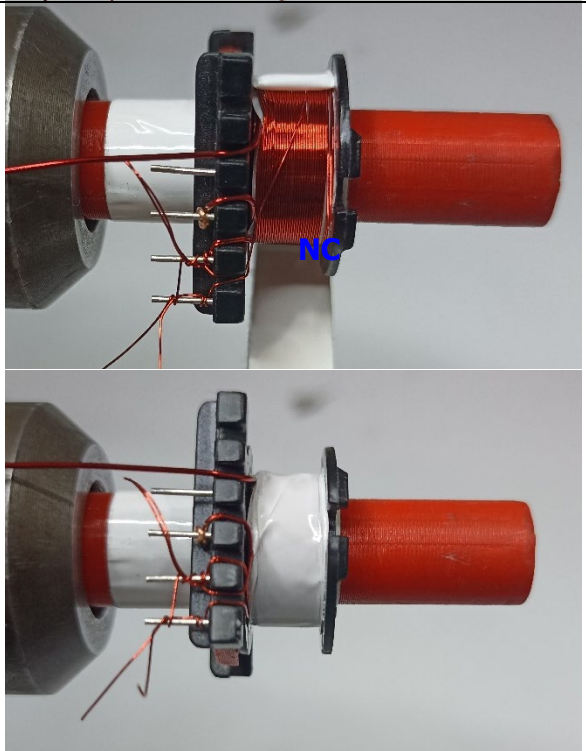
Item	Description
[1]	Core: EQ25, Material 3C95. FerroxCube.
[2]	Bobbin. EQ25-V-6pins. PI#: 25-01136-00.
[3]	Magnet Wire: #24 AWG, Double Coated.
[4]	Magnet Wire: #33 AWG, Double Coated.
[5]	Magnet Wire: #24 AWG, Triple Insulated Wire.
[6]	Magnet Wire: #38 AWG, Triple Insulated Wire.
[7]	Bus Wire: #30 AWG (Solid) Tinned Copper.
[8]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 8.4 mm Width.
[9]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 18.2 mm Width.
[10]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 25 mm Width.
[11]	Varnish: Dolph BC-359 or Equivalent.

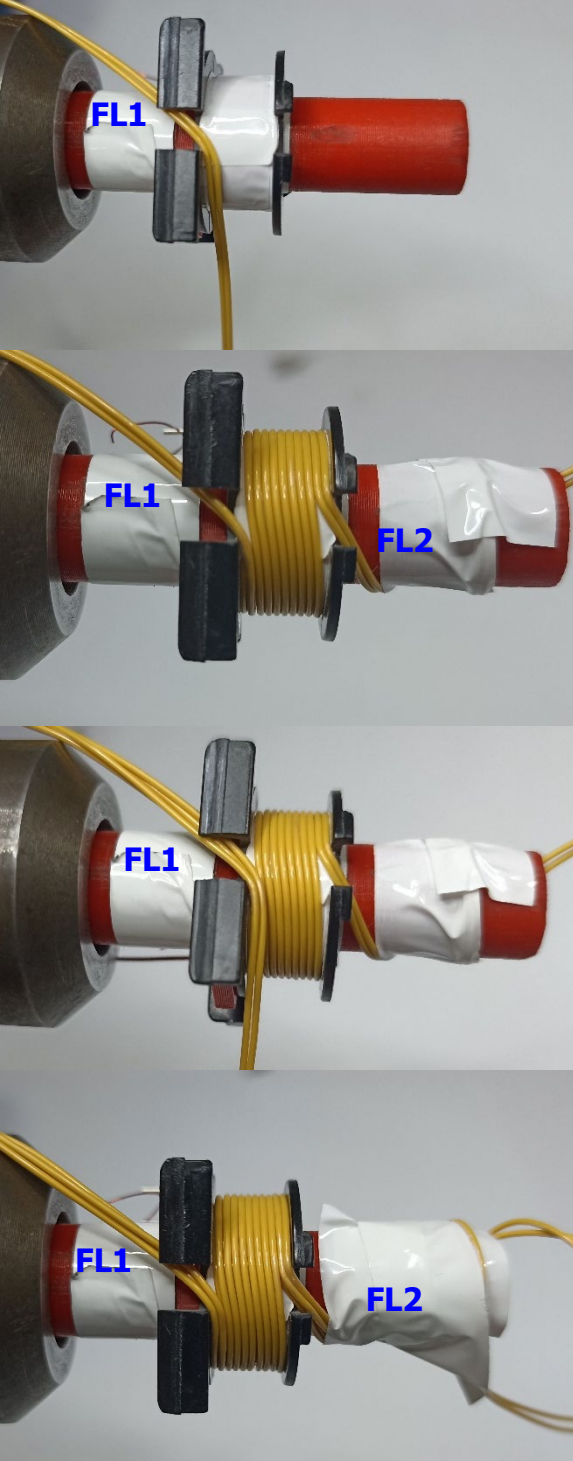
8.5 *Winding Instructions*

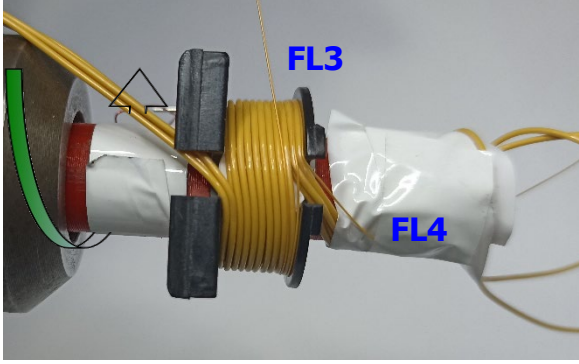
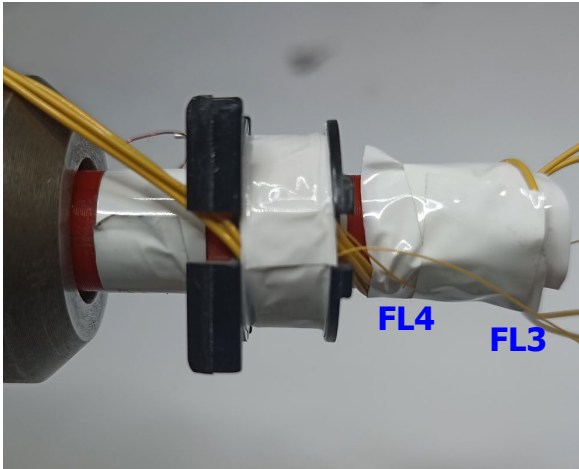
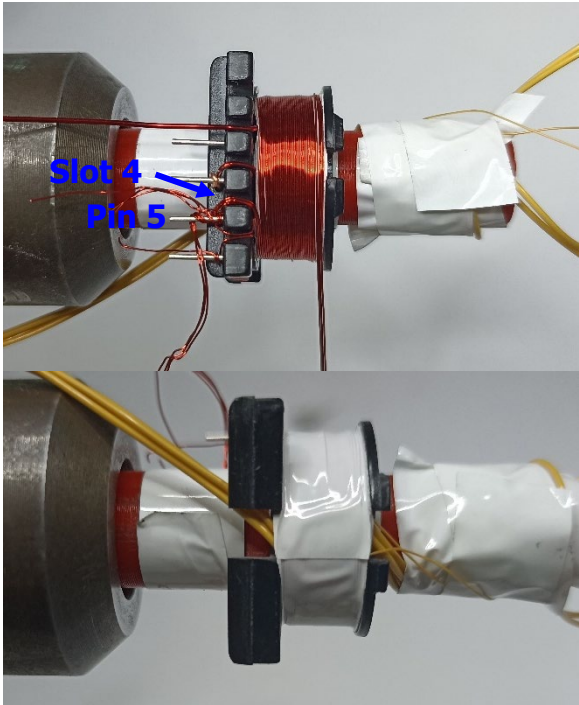
<p>Bobbin Preparation</p>		<p>Prepare the bobbin by removing pins 1 & 2 and creating 4 mm wide slots in the secondary</p>
<p>Bobbin and Winding Preparation</p>		<p>Position the bobbin on the mandrel such that the pin side of the bobbin is on the left side.</p> <p>Rotation of the mandrel is clock-wise as seen from the right side of the set-up.</p>
<p>WD1 1st Primary – Layer 1</p>		<p>Prepare 180 cm wire Item [3]</p> <p>Start at pin 4, enter wire to bobbin slot 3, and wind 13 turns of wire Item [3] in 1 layer, from left to right.</p>

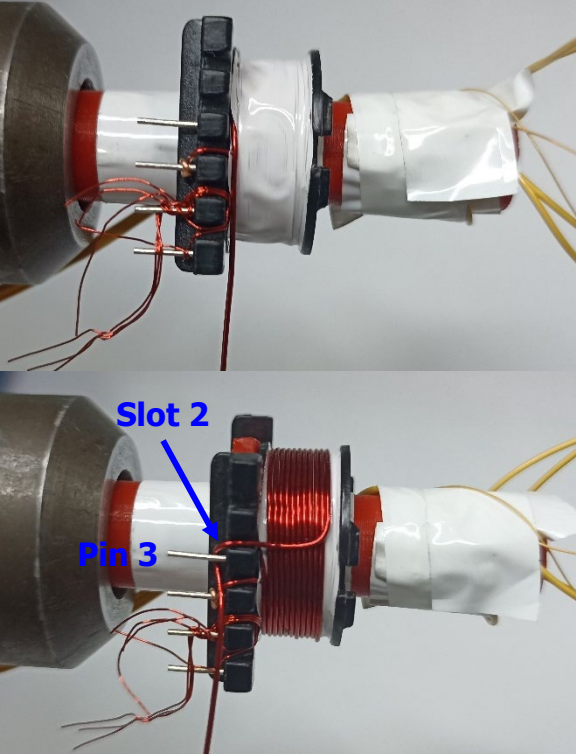
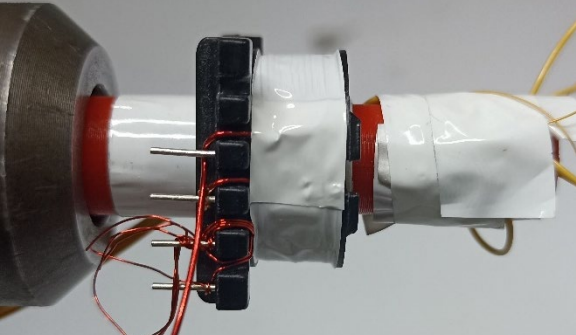
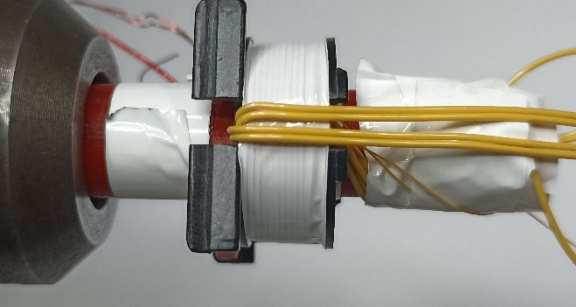
<p>WD1 1st Primary – Layer 2</p>		<p>Continue winding another 11 turns from right to left. At the end of the last turn, exit the wire out of the bobbin at Slot 2. The wire left over will be used for the 2nd half primary (11 turns)</p>
<p>Insulation</p>		<p>1 layer of tape Item [8].</p>
<p>WD2: Bias & WD3: Shield 1</p>		<p>Prepare 3x75 cm strands of wire Item [4]</p> <p>Use 1 wire Item [4] for WD2 (Bias). Start at pin 6 and enter to bobbin slot 4.</p> <p>Use another 2 wires Item [4] for WD3 (Shield 1). Start at pin 5 and enter wire to bobbin slot 4.</p> <p>Wind all the wires together for 9 turns then terminate the wire for bias to pin 5 through slot 4.</p>

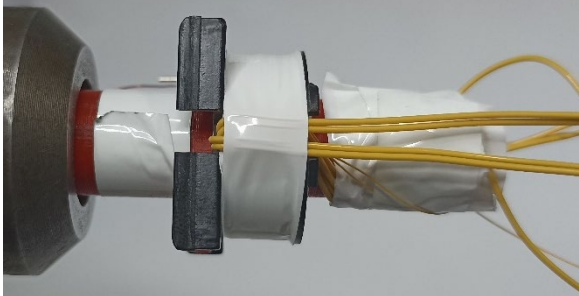
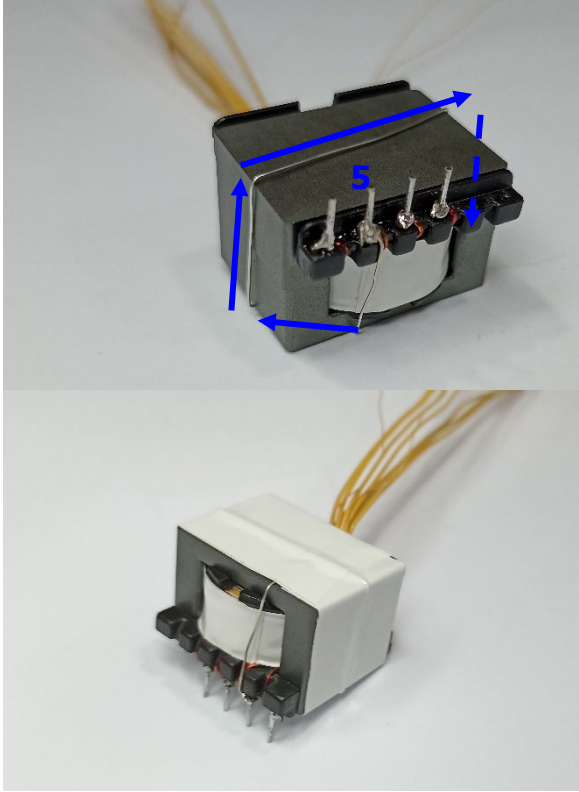


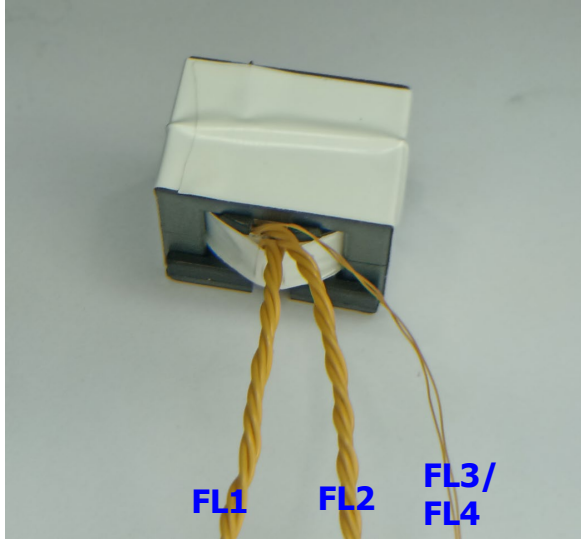
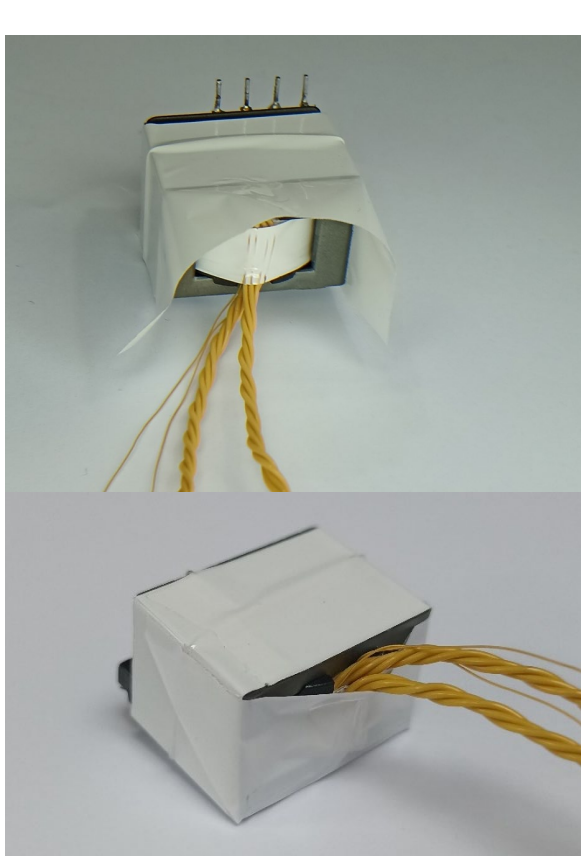
		<p>Continue winding the wires for Shield 1 for additional 3 turns (total of 12 turns) to fill the layer</p>
<p>Shield 1 No Connect & Insulation</p>		<p>Add tape item [8] to secure the windings but do not complete the turn. Cut the wires and leave as No-Connect. Complete the turn for 1 layer of tape.</p>

<p>WD4 Secondary</p>		<p>Prepare 4x60cm strands of wire item [5]</p> <p>Start at the secondary left slot of the bobbin. Use 2 wires Item [5], leave 5cm floating, and mark as FL1.</p> <p>Wind 5 turns in 1 layer.</p> <p>At the end of last turn, exit the wires at the right slot, leave 5cm floating and mark as FL2 for 1st half of Secondary.</p> <p>Repeat another winding same as above for 2nd half of Secondary, which is parallel with 1st half Secondary.</p>
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<p>Secondary Bias</p>		<p>Use item [6] for WD5 (Secondary Bias)</p> <p>Start at the right side with FL4 then wind 2 turns from right to left by turning the mandrel in the counter clockwise direction.</p> <p>Follow the ridges made by the secondary winding to minimize the bump in the next shield layer.</p>
<p>Insulation</p>		<p>Exit FL3 on the right side of the bobbin. 2 layers of tape Item [8].</p>
<p>WD6 Shield2</p>		<p>Use 3x90cm wires Item [4] for WD6 (Shield 2).</p> <p>Start with Pin 5, enter bobbin through slot 4, and wind 11 turns.</p> <p>Cut the wires and leave as No-connect</p> <p>Use 1 layer of tape Item [8]</p>

<p>WD7 2nd Primary</p>		<p>Use the wire leftover from WD1 and continue winding 11 turns from left to right.</p> <p>Exit the wire to pin 3 through Slot 2</p>
<p>Insulation</p>		<p>1 layer of tape Item [8].</p>
<p>WD4 Secondary</p>		<p>Fold the wires of the secondary winding FL1 from the left slot to exit to the right slot.</p>

<p>Insulation</p>		<p>1 layer of tape Item [8]</p>
<p>Gap and Ground Core</p>		<p>Solder the wires to their respective bobbin pins (pin 3, 4, 5, 6).</p> <p>Add gap to the middle leg of core Item [1] to get 575 μH $\pm 7\%$ primary inductance.</p> <p>Solder one end of bus wire item [7] to pin 5 and wrap the bus wire along both core halves.</p> <p>Secure core halves by wrapping 2 layers of tape Item [9] along the transformer bottom, sides, and top.</p> <p>Ensure primary inductance is still 575 μH $\pm 7\%$.</p>

<p>Twist fly leads</p>	 <p>A photograph of a transformer core with four yellow fly leads. The leads are twisted in pairs. The left pair is labeled 'FL1', the middle pair 'FL2', and the right pair 'FL3/FL4'.</p>	<p>Twist together the 4 wires of FL1</p> <p>Twist together the 4 wires of FL2</p> <p>Twist together FL3 and FL4</p> <p>Trim each of the fly leads to 5 cm.</p>
<p>Tape for Core Insulation</p>	 <p>Two photographs showing the transformer core being insulated with white tape. The top photo shows the tape being applied to the bottom and secondary side of the core. The bottom photo shows the completed transformer with the tape fully applied.</p>	<p>Cover the transformer core bottom and secondary side with 2 layers of tape item [10] for improved ESD performance</p>

<p>Finish Assembly</p>		<p>Secure the assembly with 1 layer of tape Item [8] along the transformer sides.</p> <p>Varnish with Item [11] to complete the transformer.</p> <p>Cut excess fly lead wire after soldering the transformer into the PCB.</p>
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9 Transformer Design Spreadsheet

1	ACDC_InnoSwitch4-Pro_Flyback_092322; Rev.1.0; Copyright Power Integrations 2022	INPUT	INFO	OUTPUT	UNIT S	InnoSwitch4-Pro Flyback Design Spreadsheet
2	APPLICATION VARIABLES					
3	INPUT_TYPE	AC		AC		Input Type
4	VIN_MIN			90	V	Minimum AC input voltage
5	VIN_MAX			265	V	Maximum AC input voltage
6	VIN_RANGE			UNIVERSAL		Input voltage range
7	FLINE			60	Hz	AC Input voltage frequency
8	CAP_INPUT	118.0		118.0	uF	Input capacitance
10	SET-POINT 1					
11	VOUT1	21.000		21.000	V	Output voltage 1, should be the highest output voltage required
12	CDC1	0.000		0.000	V	Cable-drop compensation required on set-point 1
13	IOUT1	3.000		3.000	A	Output current 1
14	POUT1		Info	63.00	W	The output power required exceeds the device capability: Verify thermal performance if no other warnings
15	EFFICIENCY1	0.93		0.93		Converter efficiency for output 1
16	Z_FACTOR1	0.60		0.60		Z-factor for output 1
17	TYPE	APDO		APDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
19	SET-POINT 2					
20	VOUT2	20.000		20.000	V	Output voltage 2
21	CDC2	0.000		0.000	V	Cable-drop compensation required on set-point 2
22	IOUT2	3.250		3.250	A	Output current 2
23	POUT2		Info	65.00	W	The output power required exceeds the device capability: Verify thermal performance if no other warnings
24	EFFICIENCY2	0.93		0.93		Converter efficiency for output 2
25	Z_FACTOR2	0.60		0.60		Z-factor for output 2
26	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
28	SET-POINT 3					
29	VOUT3	15.000		15.000	V	Output voltage 3
30	CDC3	0.000		0.000	V	Cable-drop compensation required on set-point 3
31	IOUT3	3.000		3.000	A	Output current 3
32	POUT3			45.00	W	Output power 3
33	EFFICIENCY3	0.92		0.92		Converter efficiency for output 3
34	Z_FACTOR3	0.60		0.60		Z-factor for output 3
35	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
37	SET-POINT 4					
38	VOUT4	12.000		12.000	V	Output voltage 4
39	CDC4	0.000		0.000	V	Cable-drop compensation required on set-point 4
40	IOUT4	3.000		3.000	A	Output current 4
41	POUT4			36.00	W	Output power 4
42	EFFICIENCY4	0.91		0.91		Converter efficiency for output 4
43	Z_FACTOR4	0.60		0.60		Z-factor for output 4



44	TYPE	PDO	Info	PDO		The voltage entered is not a standard PDO(Power Delivery Object)
46 SET-POINT 5						
47	VOUT5	9.000		9.150	V	Output voltage 5
48	CDC5	0.150		0.150	V	Cable-drop compensation required on set-point 5
49	IOUT5	3.000		3.000	A	Output current 5
50	POUT5			27.45	W	Output power 5
51	EFFICIENCY5	0.90		0.90		Converter efficiency for output 5
52	Z_FACTOR5	0.60		0.60		Z-factor for output 5
53	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
55 SET-POINT 6						
56	VOUT6	5.000		5.150	V	Output voltage 6
57	CDC6	0.150		0.150	V	Cable-drop compensation required onset-point 6
58	IOUT6	3.000		3.000	A	Output current 6
59	POUT6			15.45	W	Output power 6
60	EFFICIENCY6	0.88		0.88		Converter efficiency for output 6
61	Z_FACTOR6	0.60		0.60		Z-factor for output 6
62	TYPE	PDO	Info	PDO		Select whether this set-point is a PDO (Power Delivery Object) or APDO (Augmented Power Delivery Object)
64 SET-POINT 7						
65	VOUT7	3.300		3.300	V	Output voltage 7
66	CDC7	0.000		0.000	V	Cable-drop compensation required onset-point 7
67	IOUT7	3.000		3.000	A	Output current 7
68	POUT7			9.90	W	Output power 7
69	EFFICIENCY7	0.88		0.88		Converter efficiency for output 7
70	Z_FACTOR7	0.60		0.60		Z-factor for output 7
71	TYPE	APDO		APDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
92 PRIMARY CONTROLLER SELECTION						
93	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
94	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
95	VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
96	DEVICE_GENERIC	INN4373		INN4373		Device selection
97	DEVICE_CODE			INN4373F		Device code
98	PDEVICE_MAX			60	W	Device maximum power capability
99	RDSON_100DEG			1.02	Ω	Primary switch on-time resistance at 100°C
100	ILIMIT_MIN			1.748	A	Primary switch minimum current limit
101	ILIMIT_TYP			1.900	A	Primary switch typical current limit
102	ILIMIT_MAX			2.052	A	Primary switch maximum current limit
103	VDRAIN_ON_PRSW			0.75	V	Primary switch on-time voltage drop
104	VDRAIN_OFF_PRSW			570.31	V	Peak drain voltage on the primary switch during turn-off
108 WORST CASE ELECTRICAL PARAMETERS						
109	FSWITCHING_MAX	97000	Info	97000	Hz	The worst case minimum operating frequency is less than 25kHz: may result in audible noise
110	VOR	147.0		147.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
111	VMIN			93.40	V	Valley of the rectified minimum input AC voltage at full load



112	KP			0.592		Measure of continuous/discontinuous mode of operation
113	MODE_OPERATION			CCM		Mode of operation
114	DUTYCYCLE			0.611		Primary switch duty cycle
115	TIME_ON			10.95	us	Primary switch on-time
116	TIME_OFF			3.61	us	Primary switch off-time
117	LPRIMARY_MIN			547.4	uH	Minimum primary magnetizing inductance
118	LPRIMARY_TYP			576.2	uH	Typical primary magnetizing inductance
119	LPRIMARY_TOL			5.0	%	Primary magnetizing inductance tolerance
120	LPRIMARY_MAX			605.1	uH	Maximum primary magnetizing inductance
122 PRIMARY CURRENT						
123	I _{AVG_PRIMARY}			0.733	A	Primary switch average current
124	I _{PEAK_PRIMARY}			1.962	A	Primary switch peak current
125	I _{PEDESTAL_PRIMARY}			0.707	A	Primary switch current pedestal
126	I _{RIPPLE_PRIMARY}			1.857	A	Primary switch ripple current
127	I _{RMS_PRIMARY}			1.002	A	Primary switch RMS current
129 SECONDARY CURRENT						
130	I _{PEAK_SECONDARY}			13.736	A	Secondary winding peak current
131	I _{PEDESTAL_SECONDARY}			4.947	A	Secondary winding pedestal current
132	I _{RMS_SECONDARY}			5.706	A	Secondary winding RMS current
133	I _{RIPPLE_CAP_OUT}			4.690	A	Output capacitor ripple current
137 TRANSFORMER CONSTRUCTION PARAMETERS						
138 CORE SELECTION						
139	CORE	EQ25		EQ25		Core selection. Refer to the "Transformer Construction" tab for the detailed report.
140	CORE NAME			EQ25-3C95		Core code
141	AE			100.0	mm ²	Core cross sectional area
142	LE			41.4	mm	Core magnetic path length
143	AL			5710	nH	Ungapped core effective inductance per turns squared
144	VE			4145	mm ³	Core volume
145	BOBBIN NAME			TBI-235-01091.1206		Bobbin name
146	AW			34.8	mm ²	Bobbin window area
147	BW			8.10	mm	Bobbin width
148	MARGIN			0.0	mm	Bobbin safety margin
150 PRIMARY WINDING						
151	N _{PRIMARY}			35		Primary winding number of turns
152	B _{PEAK}			3699	Gauss	Peak flux density
153	B _{MAX}			3356	Gauss	Maximum flux density
154	B _{AC}			1581	Gauss	AC flux density (0.5 x Peak to Peak)
155	AL _G			470	nH	Typical gapped core effective inductance per turns squared
156	LG			0.245	mm	Core gap length
158 PRIMARY BIAS WINDING						
159	N _{BIAS_PRIMARY}			9		Primary bias winding number of turns
161 SECONDARY WINDING						
162	N _{SECONDARY}	5		5		Secondary winding number of turns
163						
164 SECONDARY BIAS WINDING						
165	N _{BIAS_SECONDARY}			2		Secondary bias winding number of turns
168 PRIMARY COMPONENTS SELECTION						
169 CLAMPZERO						
170	L _{LEAK}	6.80		6.80	uH	Primary winding leakage inductance



171	CCLAMP			100.0	nF	Primary clamp capacitor
172	RD_CLAMPZERO	AUTO		30	kΩ	HSD resistor
173	TLLDL/THLDL			120.0	ns	HSD resistor programmed delay
174	TIME_CLAMPZERO_OFF_TO_PRIMARY_ON			65.0	ns	Time between the ClampZero FET turn off and the primary FET turns on based on the HSD resistor selection
175	TIME_VDS_VALLEY			53.7	ns	Time taken by the VDS ring to reach its first valley
176	IPEAK_CLAMPZERO			1.915	A	Active clamp peak current
178 LINE UNDERVOLTAGE/OVERVOLTAGE						
179	BROWN-IN REQUIRED			72.00	V	Required AC RMS/DC line brown-in threshold
180	RLS			3.56	MΩ	Connect two 1.78 MOhm resistors to the V-pin for the required UV/OV threshold
181	BROWN-IN ACTUAL			71.40	V	Actual AC RMS/DC brown-in threshold using standard resistors
182	BROWN-OUT ACTUAL			64.58	V	Actual AC RMS/DC brown-out threshold using standard resistors
183	OVERVOLTAGE_LINE			300.47	V	Actual AC RMS/DC line over-voltage threshold
185 PRIMARY BIAS WINDING						
186	VBIAS_PRIMARY	8.00	Info	8.00	V	The rectified primary bias voltage maybe too low to supply the BPP pin: Increase the rectified primary bias voltage to a value higher than 9V
187	VF_BIAS_PRIMARY			0.70	V	Primary bias winding diode forward drop
188	VREVERSE_BIASDIODE_PRIMARY			133.79	V	Primary bias diode reverse voltage (not accounting parasitic voltage ring)
189	CBIAS_PRIMARY			22	uF	Primary bias winding rectification capacitor
190	CBPP			4.70	uF	BPP pin capacitor
194 SECONDARY COMPONENTS SELECTION						
195 RECTIFIER						
196	VDRAIN_OFF_SRFET			74.54	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
197	SRFET	AUTO		AO4294		Secondary rectifier (Logic MOSFET)
198	VBREAKDOWN_SRFET			100	V	Secondary rectifier breakdown voltage
199	RDS_ON_SRFET			15.5	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
201 SECONDARY BIAS WINDING						
202	USE_SECONDARYBIAS	AUTO		YES		Select to use secondary bias winding or not
203	VBIAS_SECONDARY			6.00	V	Rectified secondary bias voltage at full load
204	VF_BIAS_SECONDARY			0.70	V	Secondary bias winding diode forward drop
205	VREVERSE_BIASDIODE_SECONDARY			27.42	V	Secondary bias diode reverse voltage (not accounting parasitic voltage ring)
206	CBIAS_SECONDARY			10	uF	Secondary bias winding rectification capacitor
207	CBPS			2.20	uF	BPS pin capacitor



10 Performance Data

Note: 1. Output voltage measured on the PCB unless otherwise specified.
2. For data points showing performance across varying input line voltage and output load current, measurements were taken from full load to no load, with input line voltage from low-line to high-line, at room temperature ambient (approximately 25 °C) unless otherwise specified.

10.1 No-Load Input Power

Note: 1. Unit tested without Type-C cable connected to output.
2. For each line voltage, soak time = 10 min and integration time = 5 min.

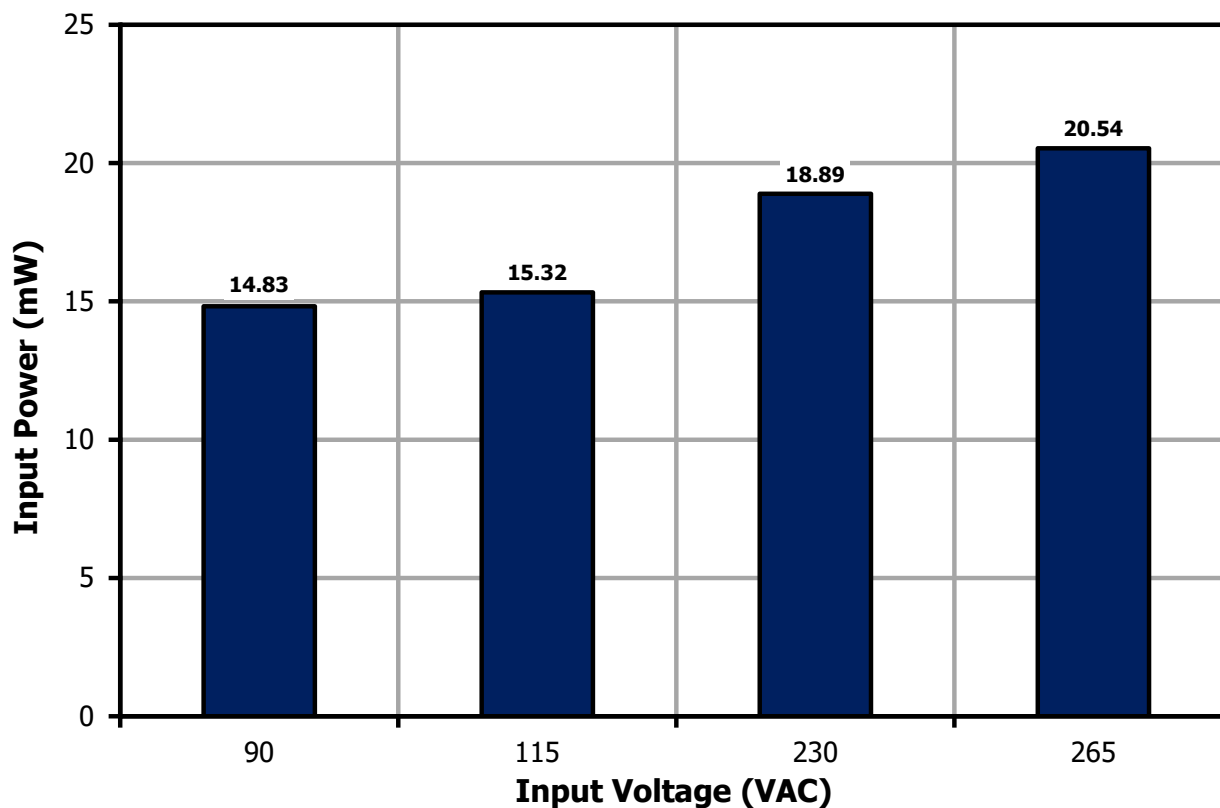


Figure 12 – No-Load Input Power vs. Input Line Voltage.

10.2 Full Load Efficiency (On-board)

V _{OUT} (V)	Load (A)	Power (W)	Full Load Efficiency (%)			
			90 VAC	115 VAC	230 VAC	265 VAC
5	3.0	15	91.44	91.85	91.35	90.85
9	3.0	27	92.09	92.62	93.03	92.71
12	3.0	36	92.24	92.80	93.51	93.29
15	3.0	45	92.33	92.92	93.80	93.62
20	3.25	65	91.67	92.91	94.06	93.97

10.3 Average and 10% Load Efficiency

Measurements were taken after 30-minute delay per input line voltage and 1-minute delay per load condition. Output voltage was measured on the board.

10.3.1 Efficiency Requirements

V _{OUT} (V)	Model (V)	Test	Average Efficiency (%)		10% Load Efficiency (%)
			Effective Power (W)	2016 DOE6 (New EISA2007)	Jan-16 CoC v5 Tier 2
		5	<6	15	81.39
9	>6	27	86.62	87.30	77.30
12	>6	36	87.40	88.30	78.30
15	>6	45	87.73	88.85	78.85
20	>6	65	88.00	89.00	79.00

10.3.2 Efficiency Performance Summary (On Board)

V _{OUT} (V)	Power (W)	Average Efficiency (%)		10% Load Efficiency (%)	
		115 VAC	230 VAC	115 VAC	230 VAC
5	15	91.35	90.18	86.89	83.51
9	27	92.18	92.17	87.42	85.94
12	36	92.29	92.71	87.00	86.58
15	45	92.32	93.07	87.07	86.97
20	65	92.37	93.43	87.47	88.25

10.3.3 Average and 10% Load Efficiency Measurements

10.3.3.1 Output: 5 V / 3.0 A

Input (VAC)	Load (%)	Design Performance					Efficiency Standards		Remarks	
		P _{IN} (W)	V _{OUT} (V)	I _{OUT} (A)	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 (%)		CoC v5 Tier 2 (%)
115	100	16.680	5.108	3.000	15.321	91.85	91.35	81.39	81.84	PASS
	75	12.466	5.091	2.249	11.452	91.87				
	50	8.303	5.068	1.500	7.601	91.55				
	25	4.191	5.039	0.750	3.778	90.15				
	10	1.735	5.031	0.300	1.508	86.89				
230	100	16.810	5.119	3.000	15.356	91.35	90.18	81.39	81.84	PASS
	75	12.590	5.098	2.249	11.467	91.08				
	50	8.420	5.072	1.500	7.607	90.34				
	25	4.301	5.044	0.750	3.782	87.93				
	10	1.806	5.033	0.300	1.508	83.51				

10.3.3.2 Output: 9 V / 3.0 A

Input (VAC)	Load (%)	Design Performance					Efficiency Standards		Remarks	
		P _{IN} (W)	V _{OUT} (V)	I _{OUT} (A)	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 (%)		CoC v5 Tier 2 (%)
115	100	29.520	9.116	2.999	27.342	92.62	92.18	86.62	87.30	PASS
	75	22.100	9.100	2.249	20.468	92.62				
	50	14.740	9.078	1.500	13.615	92.37				
	25	7.446	9.051	0.750	6.784	91.11				
	10	3.096	9.034	0.300	2.707	87.42				
230	100	29.440	9.131	2.999	27.387	93.03	92.17	86.62	87.30	PASS
	75	22.080	9.110	2.249	20.492	92.81				
	50	14.750	9.085	1.500	13.624	92.37				
	25	7.500	9.054	0.750	6.787	90.49				
	10	3.151	9.038	0.300	2.708	85.94				

10.3.3.3 Output: 12 V / 3.0 A

Input (VAC)	Load (%)	Design Performance						Efficiency Standards		Remarks
		P _{IN} (W)	V _{OUT} (V)	I _{OUT} (A)	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 (%)	CoC v5 Tier 2 (%)	
115	100	38.800	12.005	2.999	36.006	92.80	92.29	87.40	88.30	PASS
	75	29.160	12.017	2.249	27.029	92.69				
	50	19.510	12.030	1.500	18.038	92.46				
	25	9.887	12.034	0.750	9.018	91.21				
	10	4.140	12.031	0.299	3.602	87.00			78.30	PASS
230	100	38.540	12.016	2.999	36.039	93.51	92.71	87.40	88.30	PASS
	75	28.990	12.029	2.249	27.056	93.33				
	50	19.440	12.037	1.500	18.051	92.85				
	25	9.900	12.039	0.750	9.024	91.15				
	10	4.163	12.035	0.300	3.604	86.58			78.30	PASS

10.3.3.4 Output: 15 V / 3.0 A

Input (VAC)	Load (%)	Design Performance						Efficiency Standards		Remarks
		P _{IN} (W)	V _{OUT} (V)	I _{OUT} (A)	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 (%)	CoC v5 Tier 2 (%)	
115	100	48.420	15.000	2.999	44.990	92.92	92.32	87.73	88.85	PASS
	75	36.430	15.019	2.249	33.780	92.73				
	50	24.390	15.032	1.500	22.540	92.41				
	25	12.352	15.035	0.750	11.268	91.22				
	10	5.168	15.029	0.299	4.500	87.07			78.85	PASS
230	100	48.020	15.018	2.999	45.042	93.80	93.07	87.73	88.85	PASS
	75	36.110	15.029	2.249	33.803	93.61				
	50	24.190	15.036	1.500	22.546	93.20				
	25	12.290	15.037	0.749	11.268	91.68				
	10	5.173	15.031	0.299	4.499	86.97			78.85	PASS

10.3.3.5 Output: 20 V / 3.25 A

Input (VAC)	Load (%)	Design Performance						Efficiency Standards		Remarks
		P _{IN} (W)	V _{OUT} (V)	I _{OUT} (A)	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 (%)	CoC v5 Tier 2 (%)	
115	100	70.090	20.040	3.249	65.120	92.91	92.37	88.00	89.00	PASS
	75	52.640	20.049	2.436	48.850	92.80				
	50	35.240	20.055	1.624	32.570	92.42				
	25	17.820	20.053	0.812	16.279	91.35				
	10	7.429	20.049	0.324	6.498	87.47			79.00	PASS
230	100	69.220	20.040	3.249	65.110	94.06	93.43	88.00	89.00	PASS
	75	52.030	20.046	2.436	48.840	93.87				
	50	34.830	20.047	1.624	32.560	93.48				
	25	17.630	20.045	0.812	16.271	92.29				
	10	7.360	20.042	0.324	6.495	88.25			79.00	PASS



10.4 Efficiency Across Line at 100% Load (On Board)

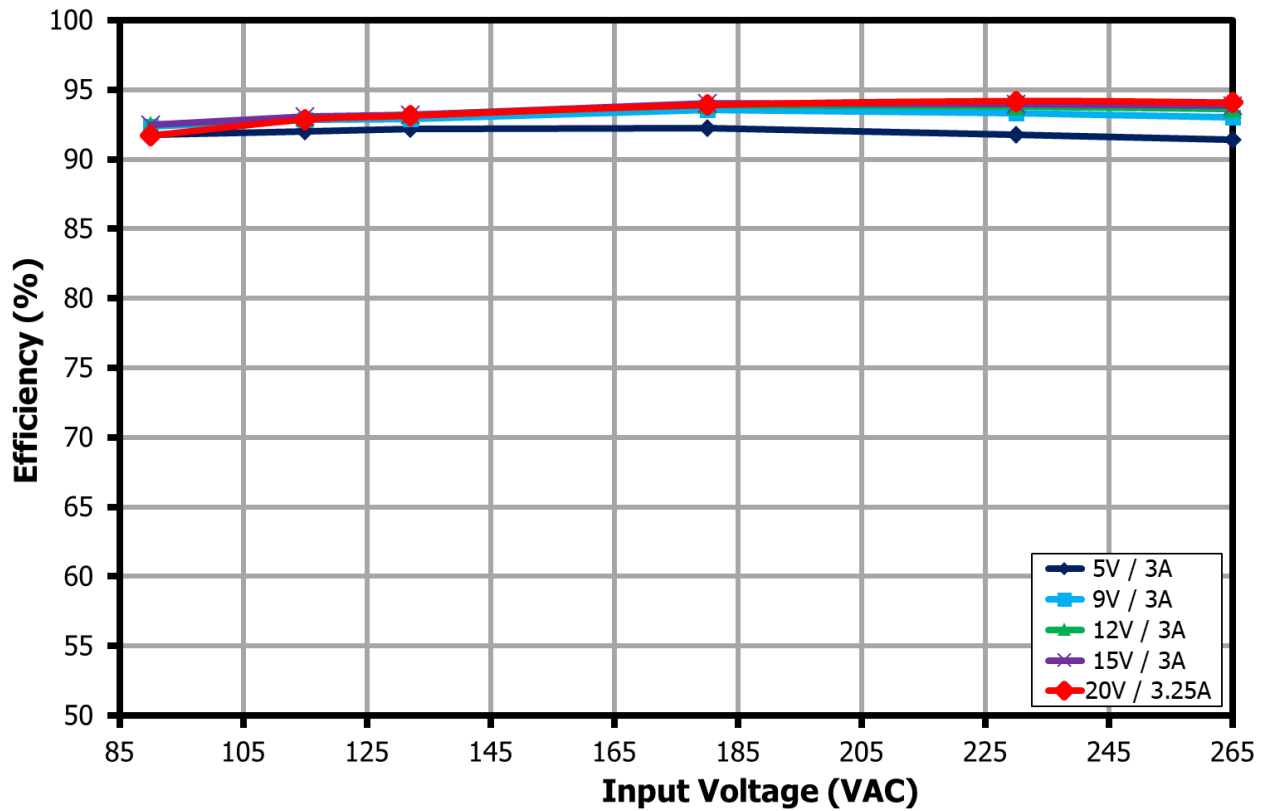


Figure 13 – Full Load Efficiency vs. Input Line for 5 V, 9 V, 12 V, 15 V, and 20 V Output, Room Temperature.

10.5 Efficiency Across Load (On Board)

10.5.1 Output: 5 V / 3.0 A

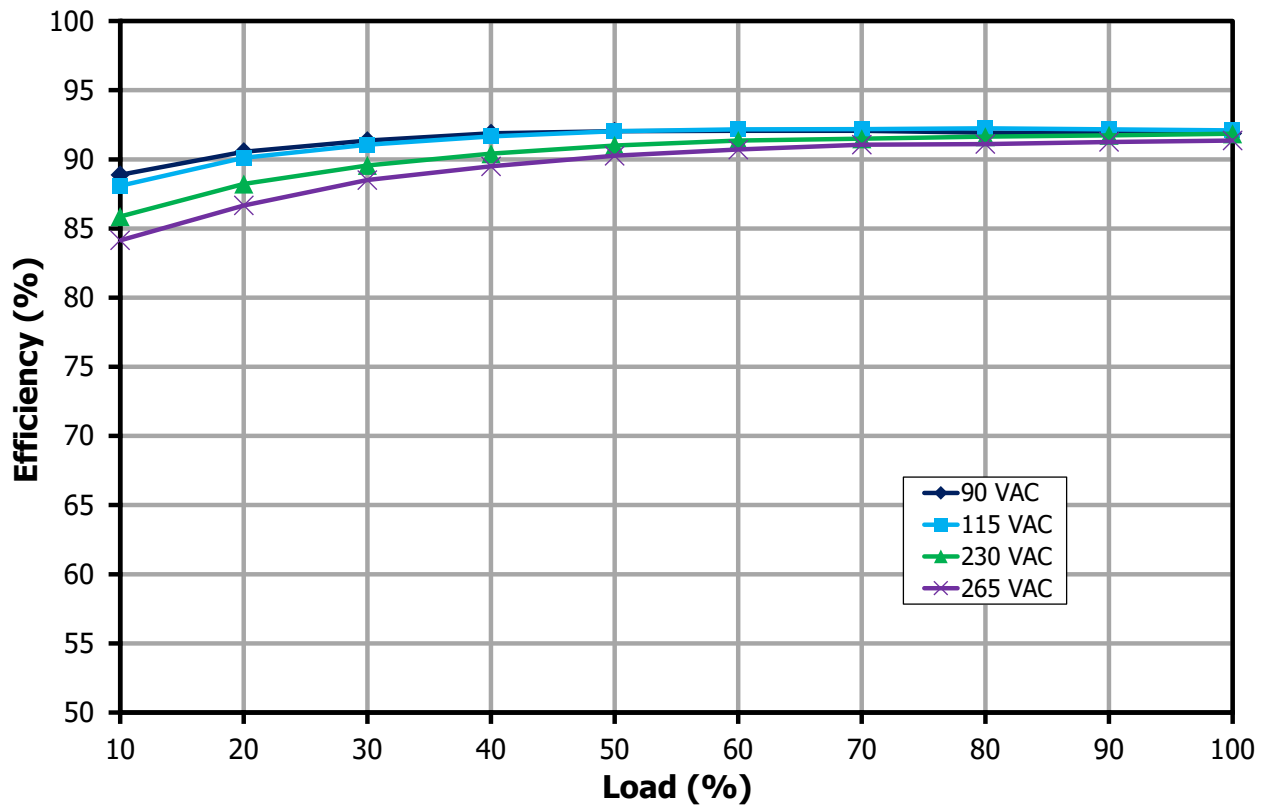


Figure 14 – Efficiency vs. Load for 5 V Output, Room Temperature.

10.5.2 Output: 9 V / 3.0 A

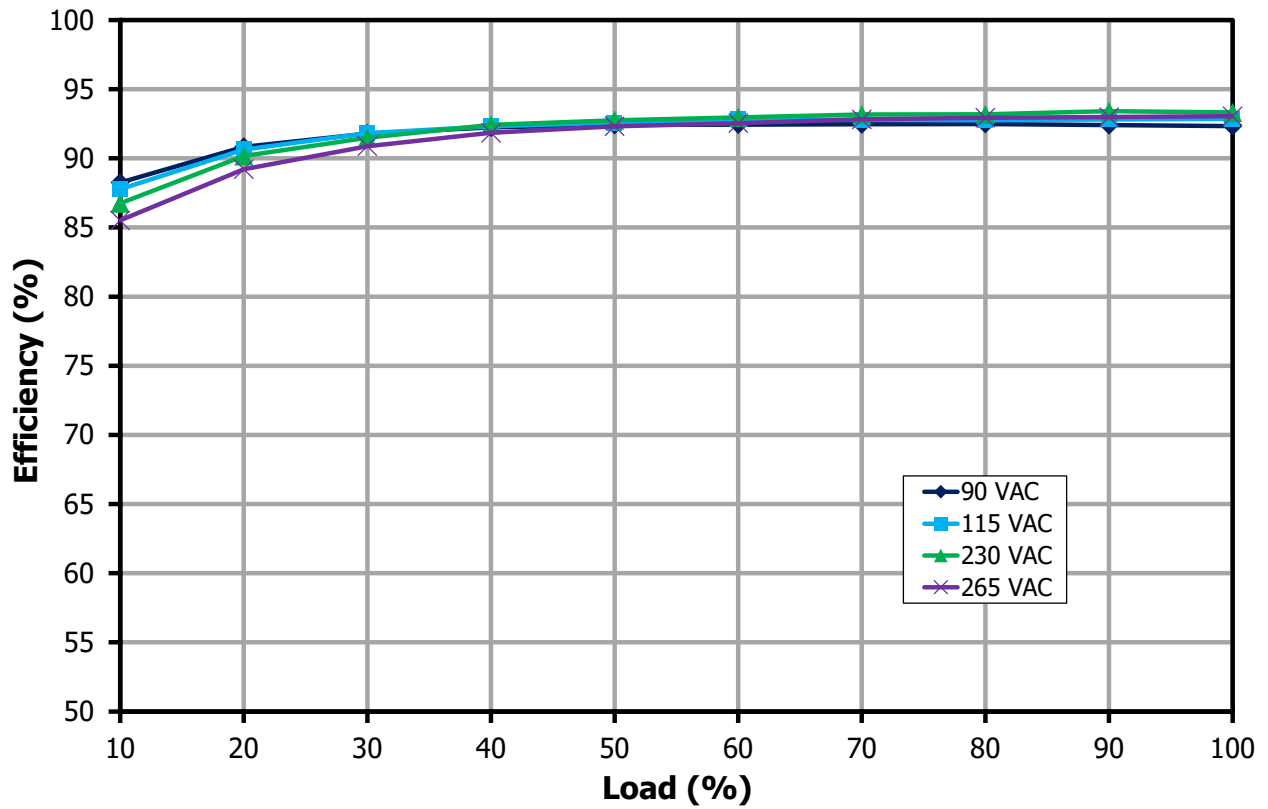


Figure 15 – Efficiency vs. Load for 9 V Output, Room Temperature.

10.5.3 Output: 12 V / 3.0 A

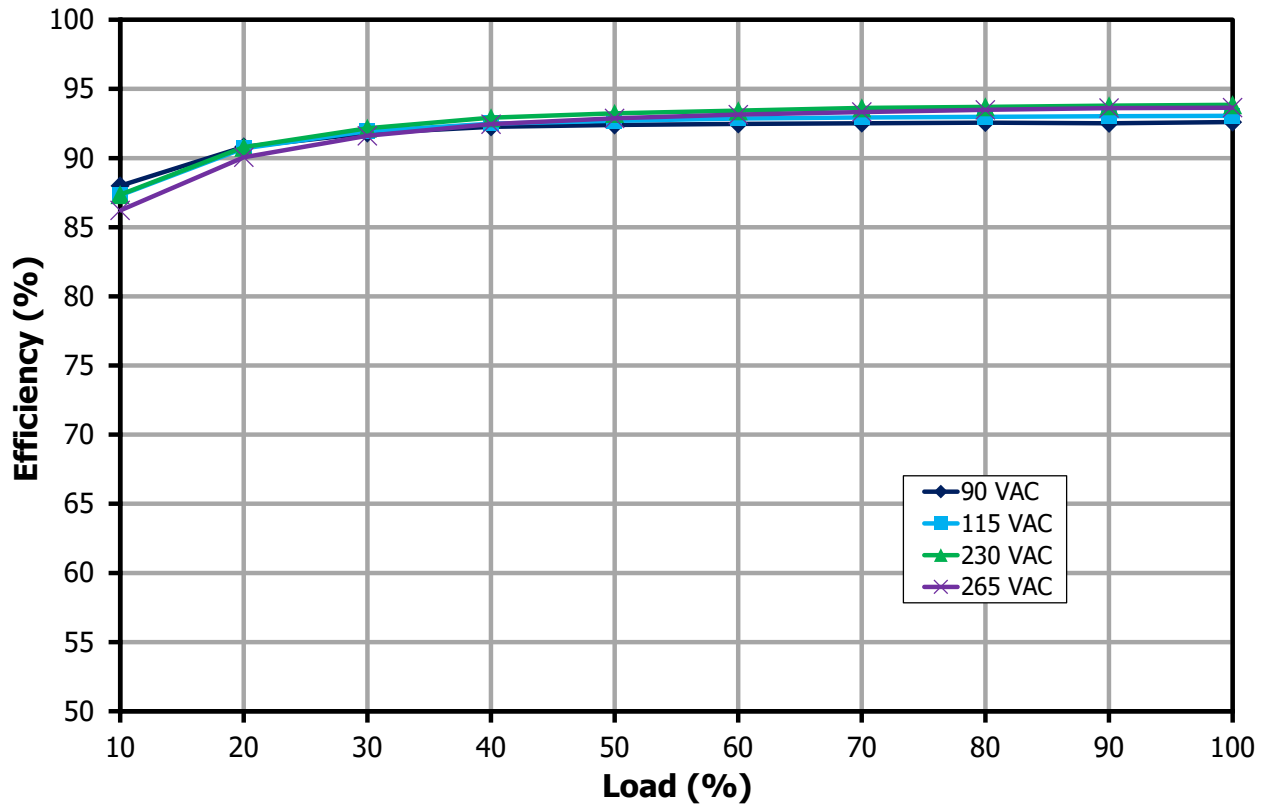


Figure 16 – Efficiency vs. Load for 12 V Output, Room Temperature.

10.5.4 Output: 15 V / 3.0 A

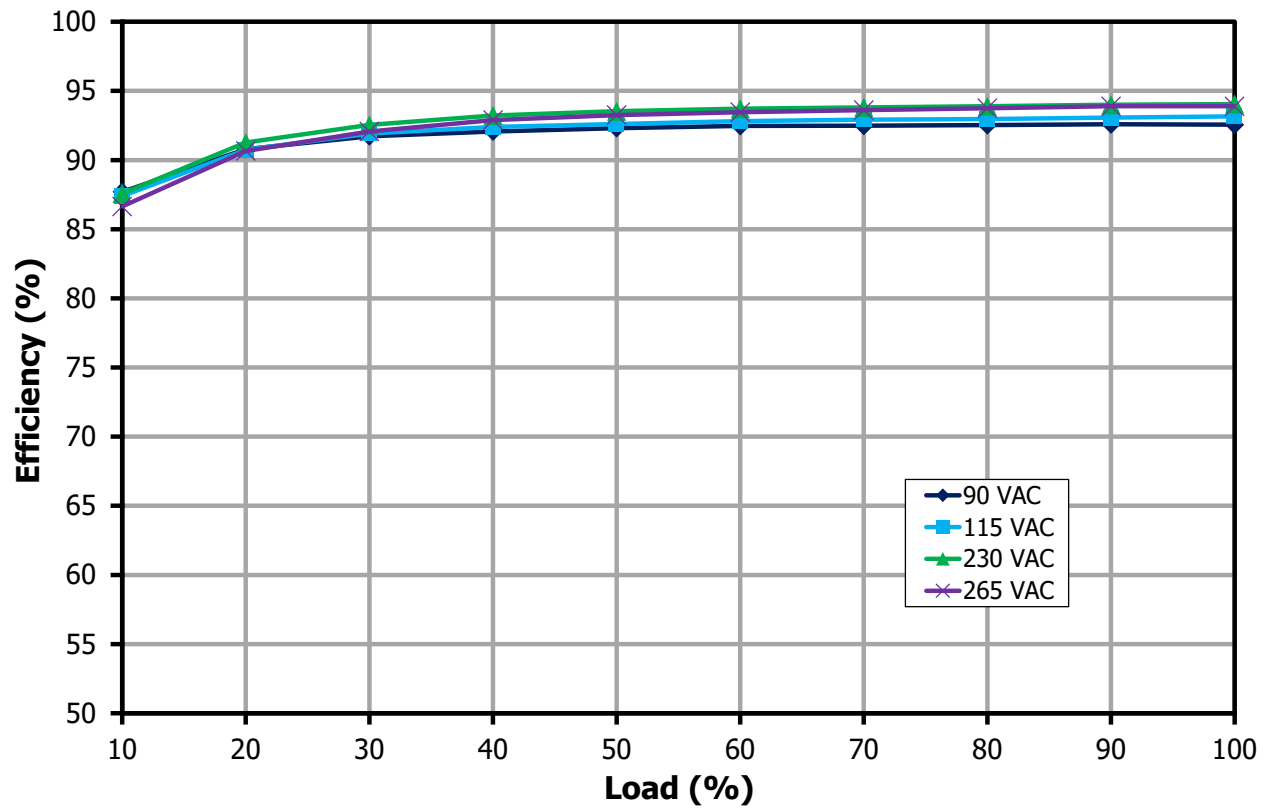


Figure 17 – Efficiency vs. Load for 15 V Output, Room Temperature.

10.5.5 Output: 20 V / 3.25 A

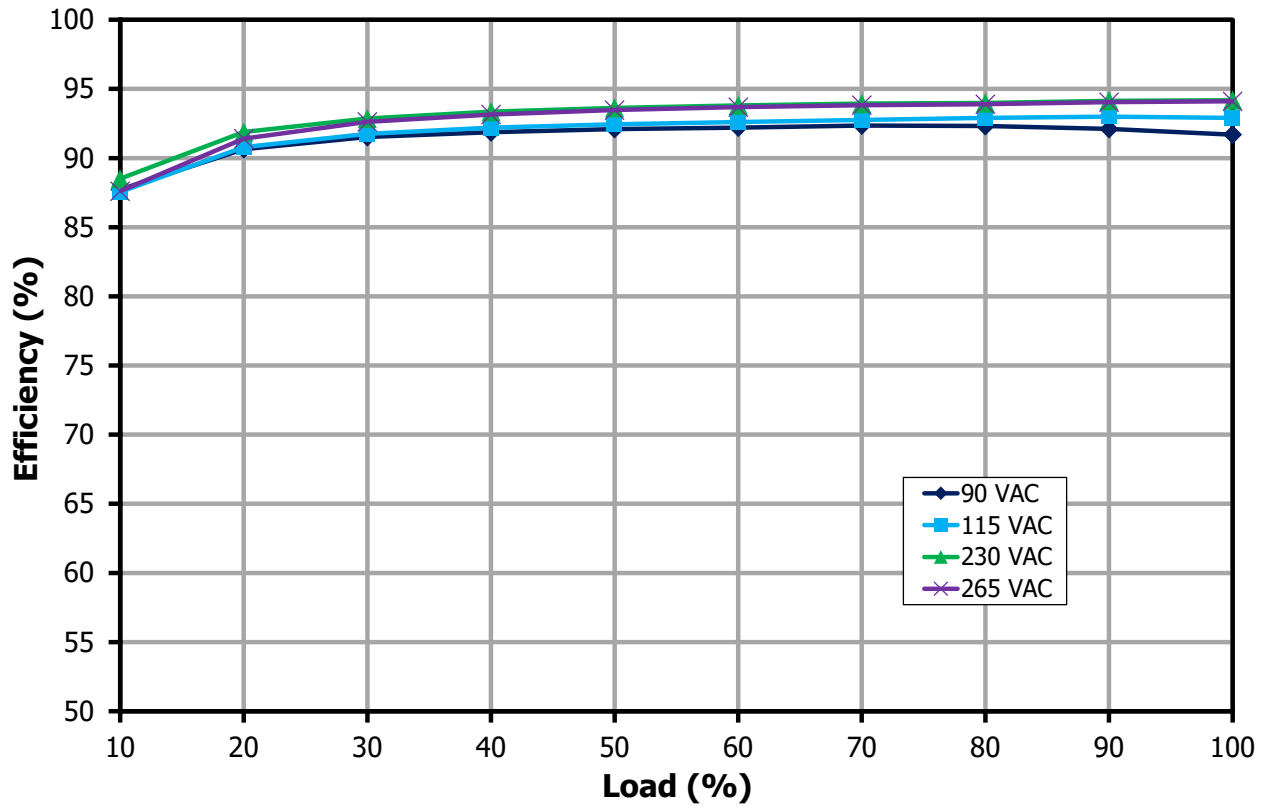


Figure 18 – Efficiency vs. Load for 20 V Output, Room Temperature.

10.6 Load Regulation (On Board)

10.6.1 Output: 5 V / 3.0 A

Cable Drop Compensation (CDC) is set to 150 mV for 5 V and 9 V fixed supply PDOs.

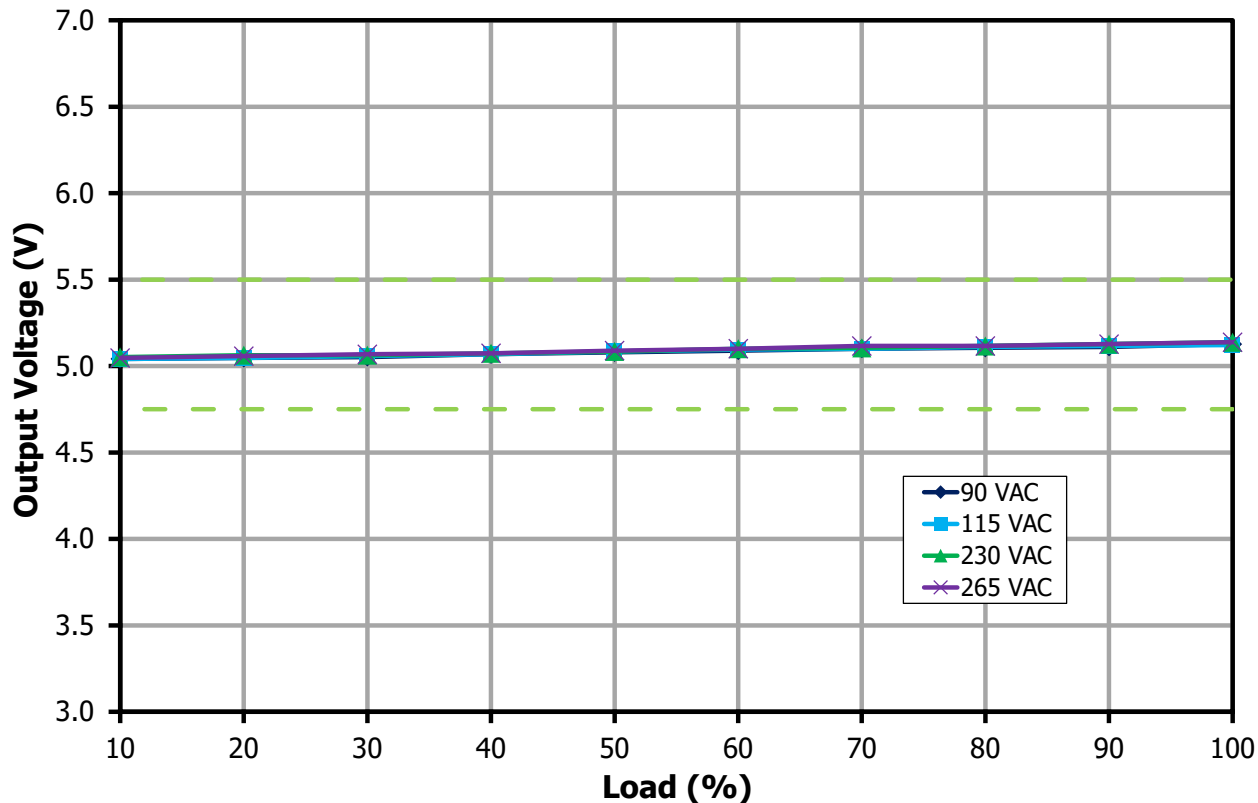


Figure 19 – Output Voltage vs. Output Load for 5 V Output, Room Temperature.

Note: USB PD Specification defines vSafe5V (4.75 V to 5.5 V, measured on-board) as the allowable VBUS Voltage range at 5 V operation

10.6.2 Output: 9 V / 3.0 A

Cable Drop Compensation (CDC) is set to 150 mV for 5 V and 9 V fixed supply PDOs.

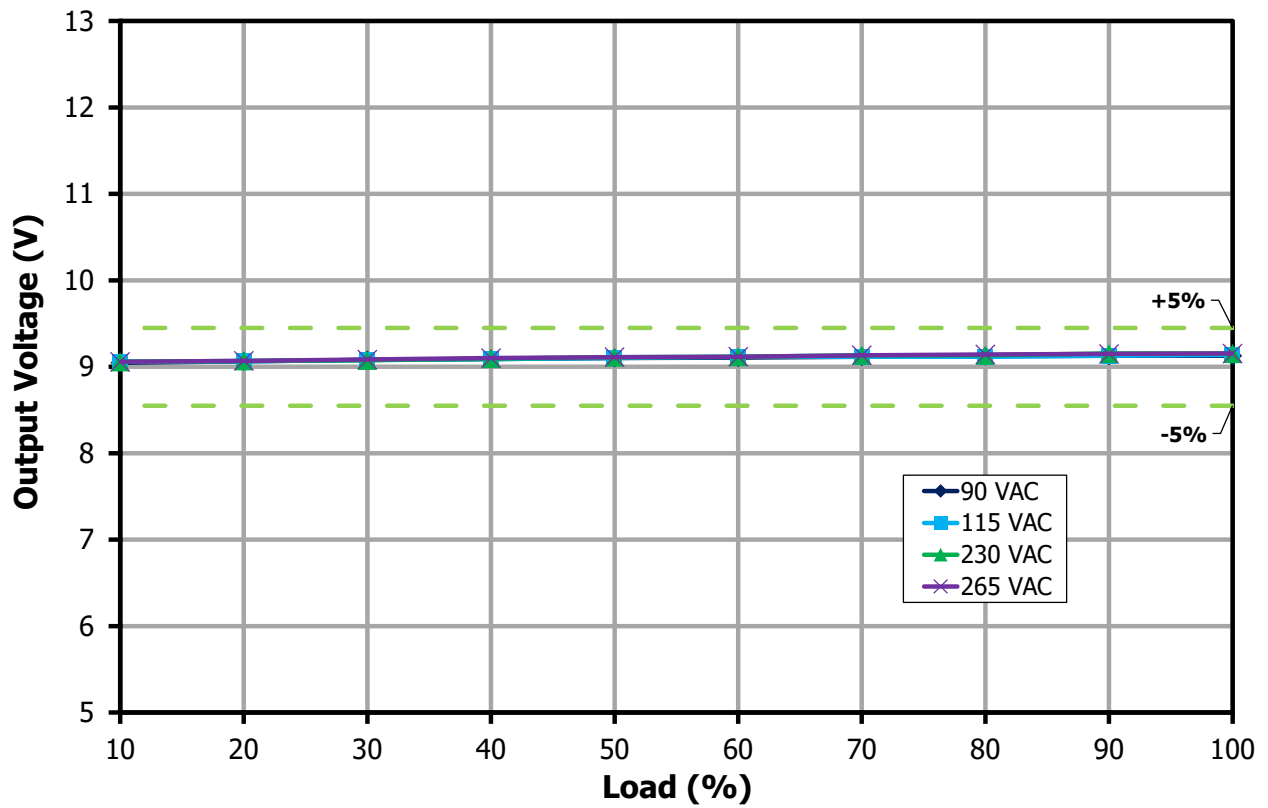


Figure 20 – Output Voltage vs. Output Load for 9 V Output, Room Temperature.

10.6.3 Output: 12 V / 3.0 A

Cable Drop Compensation (CDC) is disabled for 12 V, 15 V, and 20 V fixed supply PDOs.

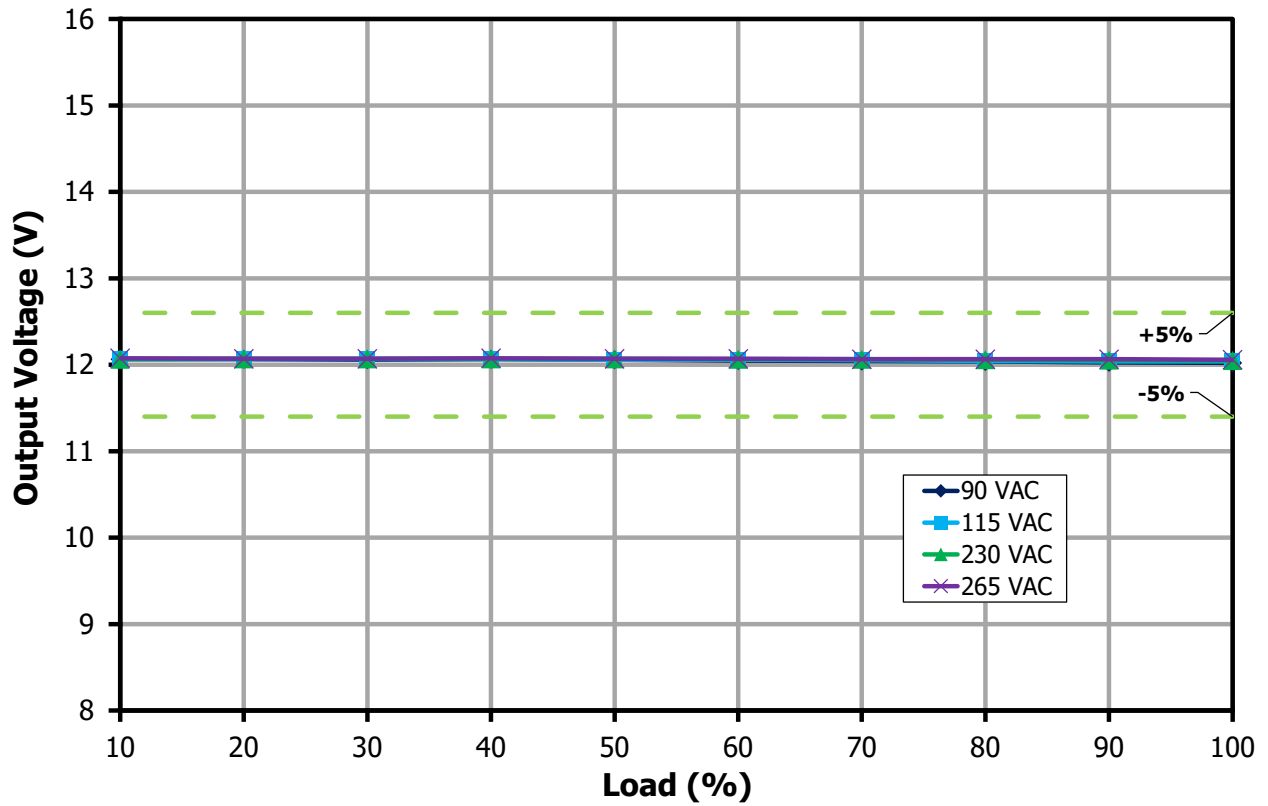


Figure 21 – Output Voltage vs. Output Load for 12 V Output, Room Temperature.

10.6.4 Output: 15 V / 3.0 A

Cable Drop Compensation (CDC) is disabled for 12 V, 15 V, and 20 V fixed supply PDOs.

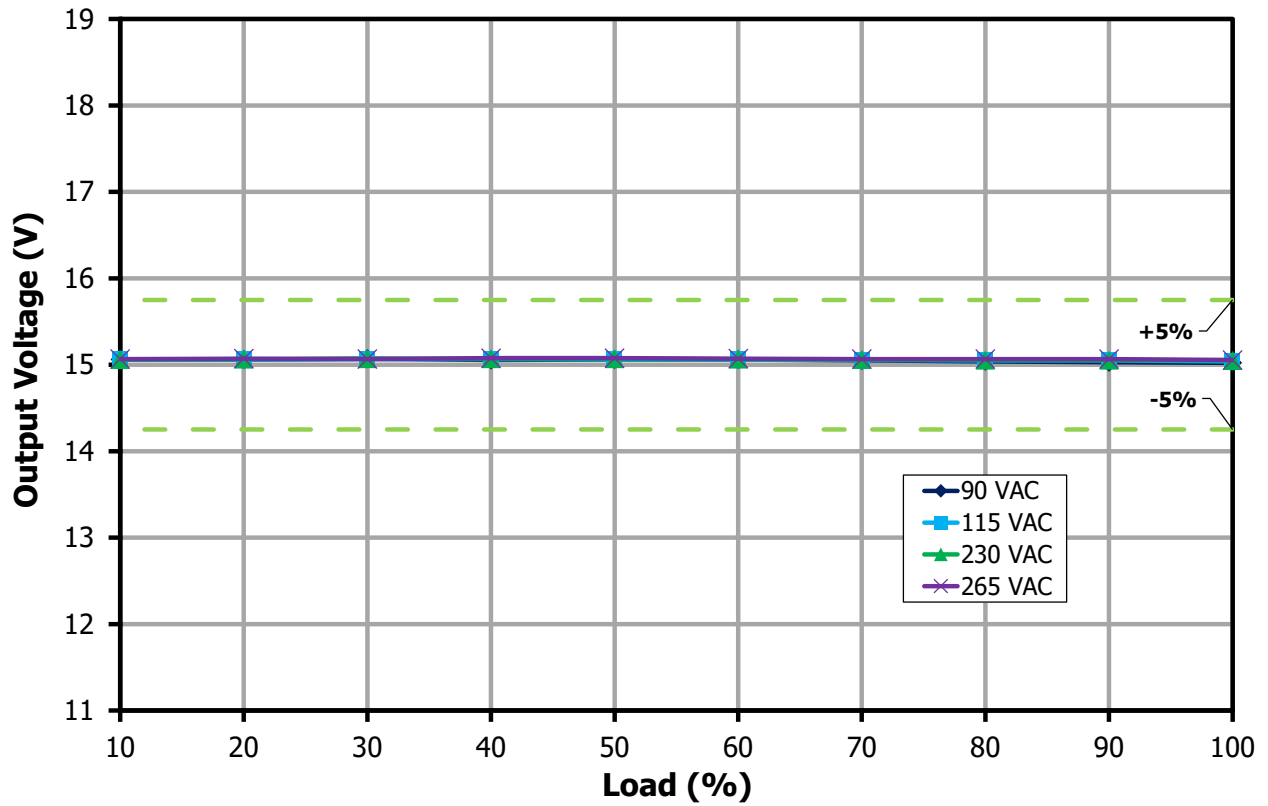


Figure 22 – Output Voltage vs. Output Load for 15 V Output, Room Temperature.

10.6.5 Output: 20 V / 3.25 A

Cable Drop Compensation (CDC) is disabled for 12 V, 15 V, and 20 V fixed supply PDOs.

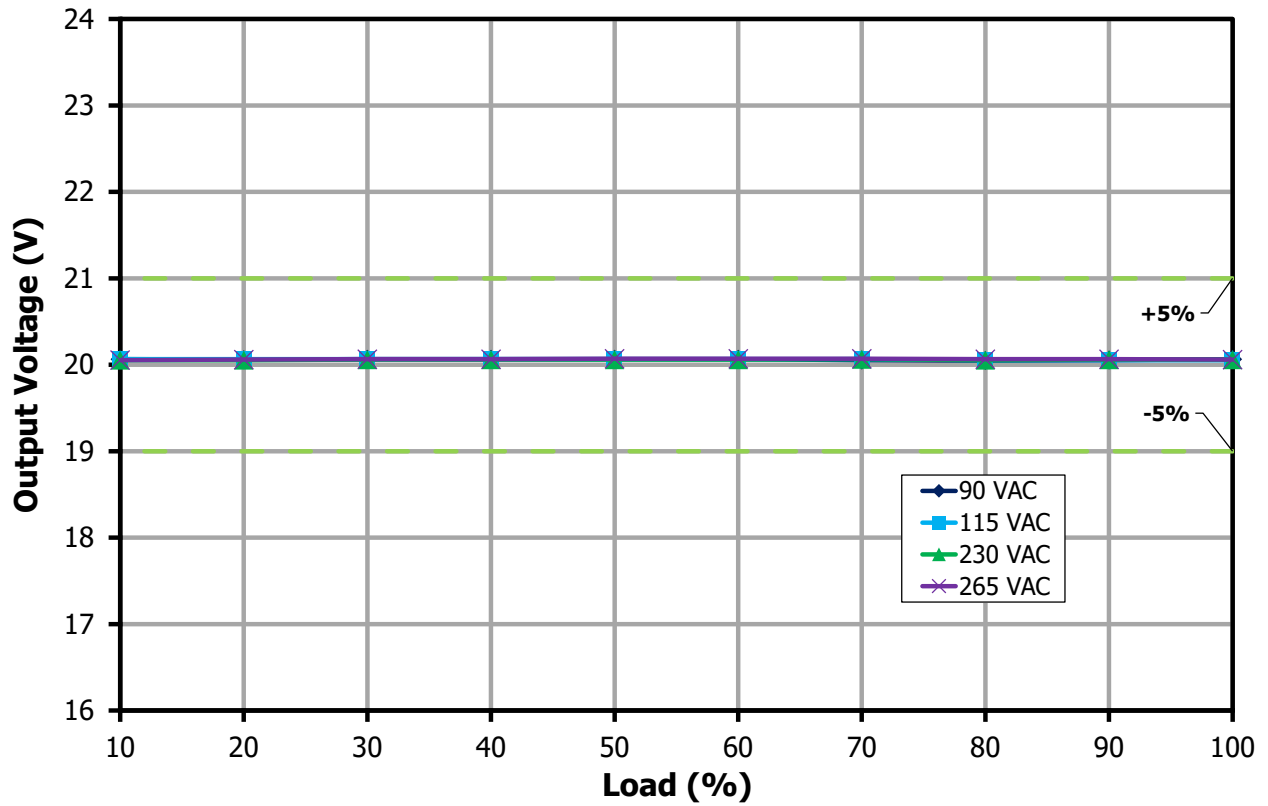


Figure 23 – Output Voltage vs. Output Load for 20 V Output, Room Temperature.

10.7 Line Regulation (On Board)

10.7.1 Output: 5 V / 3.0 A

Cable Drop Compensation (CDC) is set to 150 mV for 5 V and 9 V fixed supply PDOs.

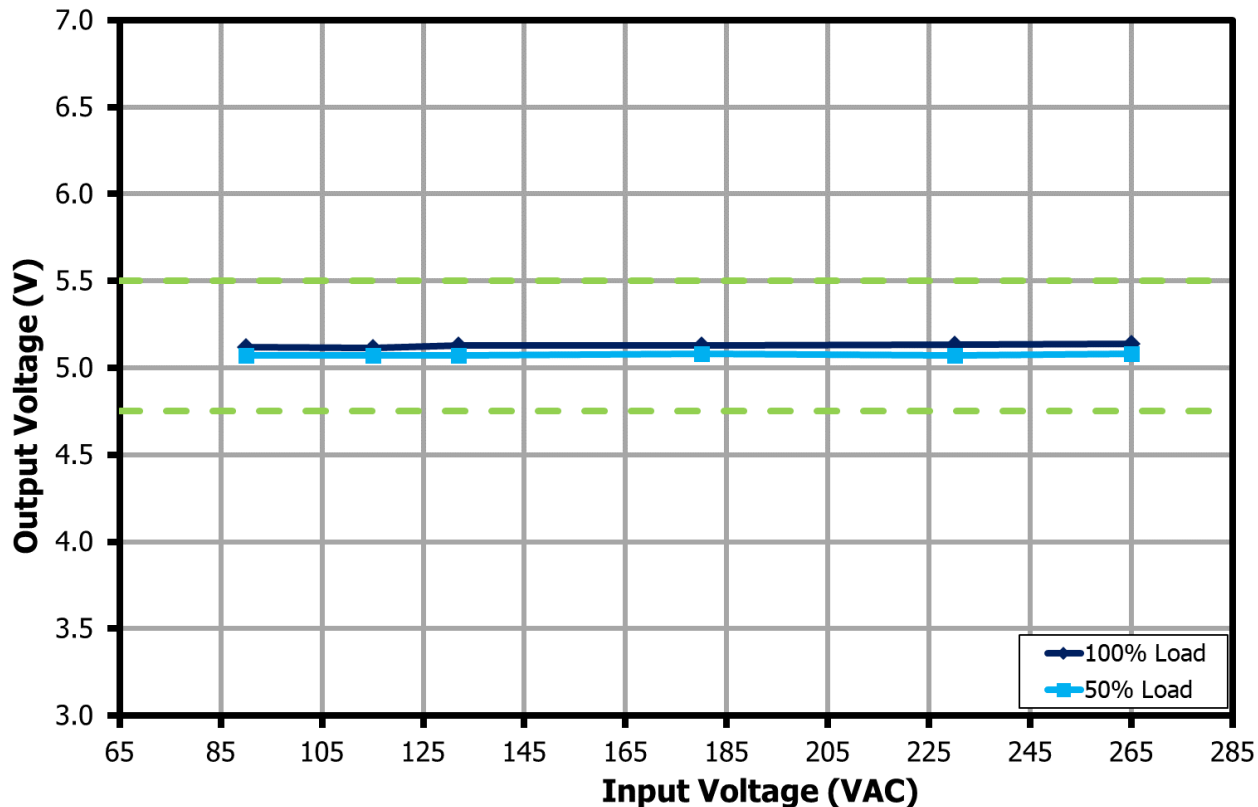


Figure 24 – Output Voltage vs. Input Line Voltage for 5 V Output, Room Temperature.

Note: USB PD Specification defines vSafe5V (4.75 V to 5.5 V, measured on-board) as the allowable VBUS Voltage range at 5 V operation

10.7.2 Output: 9 V / 3.0 A

Cable Drop Compensation (CDC) is set to 150 mV for 5 V and 9 V fixed supply PDOs.

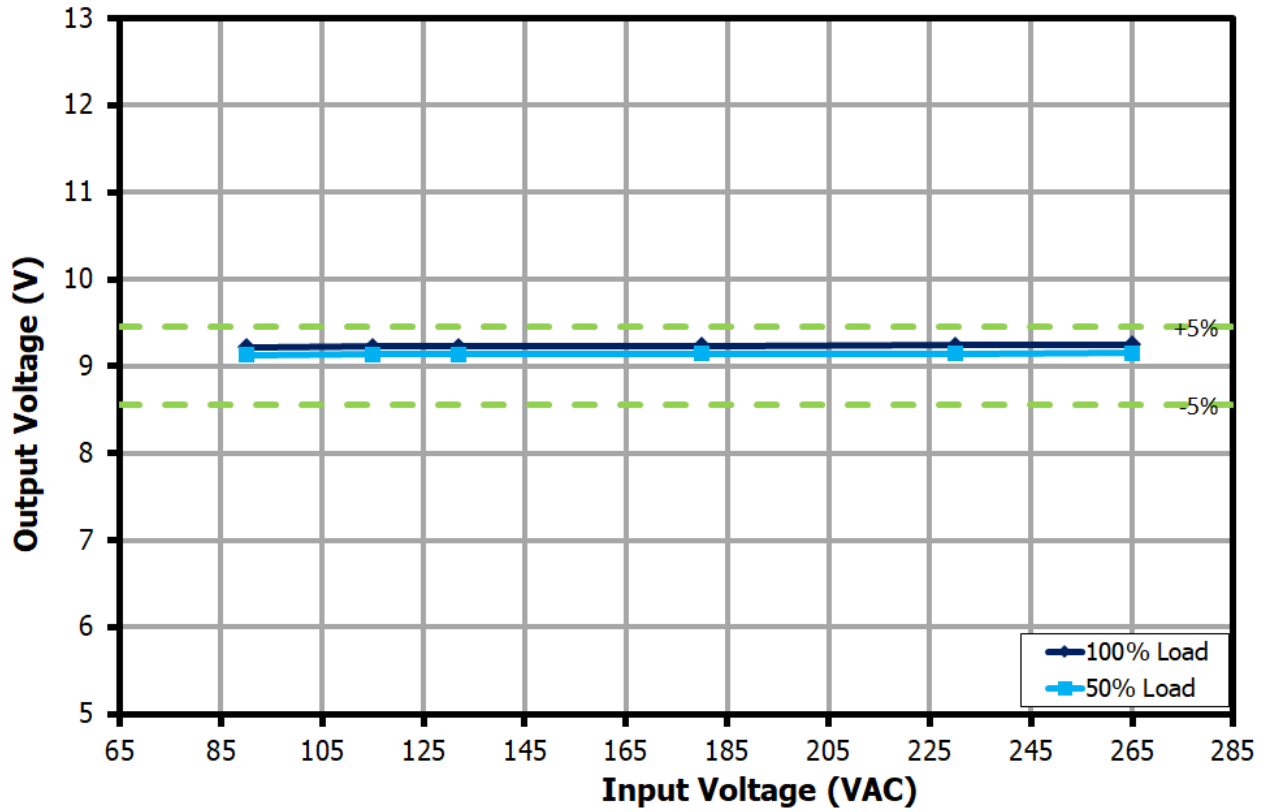


Figure 25 – Output Voltage vs. Input Line Voltage for 9 V Output, Room Temperature.

10.7.3 Output: 12 V / 3.0 A

Cable Drop Compensation (CDC) is disabled for 12 V, 15 V, and 20 V fixed supply PDOs.

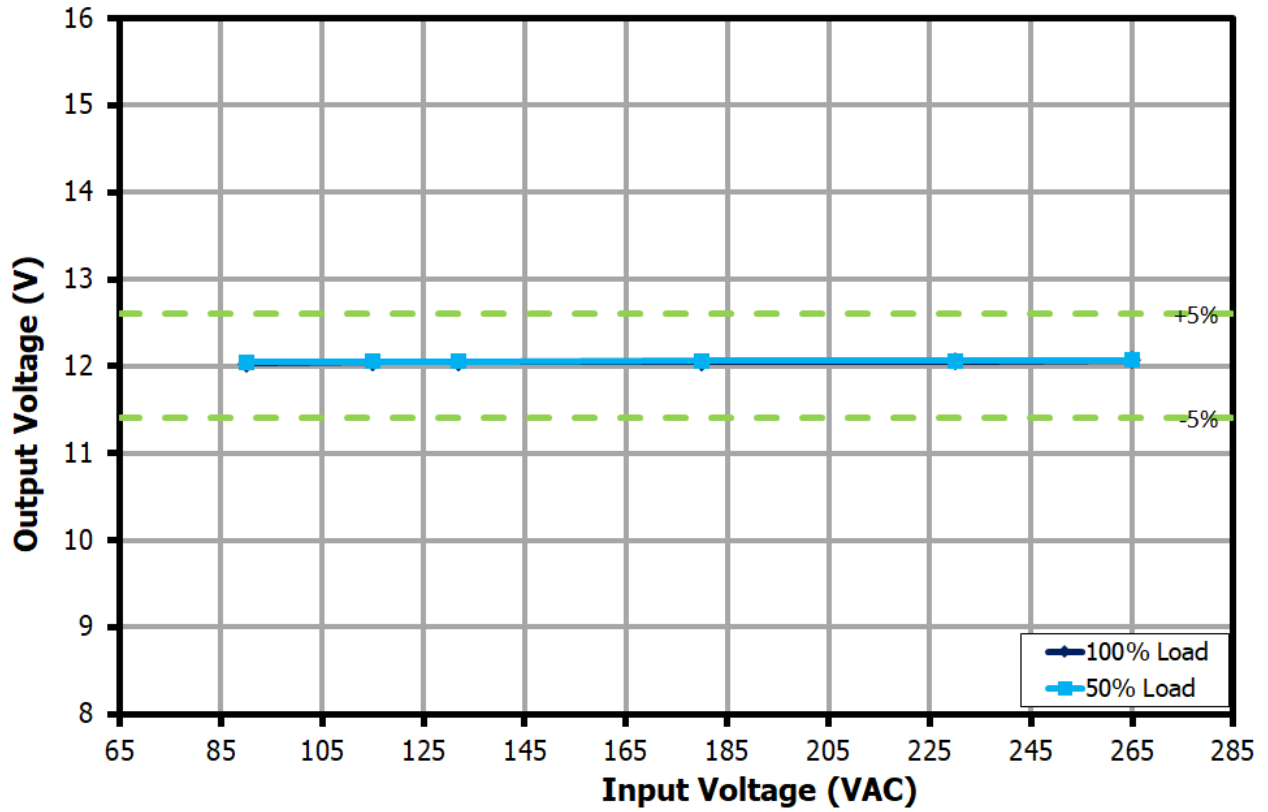


Figure 26 – Output Voltage vs. Input Line Voltage for 12 V Output, Room Temperature.

10.7.4 Output: 15 V / 3.0 A

Cable Drop Compensation (CDC) is disabled for 12 V, 15 V, and 20 V fixed supply PDOs.

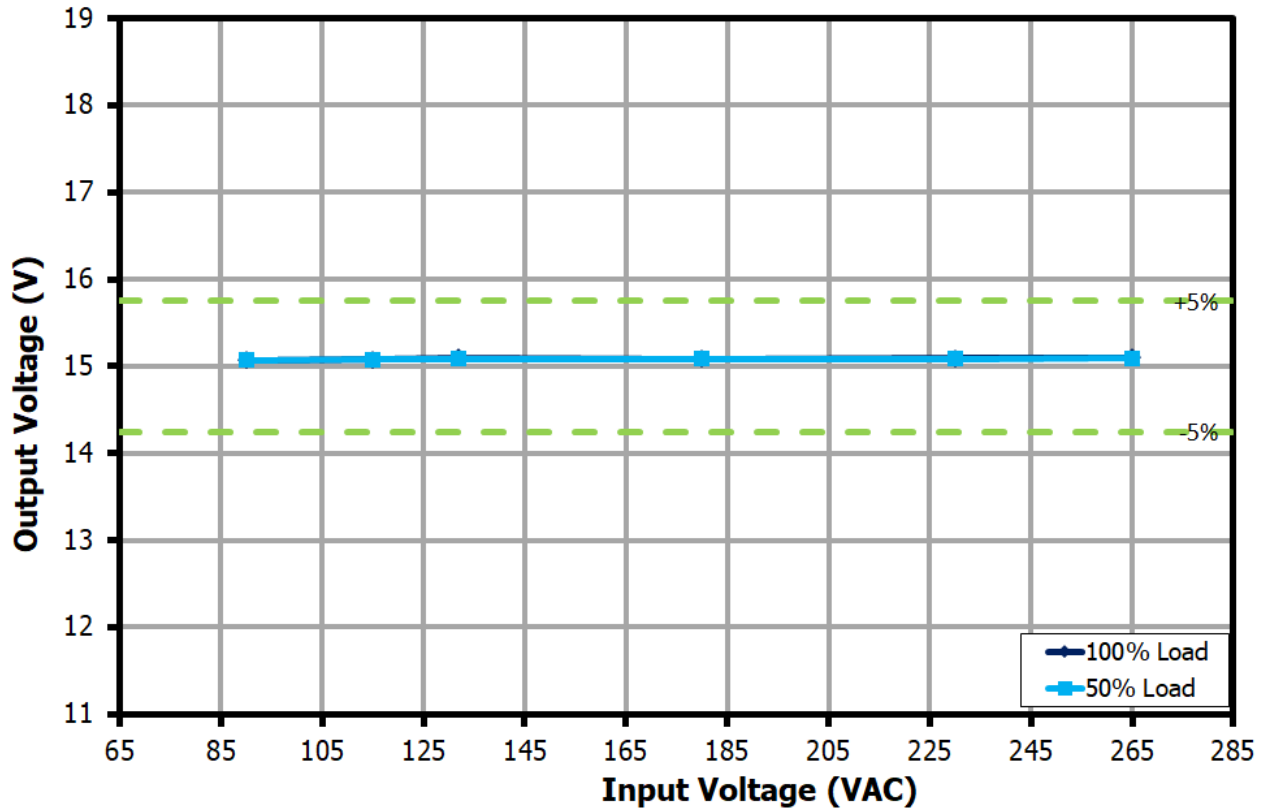


Figure 27 – Output Voltage vs. Input Line Voltage for 15 V Output, Room Temperature.

10.7.5 Output: 20 V / 3.25 A

Cable Drop Compensation (CDC) is disabled for 12 V, 15 V, and 20 V fixed supply PDOs.

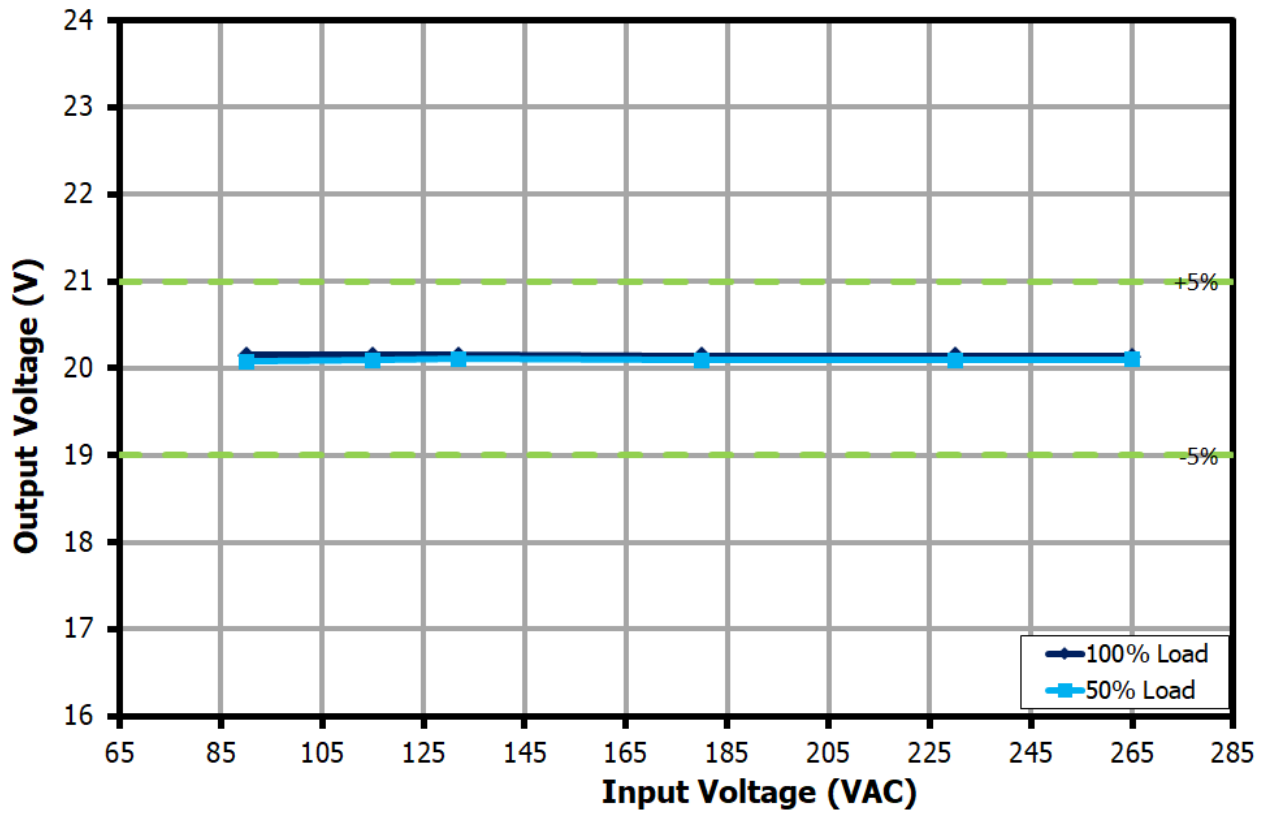


Figure 28 – Output Voltage vs. Input Line Voltage for 20 V Output, Room Temperature.

11 Thermal Performance

11.1 Thermal Performance in Open Case, Room Temperature

Note: 1. Open case thermal images are taken at room temperature ambient with the unit inside a closed acrylic box and 1-hour soak per condition.
2. For enclosed adapter application, this design is recommended to have a metallic heat spreader and suitable thermally conductive insulator pads to ensure low temperature of the bridge rectifiers and InnoSwitch4-Pro IC. The performance data below is for open case operation and does not use heat spreader for cooling.

11.1.1 Output: 20 V / 3.25 A (90 VAC)

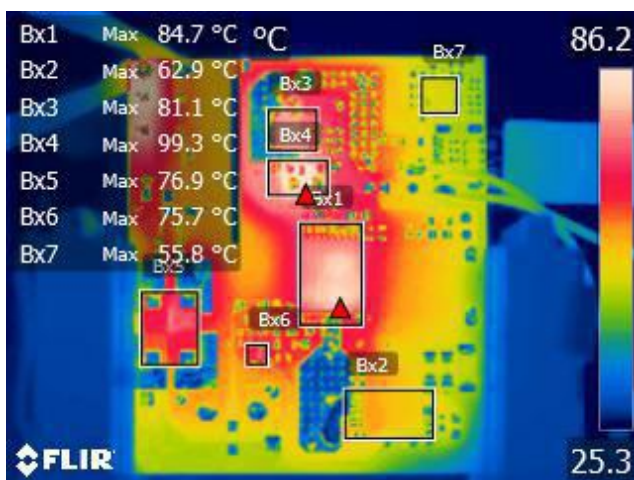


Figure 29 – Bottom Thermal Image, $T_{AMB} = 27.9$ °C.

Bx1: InnoSwitch4-Pro = 84.7 °C.
Bx2: ClampZero = 62.9 °C.
Bx3: SR FET = 81.1 °C.
Bx4: SR FET Snubber = 99.3 °C.
Bx5: Bridge Diode = 76.9 °C.
Bx6: Primary Bias BJT = 75.7 °C.
Bx7: PD Controller = 55.8 °C.



Figure 30 – Top Thermal Image, $T_{AMB} = 27.9$ °C.

Bx1: Transformer Core = 77.3 °C.
Bx2: Transformer Wire = 82.7 °C.
Bx3: Inrush Thermistor = 103.9 °C.
Bx4: Bulk Cap 1 = 62 °C.
E11: Output Cap 1 = 68.9 °C.
E12: Bulk Cap 2 = 50.6 °C.

11.1.2 Output: 20 V / 3.25 A (265 VAC)

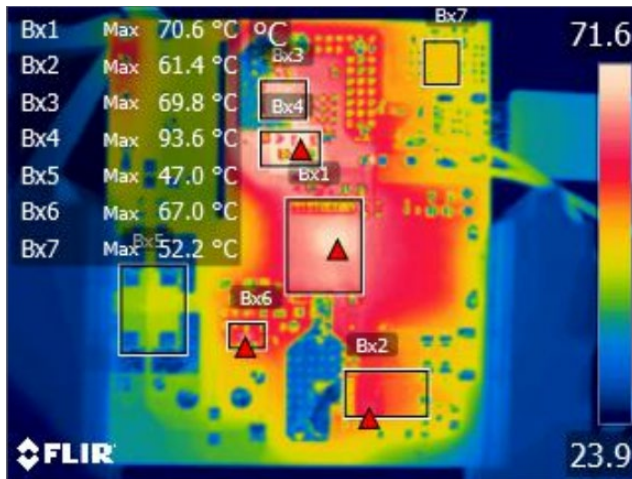


Figure 31 – Bottom Thermal Image, $T_{AMB} = 27.5$ °C.

Bx1: InnoSwitch4-Pro = 70.6 °C.
 Bx2: ClampZero = 61.4 °C.
 Bx3: SR FET = 69.8 °C.
 Bx4: SR FET Snubber = 93.6 °C.
 Bx5: Bridge Diode = 47 °C.
 Bx6: Primary Bias BJT = 67 °C.
 Bx7: PD Controller = 52.2 °C.

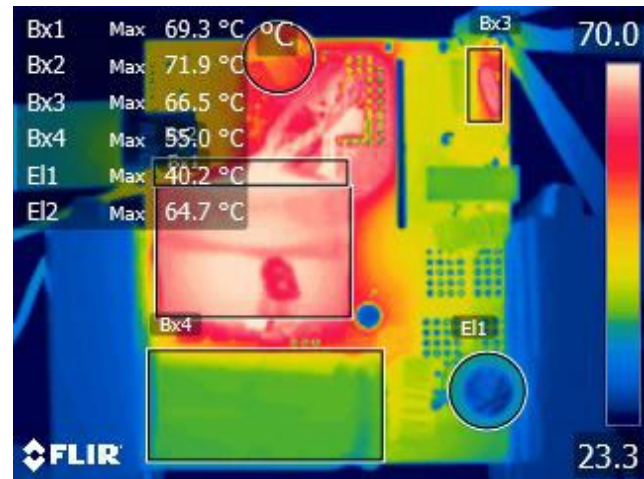


Figure 32 – Top Thermal Image, $T_{AMB} = 27.4$ °C.

Bx1: Transformer Core = 69.3 °C.
 Bx2: Transformer Wire = 71.9 °C.
 Bx3: Inrush Thermistor = 66.5 °C.
 Bx4: Bulk Cap 1 = 55.0 °C.
 E1: Bulk Cap 2 = 40.2 °C.
 E2: Output Cap 1 = 64.7 °C.

12 Waveforms

Note: 1. Output voltage captured at the end of 100 mΩ cable unless otherwise specified.
2. Waveforms taken at room temperature ambient (approximately 25 °C).

12.1 Start-up Waveforms

12.1.1 Input Voltage, Output Voltage and Current



Figure 33 – Input Voltage, Output Voltage and Current.
90 VAC, 5.0 V, 3 A (E-load CC Mode).
 $V_{BUS_IN} = 5.143$ V Steady-State.
 $t_{output_delay} = 780$ ms
CH1: IOUT, 1 A / div.
CH2: V_{IN_AC} , 100 V / div.
CH3: V_{BUS_OUT} , 1 V / div.
CH4: V_{BUS_IN} , 1 V / div.
Time: 100 ms / div.



Figure 34 – Input Voltage, Output Voltage and Current.
265 VAC, 5.0 V, 3 A (E-load CC Mode).
 $V_{BUS_IN} = 5.159$ V Steady-State.
 $t_{output_delay} = 769$ ms
CH1: IOUT, 1 A / div.
CH2: V_{IN_AC} , 100 V / div.
CH3: V_{BUS_OUT} , 1 V / div.
CH4: V_{BUS_IN} , 1 V / div.
Time: 100 ms / div.

12.1.2 Primary Drain Voltage and Current
 Primary Drain Voltage, Drain Current, and output voltage before the bus switch were captured.

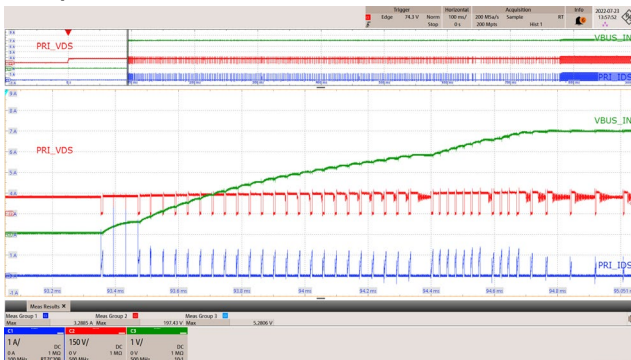


Figure 35 – Primary Drain Voltage and Current.
 90 VAC, 5.0 V, 3 A (E-load CR Mode, 1.63 Ω at the End of 100 mΩ Cable).
 $V_{DS_PRI} = 197.43$ V Maximum.
 CH1: I_{DS_PRI} , 1 A / div.
 CH2: V_{DS_PRI} , 150 V / div.
 CH3: V_{BUS_IN} , 1 V / div.
 Time: 100 ms / div. (200 μs / div. Zoom).



Figure 36 – Primary Drain Voltage and Current.
 265 VAC, 5.0 V, 3 A (E-load CR Mode, 1.63 Ω at the End of 100 mΩ Cable).
 $V_{DS_PRI} = 452.37$ V Maximum.
 CH1: I_{DS_PRI} , 1 A / div.
 CH2: V_{DS_PRI} , 150 V / div.
 CH3: V_{BUS_IN} , 1 V / div.
 Time: 100 ms / div. (200 μs / div. Zoom).

12.1.3 SR FET Drain Voltage and Gate Voltage

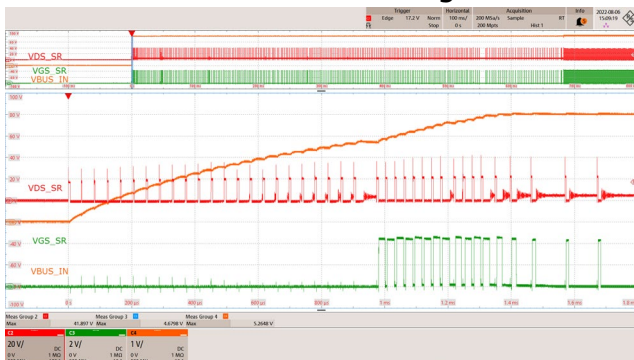


Figure 37 – SR FET Drain Voltage and Gate Voltage
 90 VAC, 5.0 V, 3 A (CR Mode, 1.61 Ω at the End of 100 mΩ Cable).
 $V_{DS_SR} = 41.897$ V Maximum.
 CH2: V_{DS_SR} , 20 V / div.
 CH3: V_{GS_SR} , 2 V / div.
 CH4: V_{BUS_IN} , 1 V / div.
 Time: 100 ms / div. (200 μs / div. Zoom).

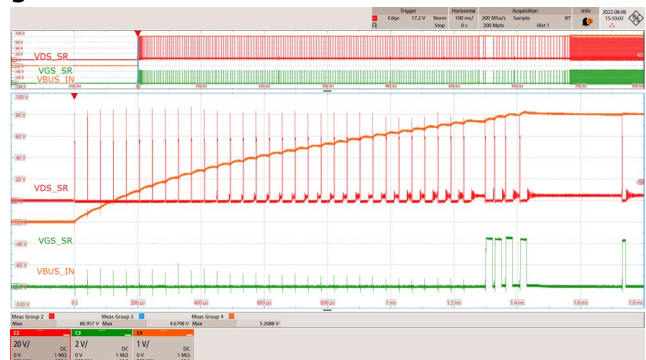


Figure 38 – SR FET Drain Voltage and Gate Voltage
 265 VAC, 5.0 V, 3 A (CR Mode, 1.61 Ω at the End of 100 mΩ Cable).
 $V_{DS_SR} = 86.957$ V Maximum.
 CH2: V_{DS_SR} , 20 V / div.
 CH3: V_{GS_SR} , 2 V / div.
 CH4: V_{BUS_IN} , 1 V / div.
 Time: 100 ms / div. (200 μs / div. Zoom).

12.2 Primary Drain Voltage and Current (Steady-State)

12.2.1 Output: 5 V / 3 A

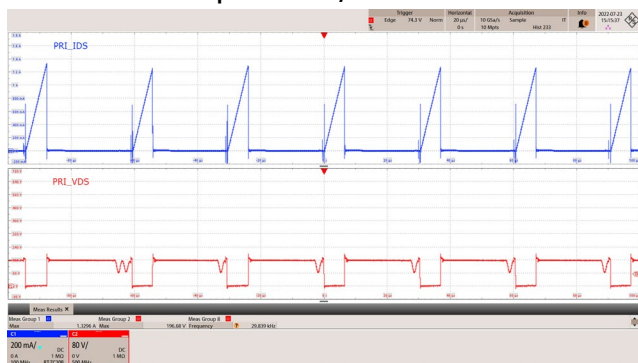


Figure 39 – Primary Drain Voltage and Current.
 90 VAC, 5.0 V, 3 A Load.
 $V_{DS_PRI} = 196.68$ V Maximum.
 CH1: I_{DS_PRI} , 200 mA / div.
 CH2: V_{DS_PRI} , 80 V / div.
 Time: 20 μ s / div.

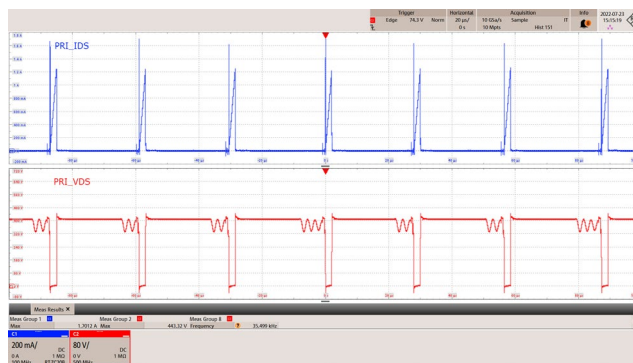


Figure 40 – Primary Drain Voltage and Current.
 265 VAC, 5.0 V, 3 A Load.
 $V_{DS_PRI} = 443.32$ V Maximum.
 CH1: I_{DS_PRI} , 200 mA / div.
 CH2: V_{DS_PRI} , 80 V / div.
 Time: 20 μ s / div.

12.2.2 Output: 9 V / 3 A

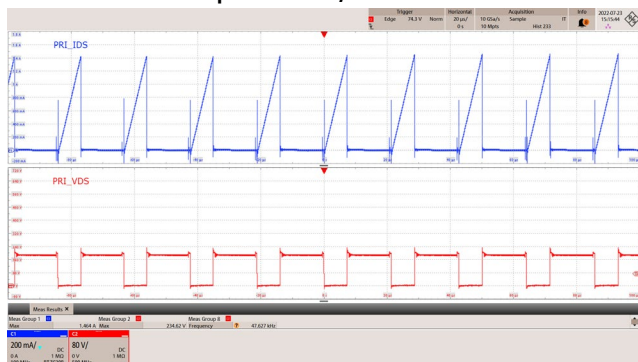


Figure 41 – Primary Drain Voltage and Current.
 90 VAC, 9.0 V, 3 A Load.
 $V_{DS_PRI} = 234.62$ V Maximum.
 CH1: I_{DS_PRI} , 200 mA / div.
 CH2: V_{DS_PRI} , 80 V / div.
 Time: 20 μ s / div.

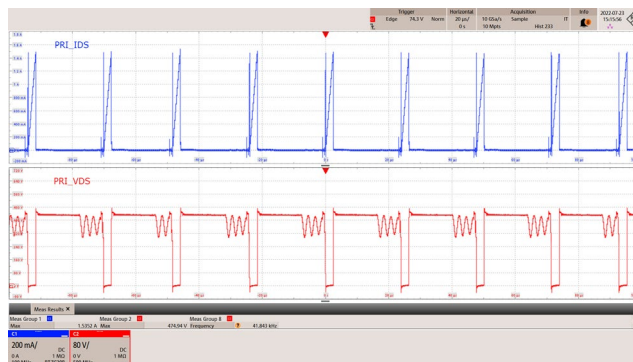


Figure 42 – Primary Drain Voltage and Current.
 265 VAC, 9.0 V, 3 A Load.
 $V_{DS_PRI} = 474.94$ V Maximum.
 CH1: I_{DS_PRI} , 200 mA / div.
 CH2: V_{DS_PRI} , 80 V / div.
 Time: 20 μ s / div.

12.2.3 Output: 12 V / 3 A

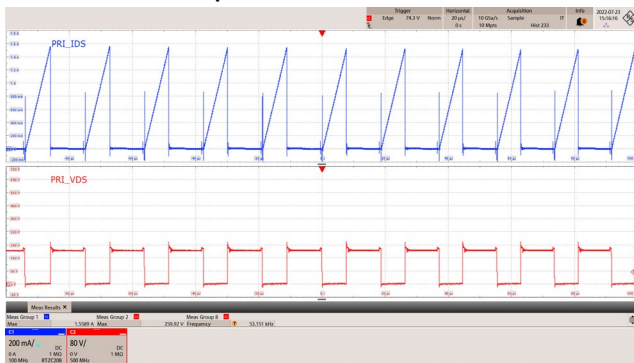


Figure 43 – Primary Drain Voltage and Current.
 90 VAC, 12.0 V, 3 A Load.
 $V_{DS_PRI} = 259.92V$ Maximum.
 CH1: I_{DS_PRI} , 200 mA / div.
 CH2: V_{DS_PRI} , 80 V / div.
 Time: 20 μs / div.

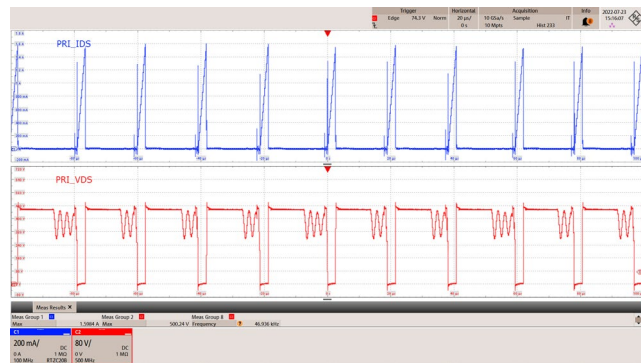


Figure 44 – Primary Drain Voltage and Current.
 265 VAC, 12.0 V, 3 A Load.
 $V_{DS_PRI} = 500.24 V$ Maximum.
 CH1: I_{DS_PRI} , 200 mA / div.
 CH2: V_{DS_PRI} , 80 V / div.
 Time: 20 μs / div.

12.2.4 Output: 15 V / 3 A

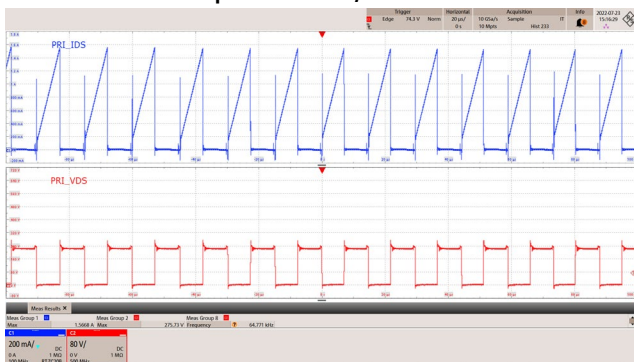


Figure 45 – Primary Drain Voltage and Current.
 90 VAC, 15.0 V, 3 A Load.
 $V_{DS_PRI} = 275.73 V$ Maximum.
 CH1: I_{DS_PRI} , 200 mA / div.
 CH2: V_{DS_PRI} , 80 V / div.
 Time: 20 μs / div.

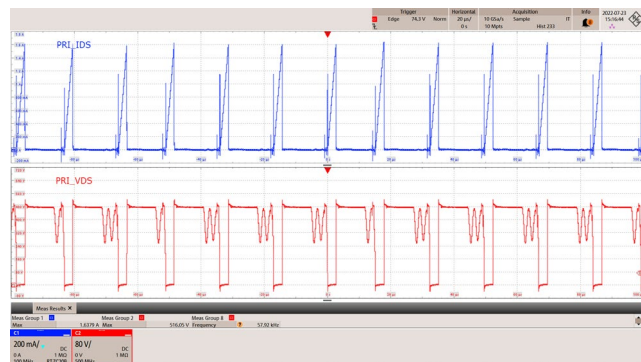


Figure 46 – Primary Drain Voltage and Current.
 265 VAC, 15.0 V, 3 A Load.
 $V_{DS_PRI} = 516.05 V$ Maximum.
 CH1: I_{DS_PRI} , 200 mA / div.
 CH2: V_{DS_PRI} , 80 V / div.
 Time: 20 μs / div.

12.2.5 Output: 20 V / 3.25 A

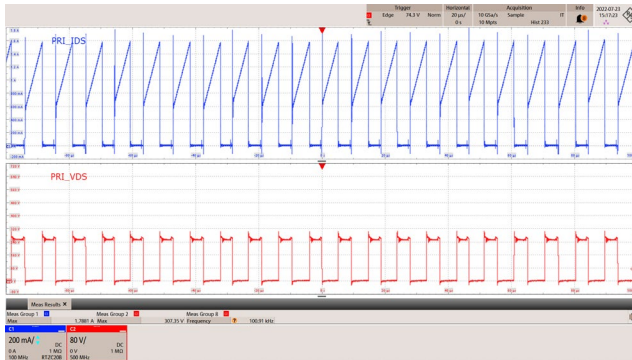


Figure 47 – Primary Drain Voltage and Current.
 90 VAC, 20.0 V, 3.25 A Load.
 $V_{DS_PRI} = 307.35$ V Maximum.
 CH1: I_{DS_PRI} , 200 mA / div.
 CH2: V_{DS_PRI} , 80 V / div.
 Time: 20 μ s / div.

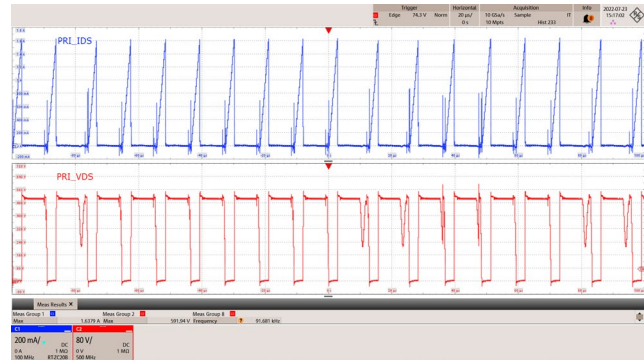


Figure 48 – Primary Drain Voltage and Current.
 265 VAC, 20.0 V, 3.25 A Load.
 $V_{DS_PRI} = 591.94$ V Maximum.
 CH1: I_{DS_PRI} , 200 mA / div.
 CH2: V_{DS_PRI} , 80 V / div.
 Time: 20 μ s / div..

12.3 SR FET Drain Voltage (Steady-State)

12.3.1 Output: 5 V / 3 A

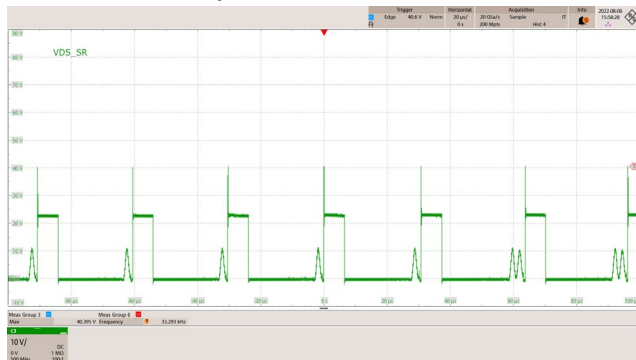


Figure 49 – SR FET Drain Voltage and Current.
 90 VAC, 5.0 V, 3 A Load.
 $V_{DS_SR} = 40.395$ V Maximum.
 CH1: V_{DS_SR} , 10 V / div.
 Time: 20 μ s / div.

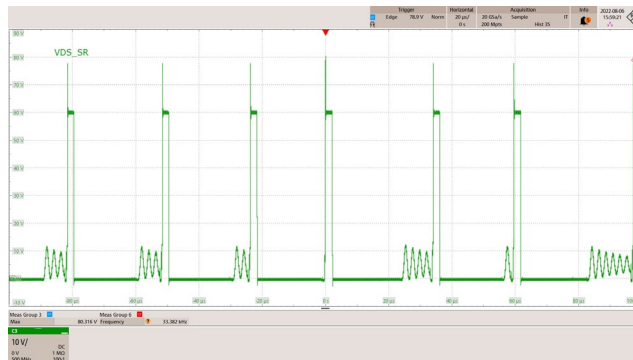


Figure 50 – SR FET Drain Voltage and Current.
 265 VAC, 5.0 V, 3 A Load.
 $V_{DS_SR} = 80.316$ V Maximum.
 CH1: V_{DS_SR} , 10 V / div.
 Time: 20 μ s / div.

12.3.2 Output: 9 V / 3 A

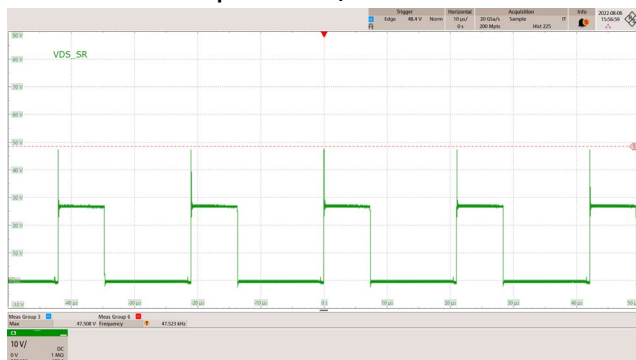


Figure 51 – SR FET Drain Voltage and Current.
 90 VAC, 9.0 V, 3 A Load.
 $V_{DS_SR} = 47.508$ V Maximum.
 CH1: V_{DS_SR} , 10 V / div.
 Time: 10 μ s / div.

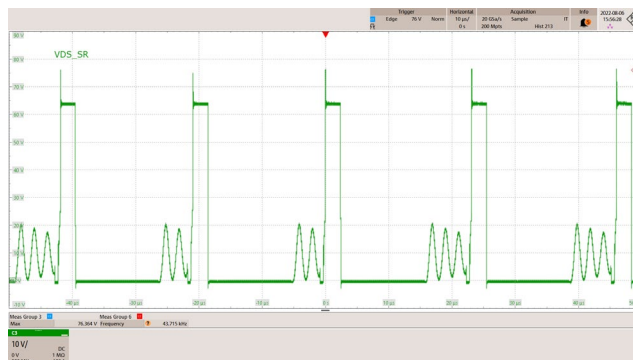


Figure 52 – SR FET Drain Voltage and Current.
 265 VAC, 9.0 V, 3 A Load.
 $V_{DS_SR} = 76.364$ V Maximum.
 CH1: V_{DS_SR} , 10 V / div.
 Time: 10 μ s / div.

12.3.3 Output: 12 V / 3 A

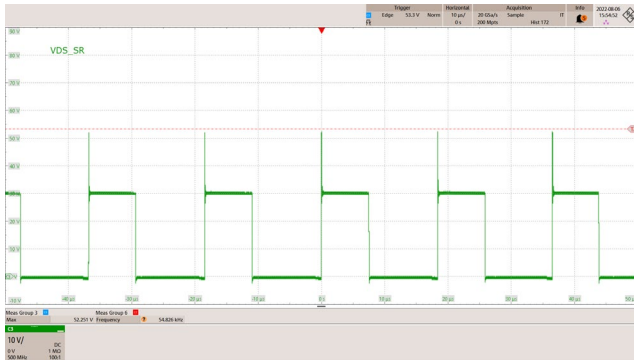


Figure 53 – SR FET Drain Voltage and Current.
 90 VAC, 12.0 V, 3 A Load.
 $V_{DS_SR} = 52.251$ V Maximum.
 CH1: V_{DS_SR} , 10 V / div.
 Time: 10 μ s / div.

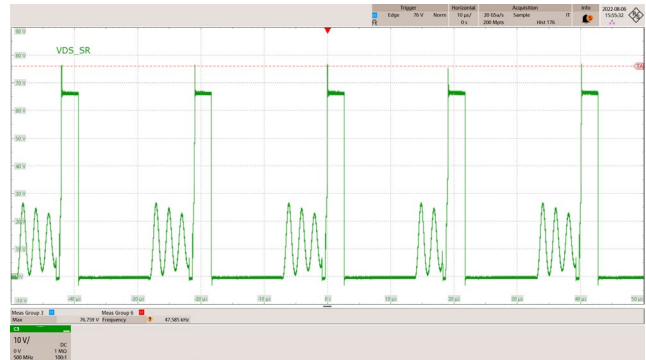


Figure 54 – SR FET Drain Voltage and Current.
 265 VAC, 12.0 V, 3 A Load.
 $V_{DS_SR} = 76.759$ V Maximum.
 CH1: V_{DS_SR} , 10 V / div.
 Time: 10 μ s / div.

12.3.4 Output: 15 V / 3 A

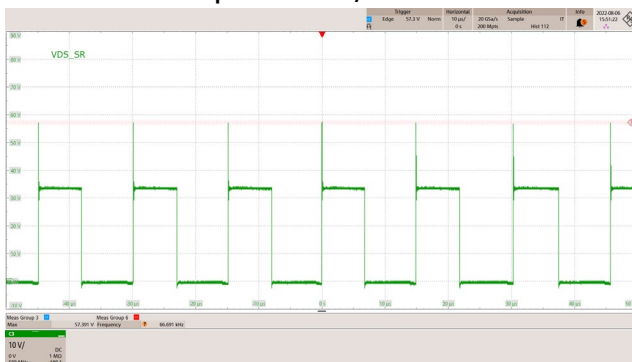


Figure 55 – SR FET Drain Voltage and Current.
 90 VAC, 15.0 V, 3 A Load.
 $V_{DS_SR} = 57.391$ V Maximum.
 CH1: V_{DS_SR} , 10 V / div.
 Time: 10 μ s / div.

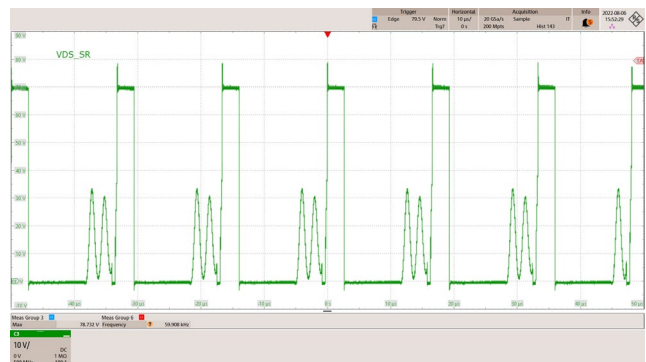


Figure 56 – SR FET Drain Voltage and Current.
 265 VAC, 15 V, 3 A Load.
 $V_{DS_SR} = 78.732$ V Maximum.
 CH1: V_{DS_SR} , 10 V / div.
 Time: 10 μ s / div.

12.3.5 Output: 20 V / 3.25 A

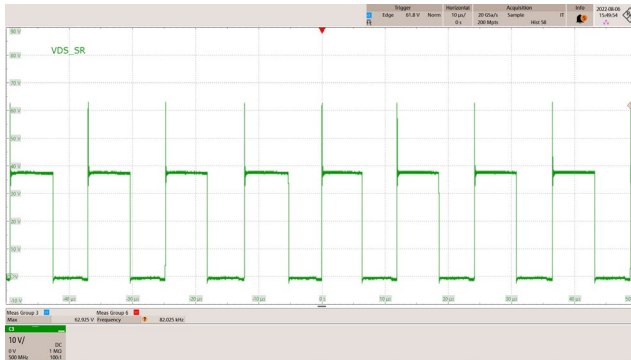


Figure 57 – SR FET Drain Voltage and Current.
 90 VAC, 20.0 V, 3.25 A Load.
 $V_{DS_SR} = 62.925$ V Maximum.
 CH1: V_{DS_SR} , 10 V / div.
 Time: 10 μ s / div.

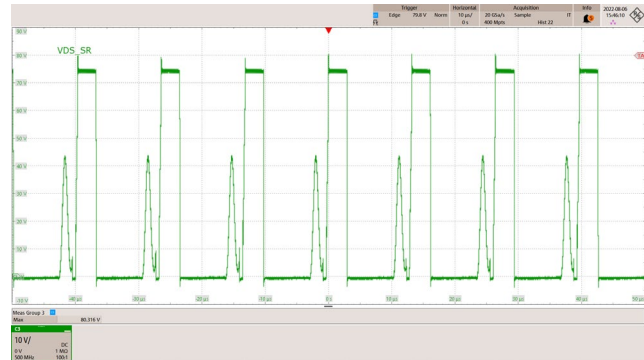


Figure 58 – SR FET Drain Voltage and Current.
 265 VAC, 20.0 V, 3.25 A Load.
 $V_{DS_SR} = 80.316$ V Maximum.
 CH1: V_{DS_SR} , 10 V / div.
 Time: 10 μ s / div.

12.4 Primary and SR FET Drain Voltage and Current (during Output Voltage Transition)

12.4.1 Primary Drain Voltage and Current, 3.3 V to 21 V PPS Transition

Primary Drain Voltage, Drain Current, and output voltage on the board were captured. The USB PD Sink Request was changed from 3.3 V to 21 V / 3.0 A PPS (PDO6) while the load current is at 2.85 A (~95% of current limit).

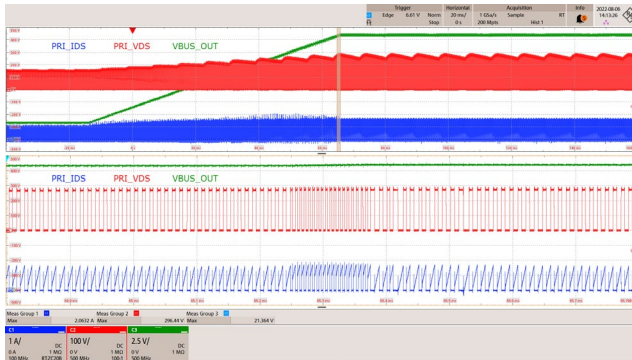


Figure 59 – Primary Drain Voltage and Current.
90 VAC, 3.3 V to 21 V V_{OUT} Transition,
2.85 A Load.
 $V_{DS_PRI} = 296.44$ V Maximum.
CH1: I_{DS_PRI} , 1 A / div.
CH2: V_{DS_PRI} , 100 V / div.
CH3: V_{BUS_OUT} , 2.5 V / div.
Time: 20 ms / div. (100 μ s / div. Zoom).



Figure 60 – Primary Drain Voltage and Current.
265 VAC, 3.3 V to 21 V V_{OUT} Transition,
2.85 A Load.
 $V_{DS_PRI} = 553.36$ V Maximum.
CH1: I_{DS_PRI} , 1 A / div.
CH2: V_{DS_PRI} , 200 V / div.
CH3: V_{BUS_OUT} , 2.5 V / div.
Time: 20 ms / div. (100 μ s / div. Zoom).

12.4.2 SR FET Drain Voltage, 3.3 V to 21 V Transition

SR FET Drain Voltage and output voltage on the board were captured. The USB PD Sink Request was changed from 3.3 V to 21 V / 3.0 A PPS (PDO6) while the load current is at 2.85 A (~95% of current limit). Note that the SR FET used in this design is rated for 120 V spike.

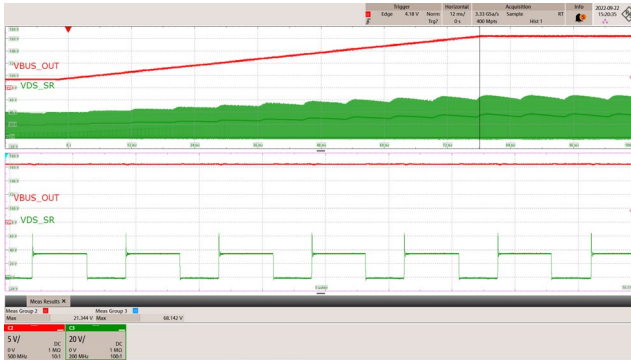


Figure 61 – SR FET Drain Voltage
 90 VAC, 3.3 V to 21 V V_{OUT} Transition,
 2.85A Load.
 $V_{DS_SRFET} = 68.142$ V Maximum.
 CH2: V_{BUS_OUT} , 5 V / div.
 CH3: V_{DS_SR} , 20 V / div.
 Time: 12 ms / div. (5 μ s / div. Zoom).

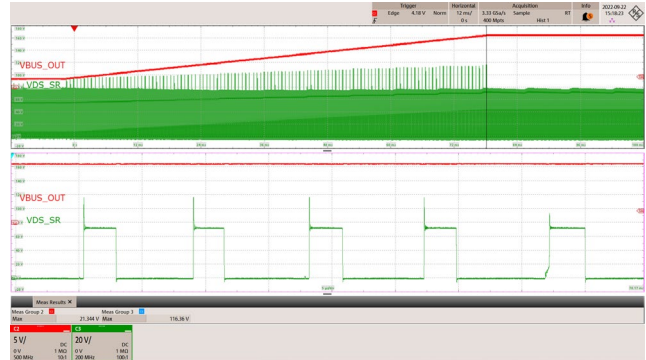


Figure 62 – SR FET Drain Voltage
 265 VAC, 3.3 V to 21 V V_{OUT} Transition,
 2.85 A Load.
 $V_{DS_SRFET} = 116.36$ V Maximum.
 CH2: V_{BUS_OUT} , 5 V / div.
 CH3: V_{DS_SR} , 20 V / div.
 Time: 12 ms / div. (5 μ s / div. Zoom).

12.4.3 SR FET Drain Voltage, Downward Vout Transition

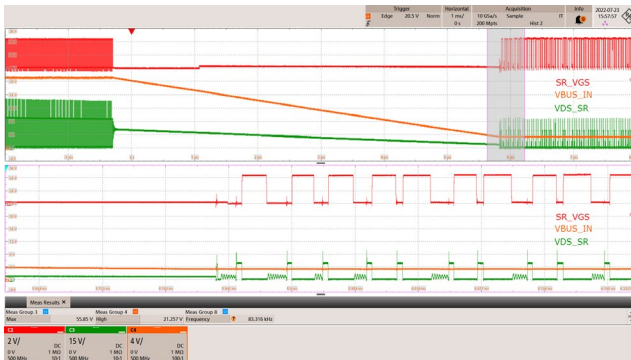


Figure 63 – SR FET Drain Voltage and Gate Voltage
 90 VAC, 21 V to 3.3 V V_{OUT} Transition,
 2.85 A Load.
 $V_{DS_SRFET} = 55.85$ V Maximum.
 CH2: V_{GS_SR} , 2 V / div.
 CH3: V_{DS_SR} , 15 V / div.
 CH4: V_{BUS_IN} , 4 V / div.
 Time: 1 ms / div. (59 μ s / div. Zoom).

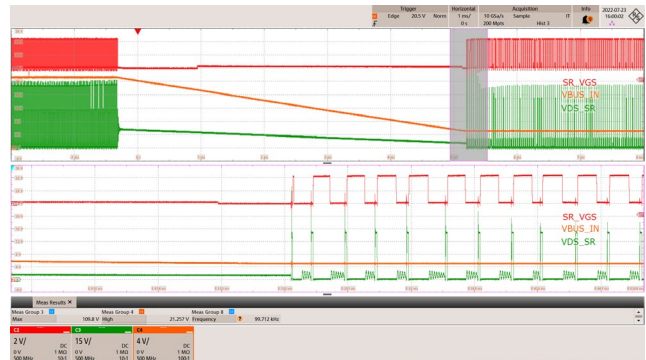


Figure 64 – SR FET Drain Voltage and Gate Voltage
 265 VAC, 21 V to 5 V V_{OUT} Transition,
 2.85 A Load.
 $V_{DS_SRFET} = 109.8$ V Maximum.
 CH2: V_{GS_SRFET} , 2 V / div.
 CH3: V_{DS_SRFET} , 15 V / div.
 CH4: V_{BUS_IN} , 4 V / div.
 Time: 1 ms / div. (59 μ s / div. Zoom).

12.5 Load Transient Response

Output voltage waveform on the board was captured with dynamic load transient from 10% to 100%. Duration for load states (high = 20 ms; low = 20 ms) was chosen to clearly show steady-state for each load condition. Load slew rate (150 mA / μ s) is based on USB PD 3.0 specification.

USB PD 3.0 specification allows a voltage overshoot /undershoot of ± 0.5 V (vSrcValid) on top of $\pm 5\%$ tolerance from the operating voltage (vSrcNew) within the first 5 ms of applying a load transient (tSrcTransient). Beyond 5 ms, the voltage limits are tightened to $\pm 5\%$ within the operating voltage.

12.5.1 Output: 5 V / 3 A

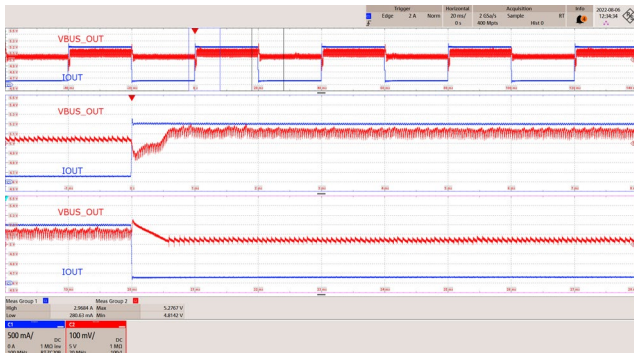


Figure 65 – Load transient response.
 90 VAC, 5.0 V, 0.3 to 3 A Load.
 V_{BUS_OUT} = 5.277 V Max., 4.814 V Min.
 CH1: IOUT, 500 mA / div.
 CH2: V_{BUS_OUT} , 100 mV / div.
 Time: 20 ms / div. (1 ms / div. Zoom).

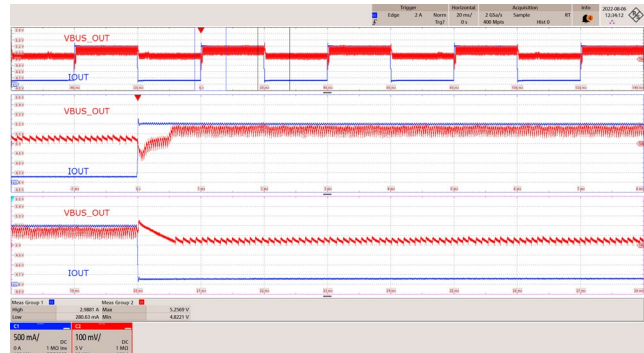


Figure 66 – Load transient response.
 265 VAC, 5.0 V, 0.3 to 3 A Load.
 V_{BUS_OUT} = 5.257 V Max., 4.822 V Min.
 CH1: IOUT, 500 mA / div.
 CH2: V_{BUS_OUT} , 100 mV / div.
 Time: 20 ms / div. (1 ms / div. Zoom).

12.5.2 Output: 9 V / 3 A

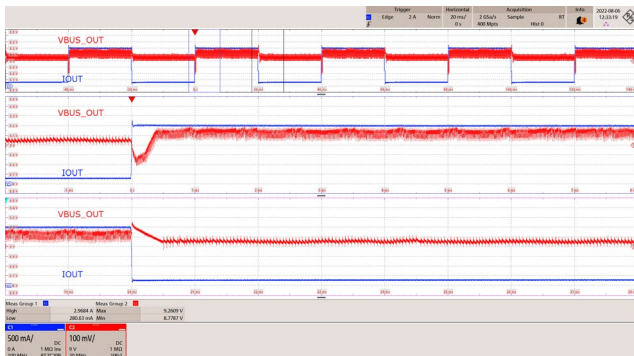


Figure 67 – Transient Response.
 90 VAC, 9.0 V, 0.3 to 3 A Load.
 V_{BUS_OUT} = 9.2609 V Max., 8.7787 V Min.
 CH1: IOUT, 500 mA / div.
 CH2: V_{BUS_OUT} , 100 mV / div.
 Time: 20 ms / div. (1 ms / div. Zoom).

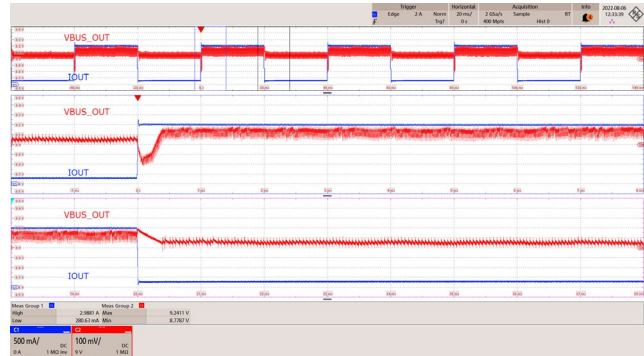


Figure 68 – Transient Response.
 265 VAC, 9.0 V, 0.3 to 3 A Load.
 V_{BUS_OUT} = 9.2411 V Max., 8.7787 V Min.
 CH1: IOUT, 500 mA / div.
 CH2: V_{BUS_OUT} , 100 mV / div.
 Time: 20 ms / div. (1 ms / div. Zoom).



12.5.3 Output: 12 V / 3 A

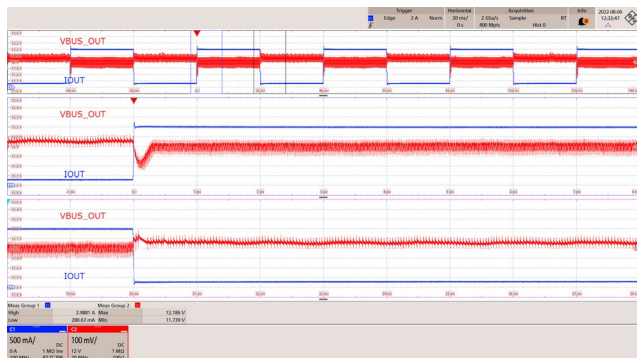


Figure 69 – Transient Response.
 90 VAC, 12.0 V, 0.3 to 3 A Load.
 $V_{BUS_OUT} = 12.186\text{ V Max.}, 11.739\text{ V Min.}$
 CH1: I_{OUT} , 500 mA / div.
 CH2: V_{BUS_OUT} , 100 mV / div.
 Time: 20 ms / div. (1 ms / div. Zoom).

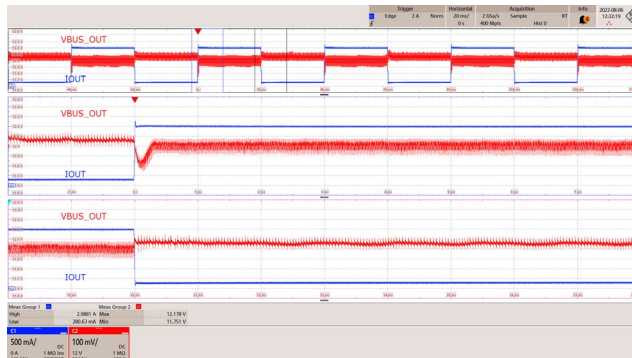


Figure 70 – Transient Response.
 265 VAC, 12.0 V, 0.3 to 3 A Load.
 $V_{BUS_OUT} = 12.178\text{ V Max.}, 11.751\text{ V Min.}$
 CH1: I_{OUT} , 500 mA / div.
 CH2: V_{BUS_OUT} , 100 mV / div.
 Time: 20 ms / div. (1 ms / div. Zoom).

12.5.4 Output: 15 V / 3 A

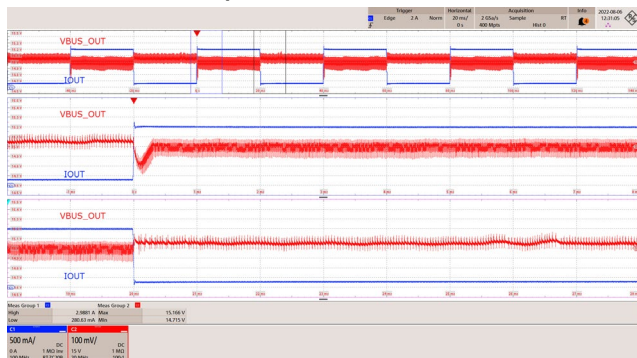


Figure 71 – Transient Response.
 90 VAC, 15.0 V, 0.3 to 3 A Load.
 $V_{BUS_OUT} = 15.166\text{ V Max.}, 14.715\text{ V Min.}$
 CH1: I_{OUT} , 500 mA / div.
 CH2: V_{BUS_OUT} , 100 mV / div.
 Time: 20 ms / div. (1 ms / div. Zoom).

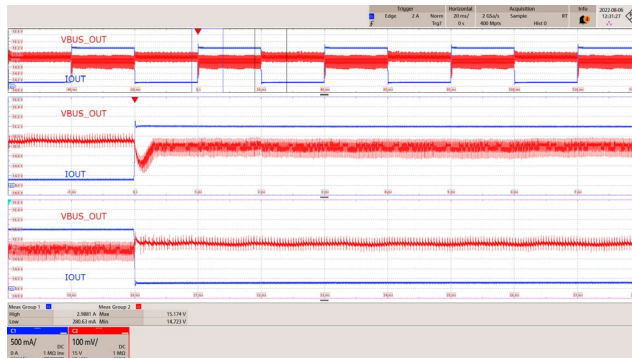


Figure 72 – Transient Response.
 265 VAC, 15.0 V, 0.3 to 3 A Load.
 $V_{BUS_OUT} = 15.174\text{ V Max.}, 14.723\text{ V Min.}$
 CH1: I_{OUT} , 500 mA / div.
 CH2: V_{BUS_OUT} , 100 mV / div.
 Time: 20 ms / div. (1 ms / div. Zoom).

12.5.5 Output: 20 V / 3.25 A

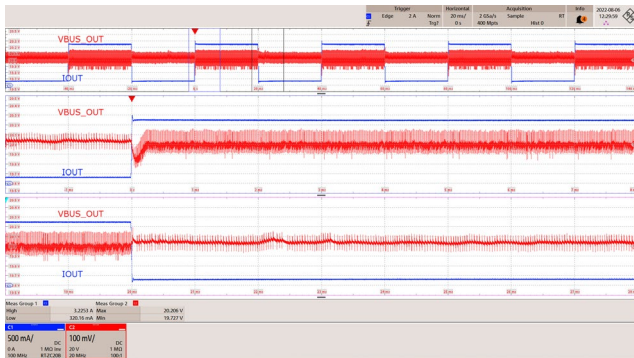


Figure 73 – Transient Response.
 90 VAC, 20.0 V, 0.325 to 3.25 A Load.
 $V_{BUS_OUT} = 20.206 \text{ V Max.}, 19.727 \text{ V Min.}$
 CH1: I_{OUT} , 500 mA / div.
 CH2: V_{BUS_OUT} , 100 mV / div.
 Time: 20 ms / div. (1 ms / div. Zoom).

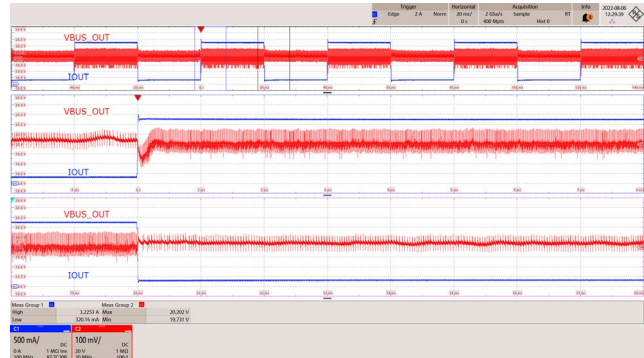


Figure 74 – Transient Response.
 265 VAC, 20.0 V, 0.325 to 3.25 A Load.
 $V_{BUS_OUT} = 20.202 \text{ V Max.}, 19.731 \text{ V Min.}$
 CH1: I_{OUT} , 500 mA / div.
 CH2: V_{BUS_OUT} , 100 mV / div.
 Time: 20 ms / div. (1 ms / div. Zoom).

12.6 Output Ripple Measurements

12.6.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF /50 V ceramic type and one (1) 47 μF /50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

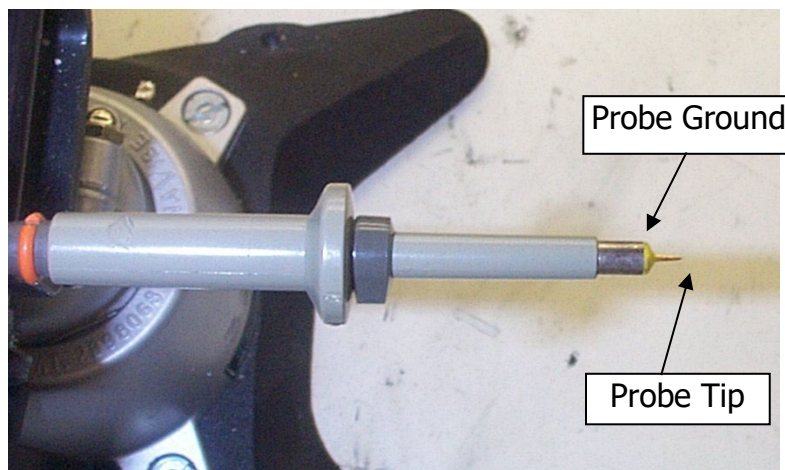


Figure 75 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)



Figure 76 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

12.6.2 Output Voltage Ripple Waveforms

Output voltage ripple waveform at full load was captured at the end of 100 mΩ cable using the ripple measurement probe with decoupling capacitors.

12.6.2.1 Output: 5 V / 3 A

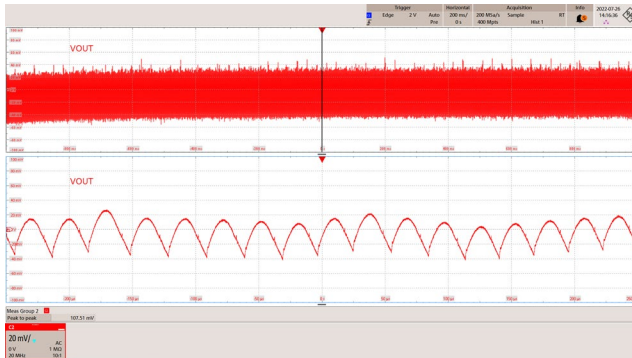


Figure 77 – Output Voltage Ripple.
90 VAC, 5.0 V, 3 A Load.
 $V_{OUT(AC)} = 107.5$ mV Peak-to-Peak.
CH1: $V_{OUT(AC)}$, 20 mV / div.
Time: 200 ms / div. (50 μ s / div. Zoom).

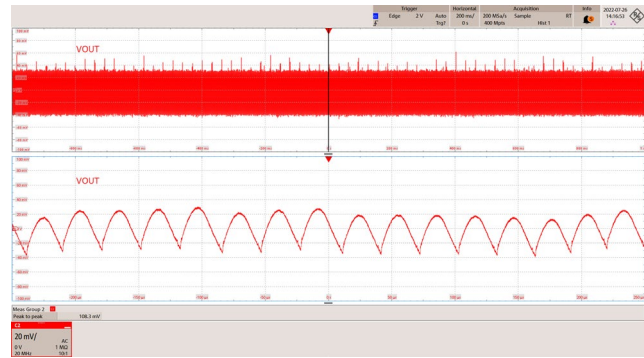


Figure 78 – Output Voltage Ripple.
265 VAC, 5.0 V, 3 A Load.
 $V_{OUT(AC)} = 108.3$ mV Peak-to-Peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 200 ms / div. (50 μ s / div. Zoom).

12.6.2.2 Output: 9 V / 3 A

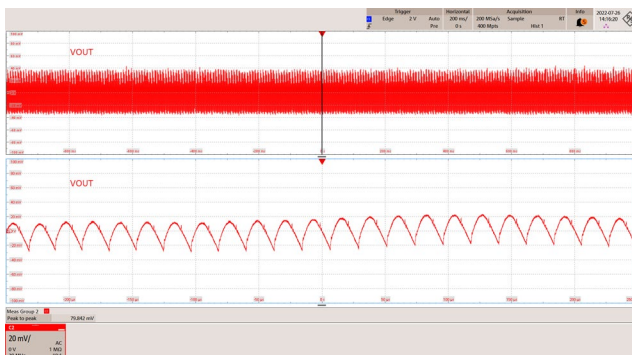


Figure 79 – Output Voltage Ripple.
90 VAC, 9.0 V, 3 A Load.
 $V_{OUT(AC)} = 79.8$ mV Peak-to-Peak.
CH1: $V_{OUT(AC)}$, 20 mV / div.
Time: 200 ms / div. (50 μ s / div. Zoom).

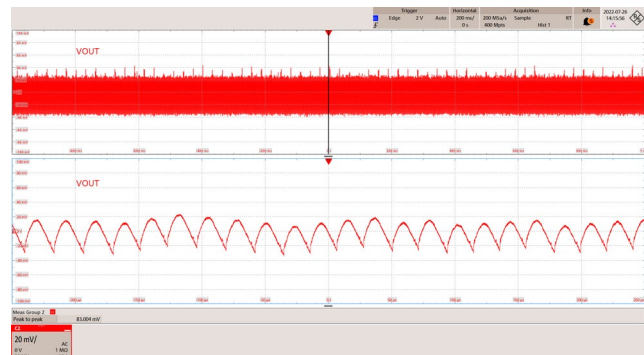


Figure 80 – Output Voltage Ripple.
265 VAC, 9.0 V, 3 A Load.
 $V_{OUT(AC)} = 83$ mV Peak-to-Peak.
CH1: $V_{OUT(AC)}$, 20 mV / div.
Time: 200 ms / div. (50 μ s / div. Zoom).

12.6.2.3 Output: 12 V / 3 A

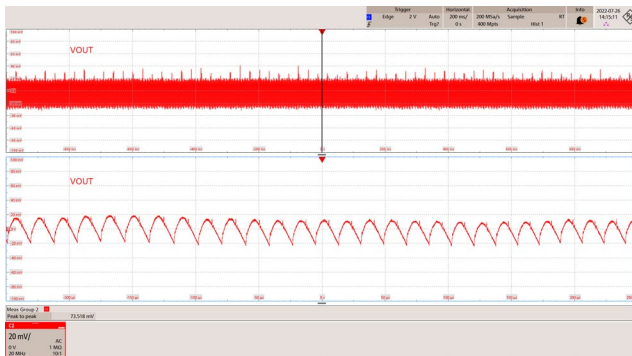


Figure 81 – Output Voltage Ripple.
 90 VAC, 12.0 V, 3 A Load.
 $V_{OUT(AC)} = 73.5$ mV Peak-to-Peak.
 CH1: $V_{OUT(AC)}$, 20 mV / div.
 Time: 200 ms / div. (50 μ s / div. Zoom).

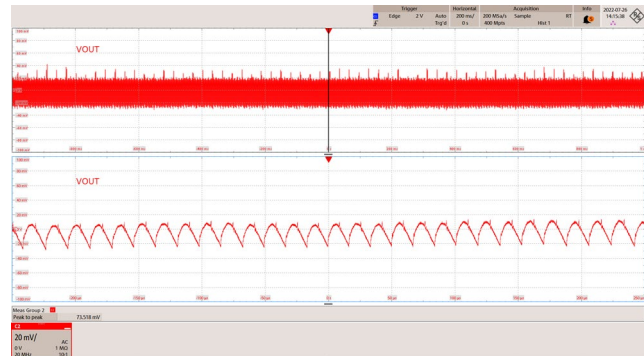


Figure 82 – Output Voltage Ripple.
 265 VAC, 12.0 V, 3 A Load.
 $V_{OUT(AC)} = 73.5$ mV Peak-to-Peak.
 CH1: $V_{OUT(AC)}$, 20 mV / div.
 Time: 200 ms / div. (50 μ s / div. Zoom).

12.6.2.4 Output: 15 V / 3 A

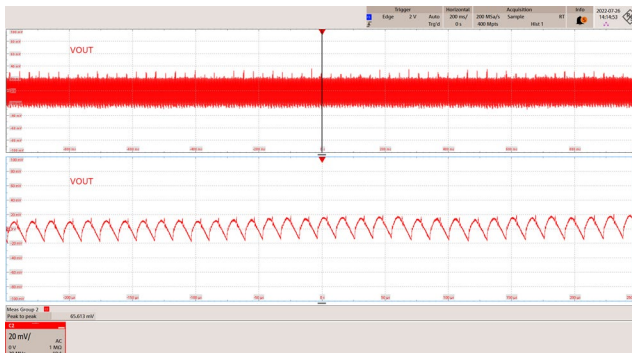


Figure 83 – Output Voltage Ripple.
 90 VAC, 15.0 V, 3 A Load.
 $V_{OUT(AC)} = 65.6$ mV Peak-to-Peak.
 CH1: $V_{OUT(AC)}$, 20 mV / div.
 Time: 200 ms / div. (50 μ s / div. Zoom).

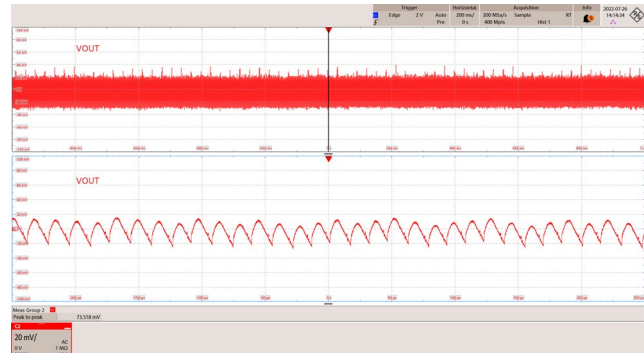


Figure 84 – Output Voltage Ripple.
 265 VAC, 15.0 V, 3 A Load.
 $V_{OUT(AC)} = 73.5$ mV Peak-to-Peak.
 CH1: $V_{OUT(AC)}$, 20 mV / div.
 Time: 200 ms / div. (50 μ s / div. Zoom).

12.6.2.5 Output: 20 V / 3.25 A

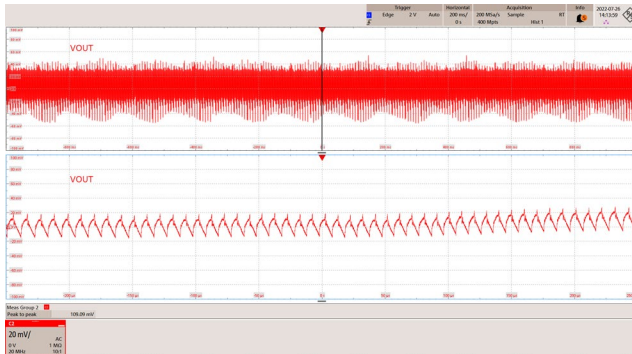


Figure 85 – Output Voltage Ripple.
 90 VAC, 20.0 V, 3.25 A Load.
 $V_{OUT(AC)}$ = 109 mV Peak-to-Peak.
 CH1: $V_{OUT(AC)}$, 20 mV / div.
 Time: 200 ms / div. (50 μs / div. Zoom).

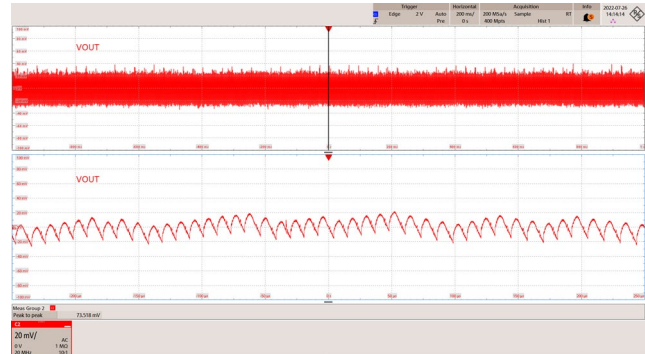


Figure 86 – Output Voltage Ripple.
 265 VAC, 20.0 V, 3.25 A Load.
 $V_{OUT(AC)}$ = 73.5 mV Peak-to-Peak.
 CH1: $V_{OUT(AC)}$, 20 mV / div.
 Time: 200 ms / div. (50 μs / div. Zoom).

12.6.3 Output Voltage Ripple Amplitude vs. Load

12.6.3.1 Output: 5 V / 3 A

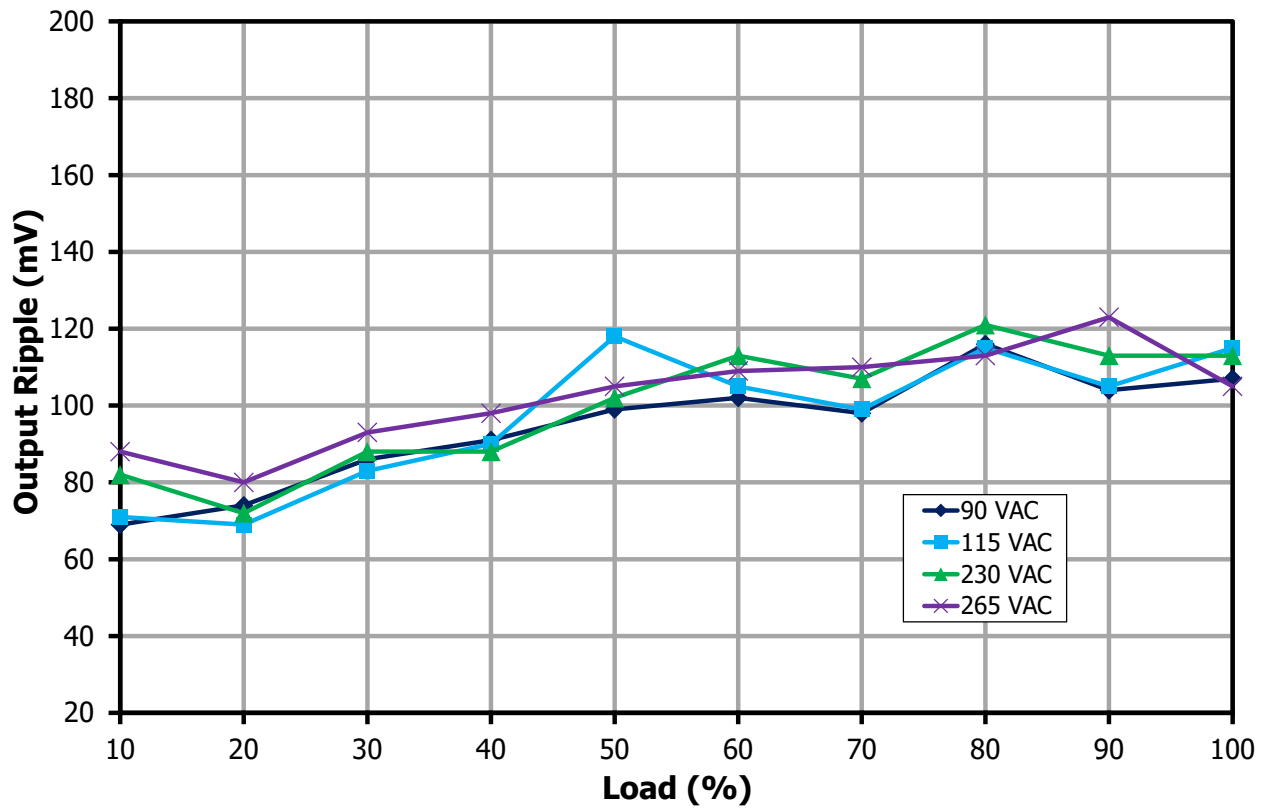


Figure 87 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 5 V Output.

12.6.3.2 Output: 9 V / 3 A

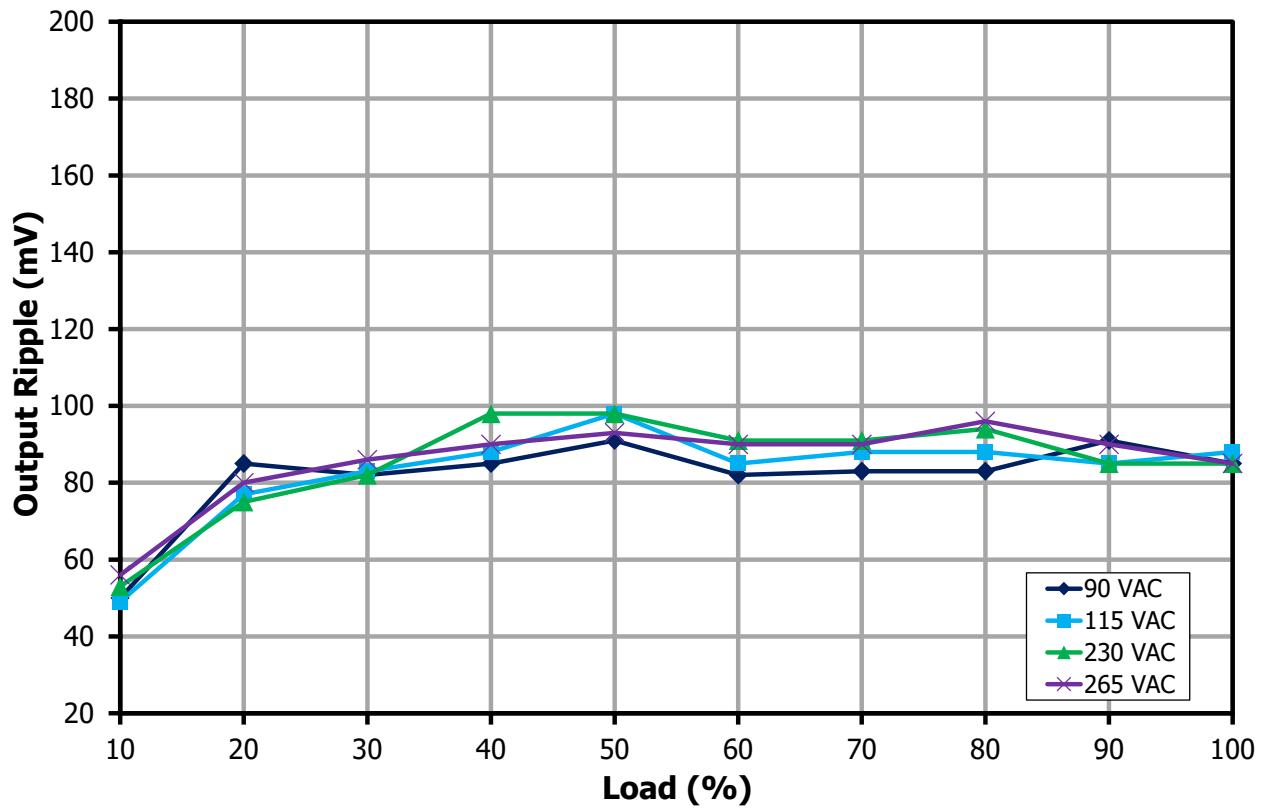


Figure 88 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 9 V Output.

12.6.3.3 Output: 12 V / 3 A

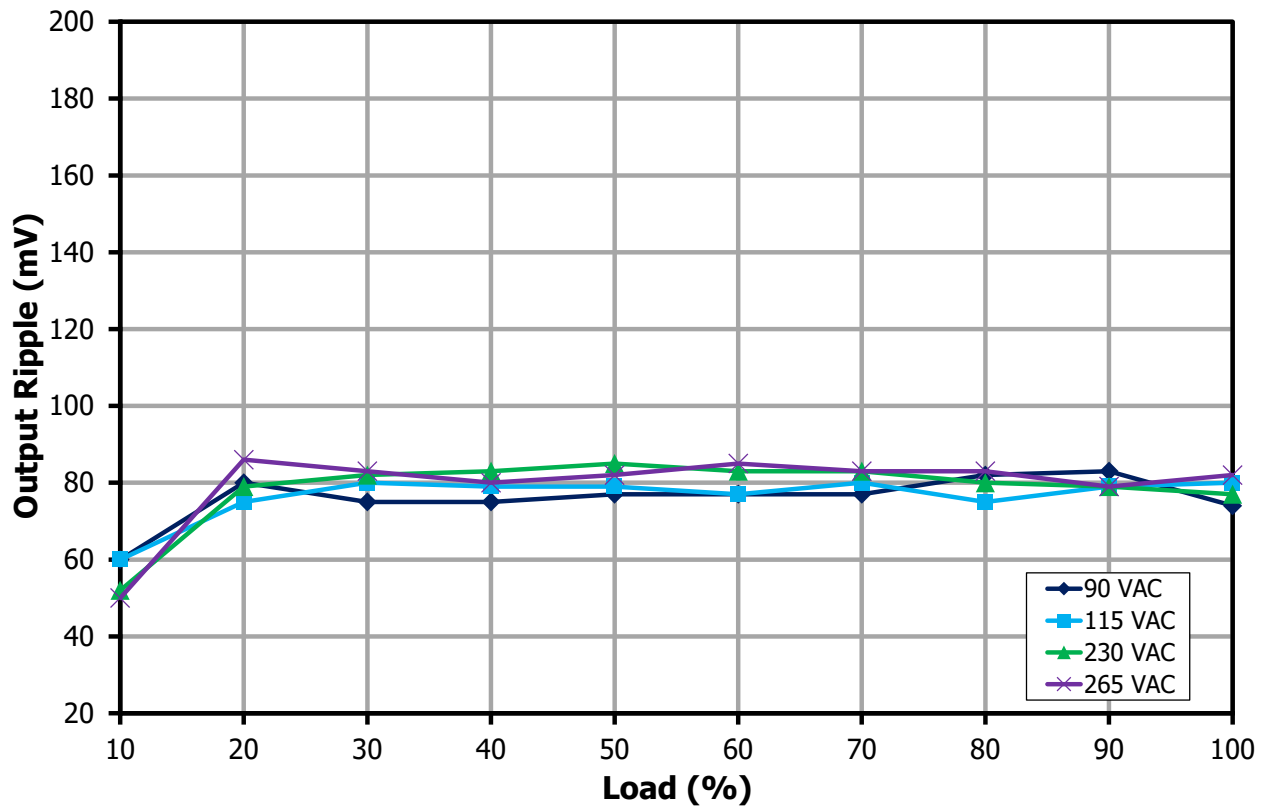


Figure 89 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 12 V Output.

12.6.3.4 Output: 15 V / 3 A

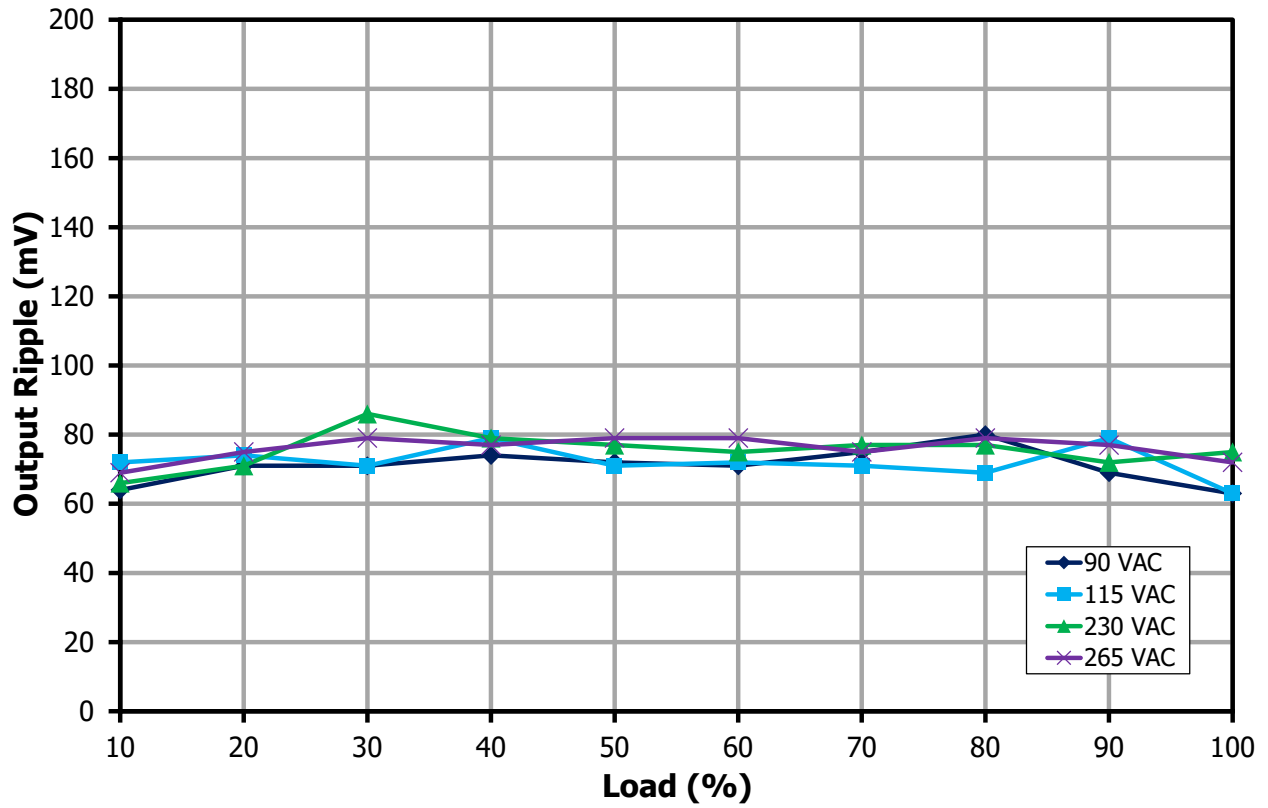


Figure 90 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 15 V Output.

12.6.3.5 Output: 20 V / 3.25 A

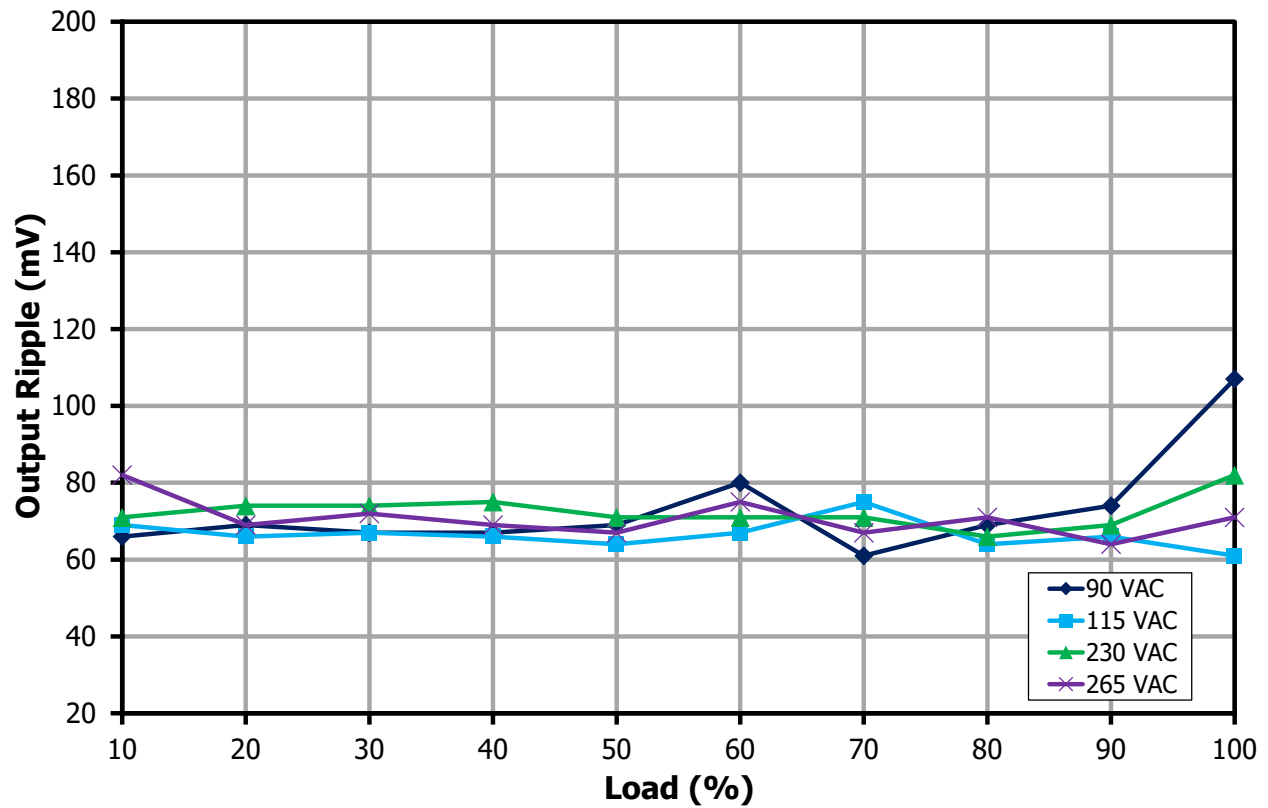


Figure 91 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 20 V Output.

13 CV/CC Profile

One Programmable Power Supply (PPS) Augmented Power Data Object (APDO) is supported in this design:

- PDO6: 3.3 V – 21 V / 3 A PPS

CV/CC profiles were taken with the output voltage measured on the board.

13.1 Output: 21 V / 3 A PPS Request, PDO6

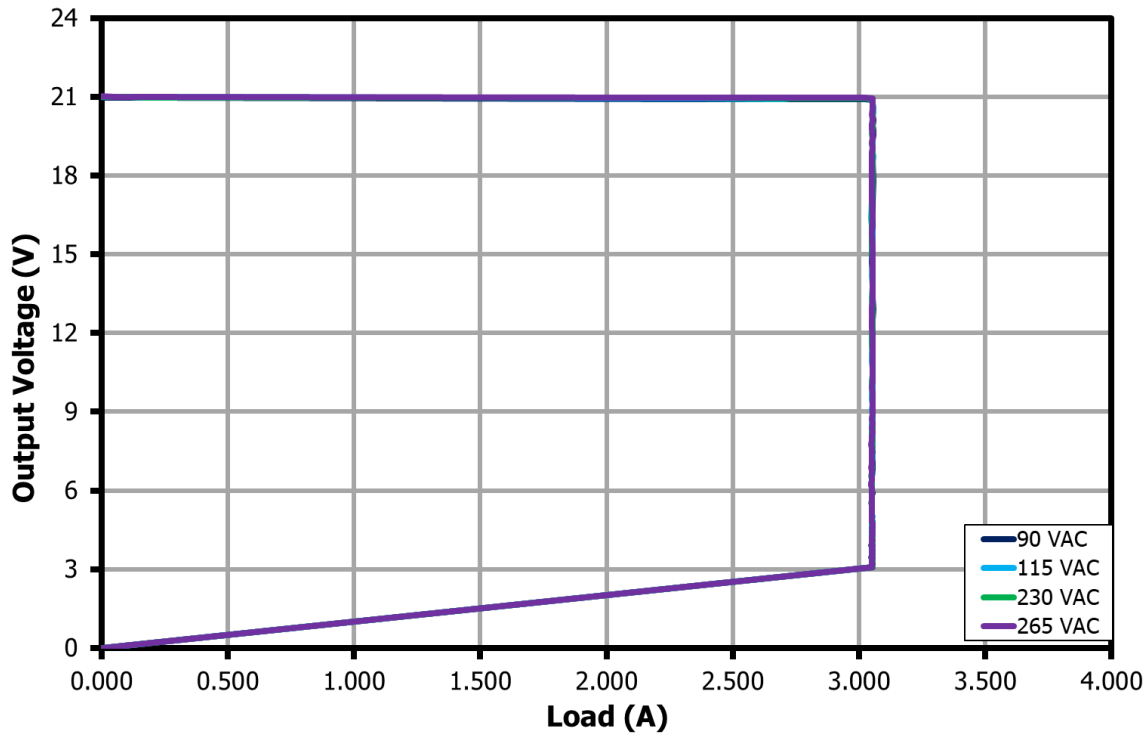


Figure 92 – CV/CC Profile for 21 V / 3 A PPS Request.

14 Voltage Step and Current Limit Test using QuadraMAX and Total Phase Analyzer

The power supply was evaluated and passed both QuadraMAX PPS Voltage Step Test (VST) and PPS Current Limit Test (CLT). The output voltage and current during VST and CLT as recorded by the Total Phase Analyzer are presented below.

14.1 Voltage Step Test (VST)

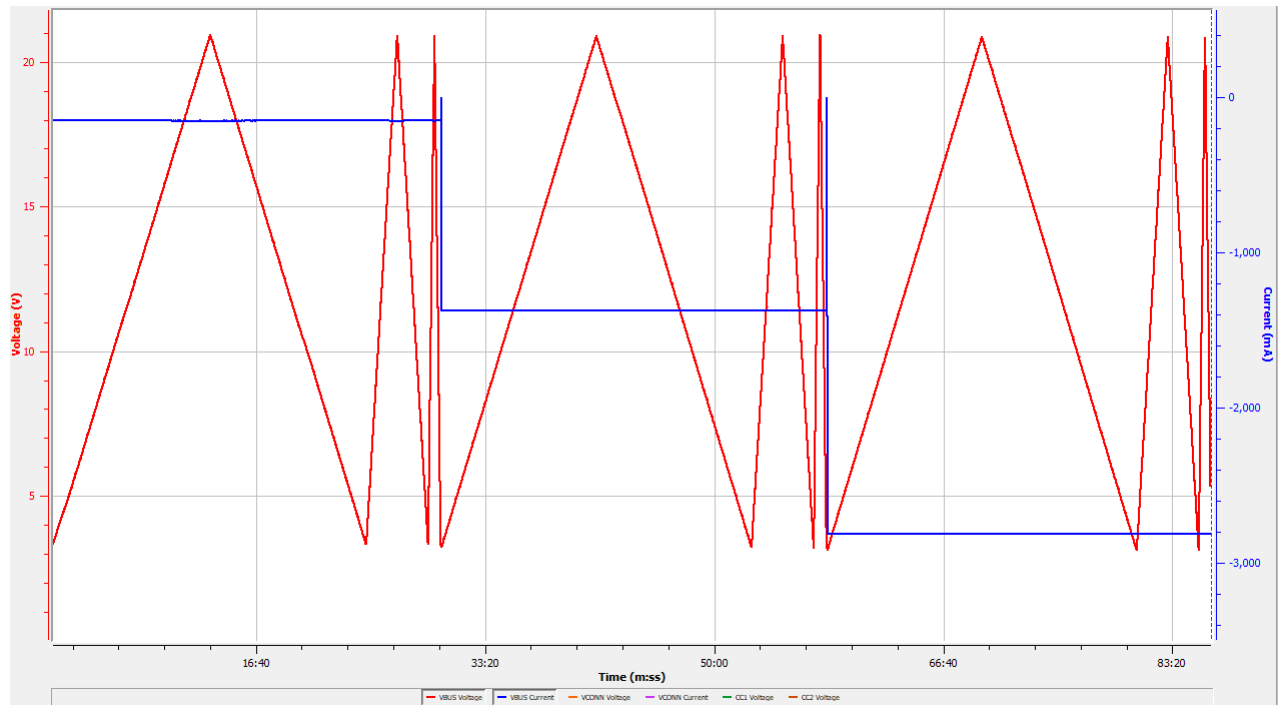


Figure 93 – Plot of SPT.6 VST from Total Phase Analyzer.

14.2 Current Limit Test (CLT)

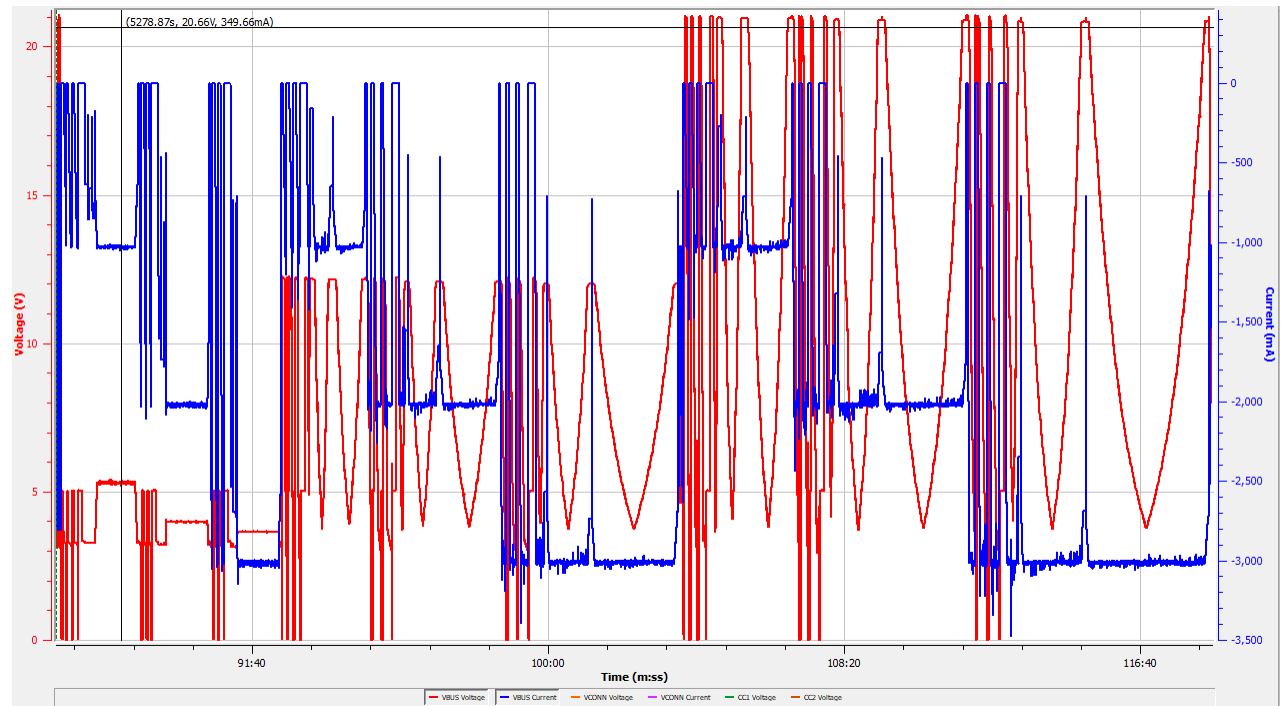
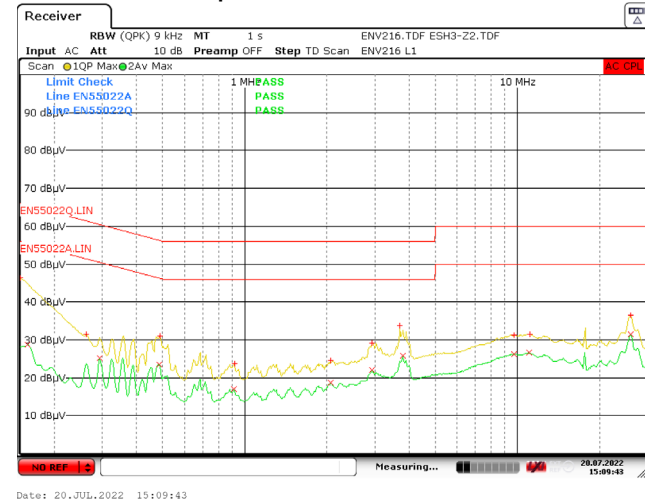


Figure 94 – Plot of SPT.7 CLT from Total Phase Analyzer.

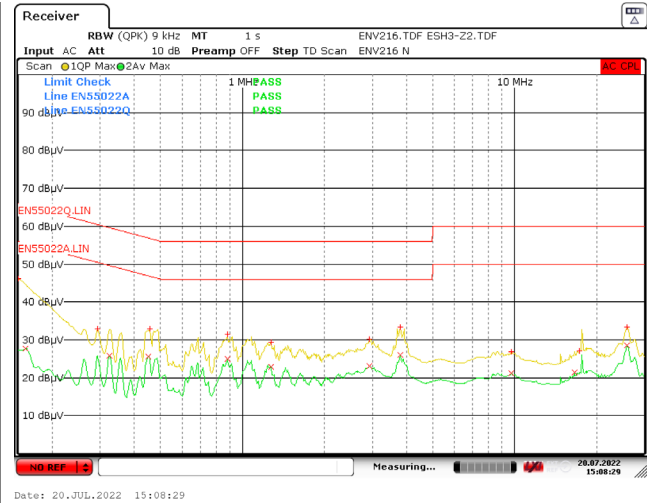
15 Conducted EMI

15.1 Floating Ground (QPK / AV)

15.1.1 Output: 5 V / 3 A

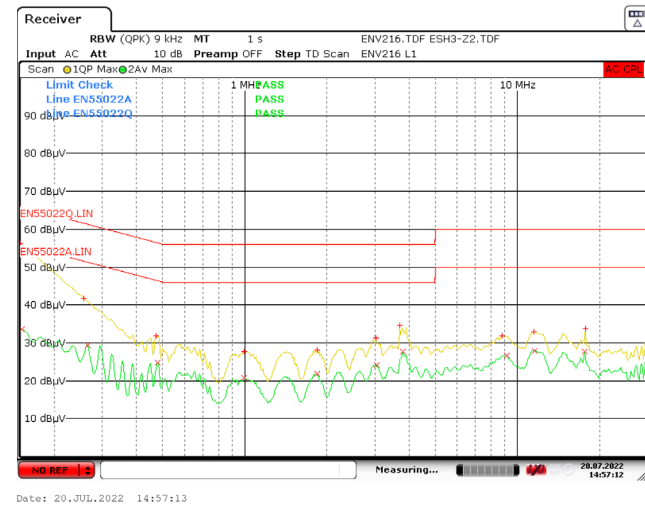


115 VAC.

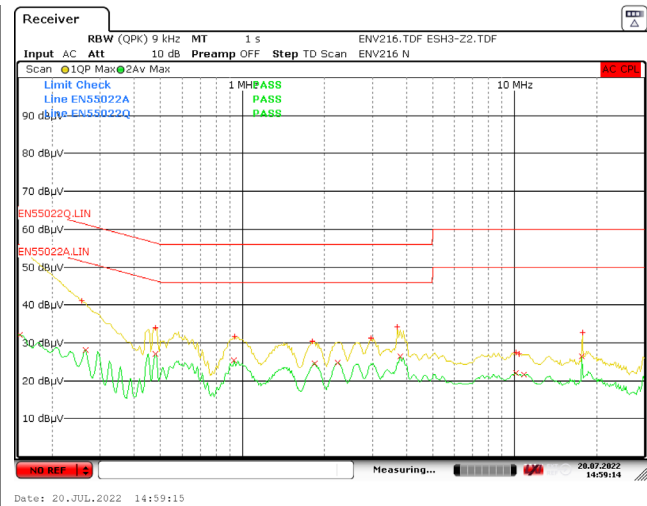


230 VAC.

Figure 95 – Floating Ground EMI, 5 V / 3 A Load [Line Scan].



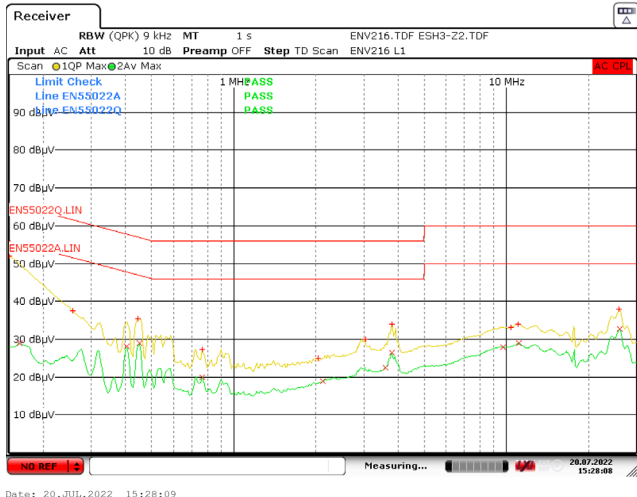
115 VAC.



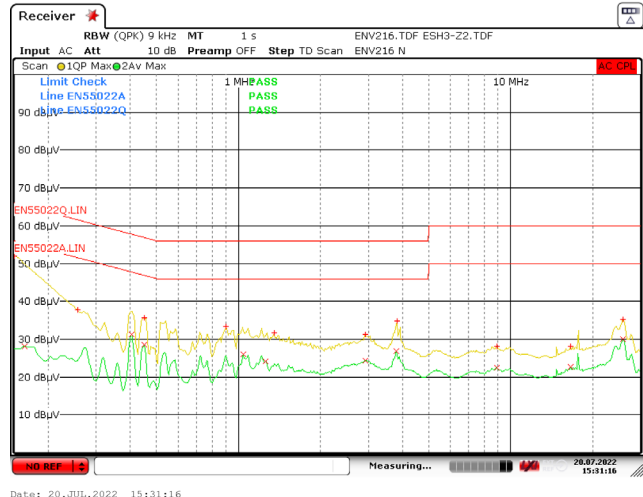
230 VAC.

Figure 96 – Floating Ground EMI, 5 V / 3 A Load [Neutral Scan].

15.1.2 Output: 9 V / 3 A

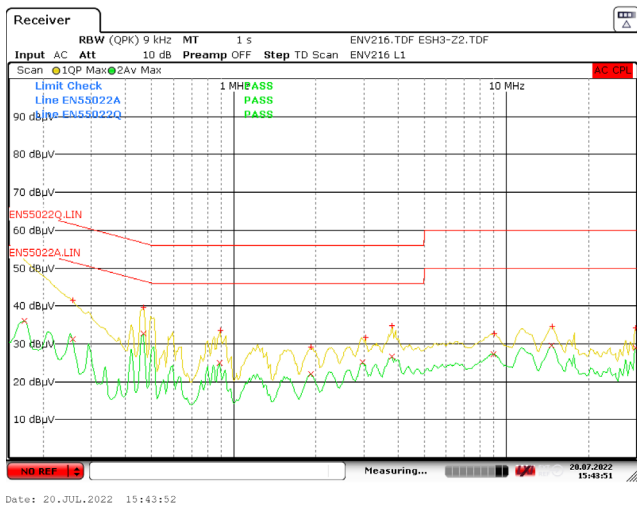


115 VAC.

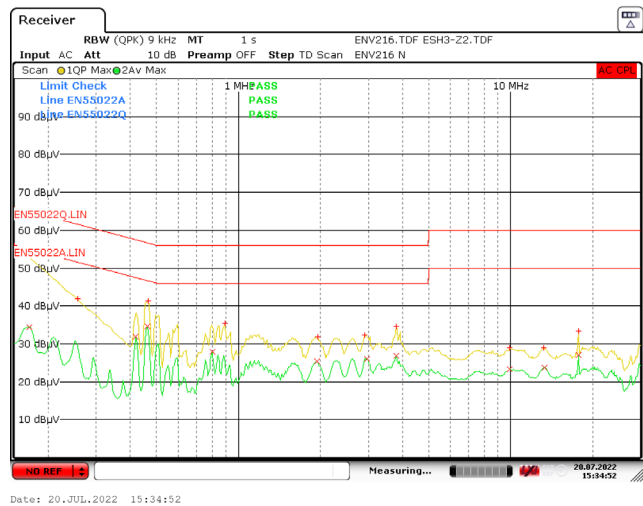


230 VAC.

Figure 97 – Floating Ground EMI, 9 V / 3 A Load [Line Scan].



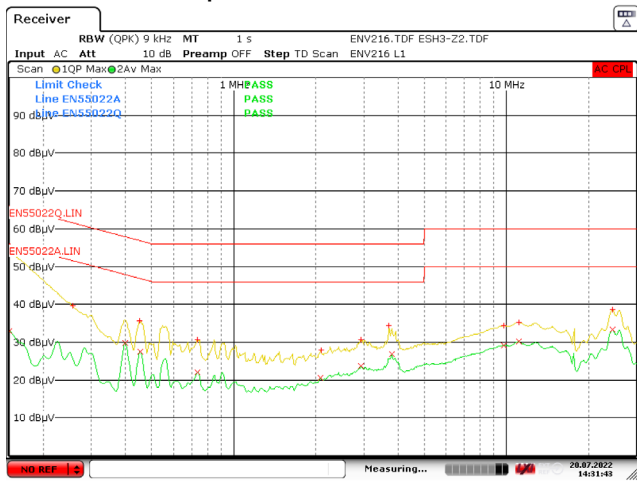
115 VAC.



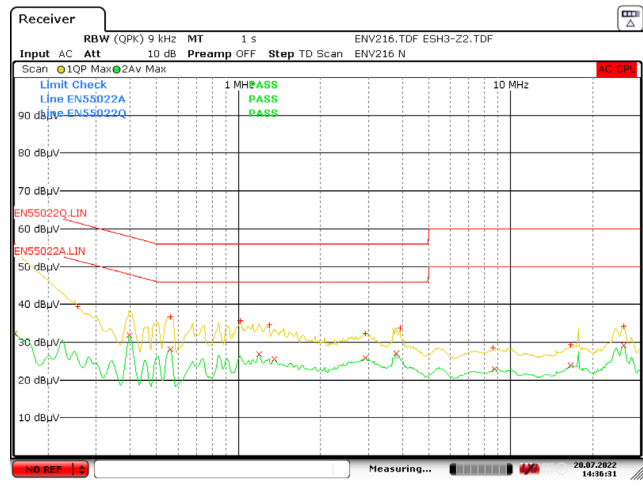
230 VAC.

Figure 98 – Floating Ground EMI, 9 V / 3 A Load [Neutral Scan].

15.1.3 Output: 12 V / 3 A

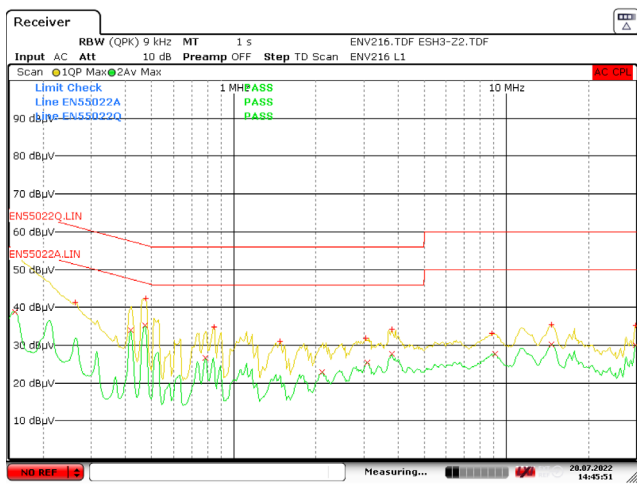


115 VAC.

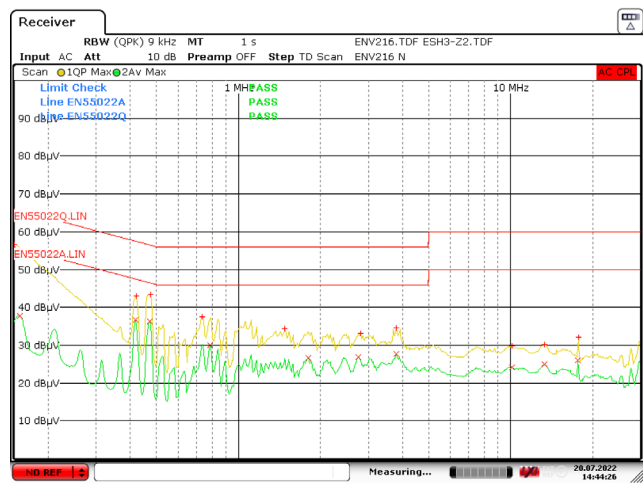


230 VAC.

Figure 99 – Floating Ground EMI, 12 V / 3 A Load [Line Scan].



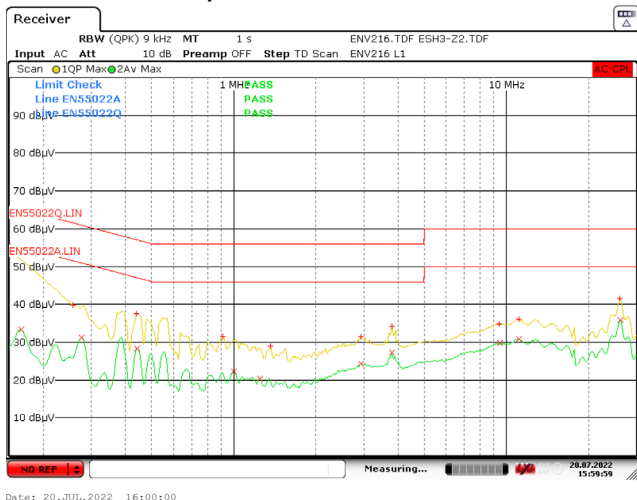
115 VAC.



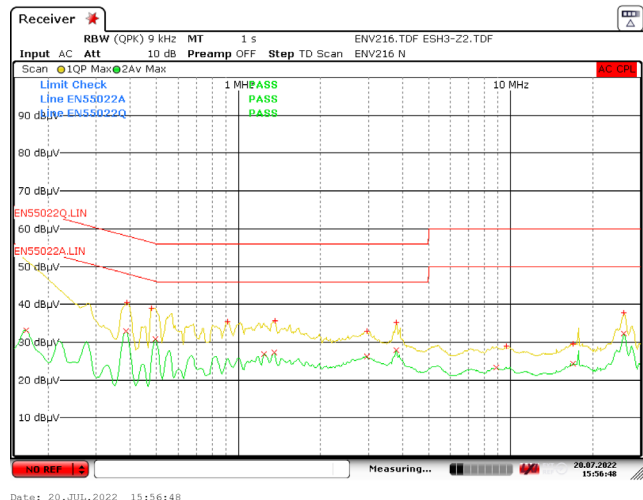
230 VAC.

Figure 100 – Floating Ground EMI, 12 V / 3 A Load [Neutral Scan].

15.1.4 Output: 15 V / 3 A

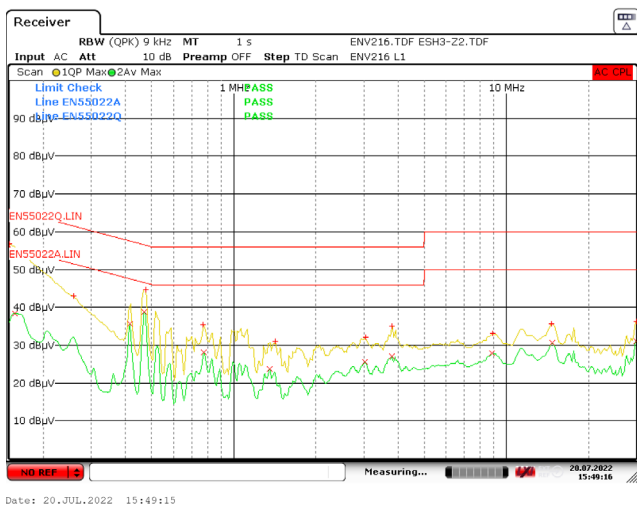


115 VAC.

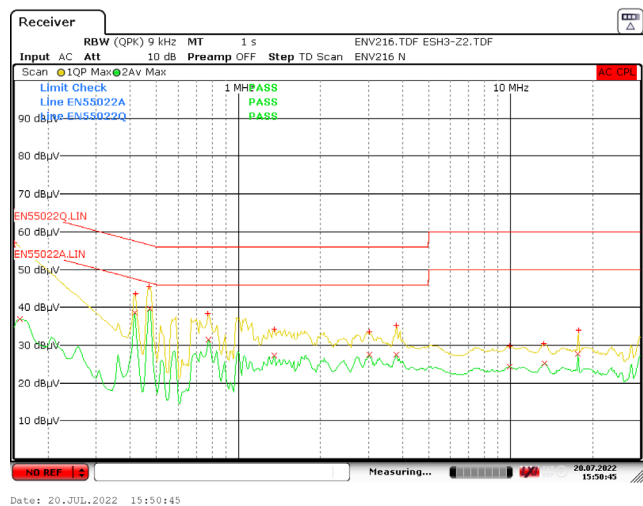


230 VAC.

Figure 101 – Floating Ground EMI, 15 V / 3 A Load [Line Scan].



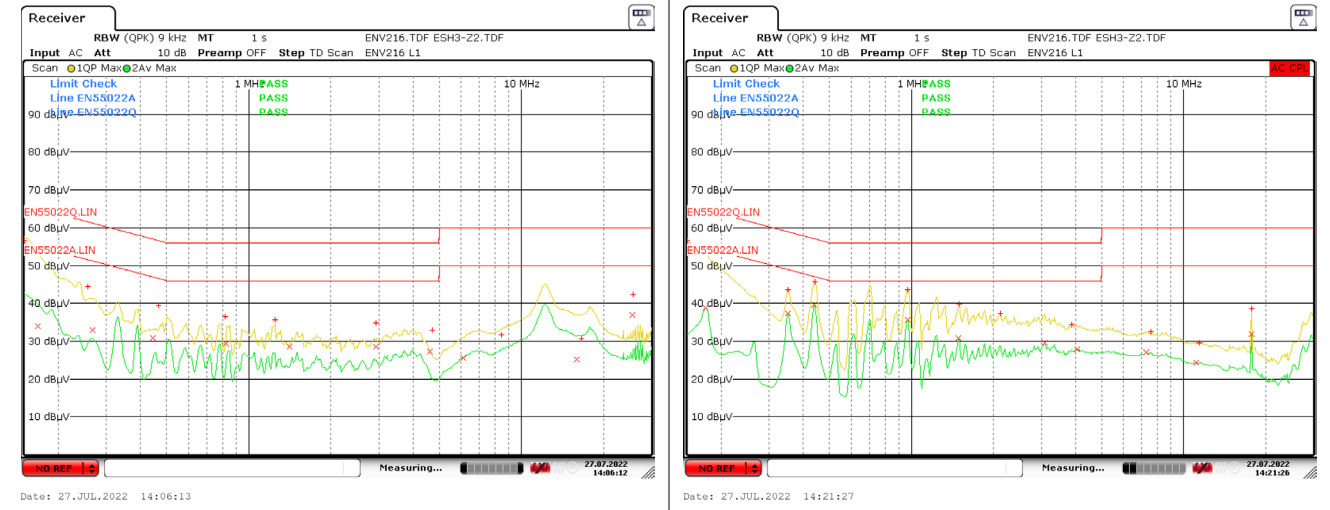
115 VAC.



230 VAC.

Figure 102 – Floating Ground EMI, 15 V / 3 A Load [Neutral Scan].

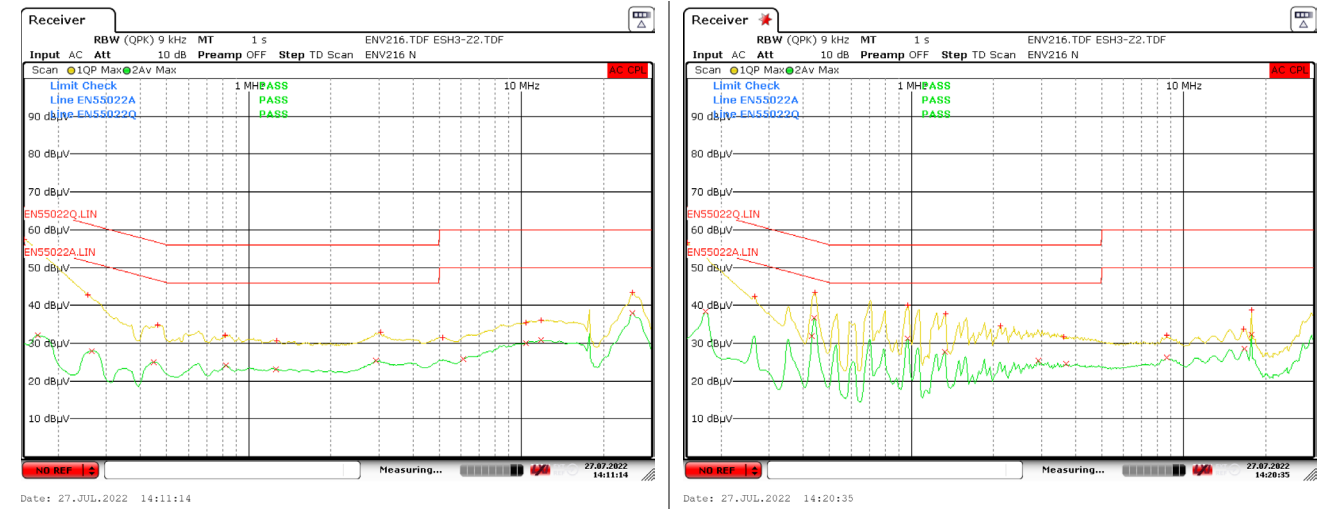
15.1.5 Output: 20 V / 3.25 A



115 VAC.

230 VAC.

Figure 103 – Floating Ground EMI, 20 V / 3.25 A Load [Line Scan].



115 VAC.

230 VAC.

Figure 104 – Floating Ground EMI, 20 V / 3.25 A Load [Neutral Scan].



16 Surge

The unit was subjected to ± 1000 V differential mode and ± 2000 V common mode combination wave surge at several line phase angles with 10 strikes for each condition.

A test failure was defined as an output latch-off that needs operator intervention to recover, or a complete loss of function that is not recoverable.

16.1 Differential Mode Surge (L1 to L2), 230 VAC Input

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 5 V / 0 A without PD Sink	Test Result 20 V / 3.25 A
+1000	L1 to L2	0	PASS	PASS
-1000	L1 to L2	0	PASS	PASS
+1000	L1 to L2	90	PASS	PASS
-1000	L1 to L2	90	PASS	PASS
+1000	L1 to L2	270	PASS	PASS
-1000	L1 to L2	270	PASS	PASS

16.2 Common Mode Surge (L1, L2 to PE), 230 VAC Input

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 5 V / 0 A without PD Sink	Test Result 20 V / 3.25 A
+2000	L1, L2 to PE	0	PASS	PASS
-2000	L1, L2 to PE	0	PASS	PASS
+2000	L1, L2 to PE	90	PASS	PASS
-2000	L1, L2 to PE	90	PASS	PASS
+2000	L1, L2 to PE	270	PASS	PASS
-2000	L1, L2 to PE	270	PASS	PASS

16.3 Common Mode Surge (L1 to PE), 230 VAC Input

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 5 V / 0 A without PD Sink	Test Result 20 V / 3.25 A
+2000	L1 to PE	0	PASS	PASS
-2000	L1 to PE	0	PASS	PASS
+2000	L1 to PE	90	PASS	PASS
-2000	L1 to PE	90	PASS	PASS
+2000	L1 to PE	270	PASS	PASS
-2000	L1 to PE	270	PASS	PASS

16.4 *Common Mode Surge (L2 to PE), 230 VAC Input*

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 5 V / 0 A without PD Sink	Test Result 20 V / 3.25 A
+2000	L2 to PE	0	PASS	PASS
-2000	L2 to PE	0	PASS	PASS
+2000	L2 to PE	90	PASS	PASS
-2000	L2 to PE	90	PASS	PASS
+2000	L2 to PE	270	PASS	PASS
-2000	L2 to PE	270	PASS	PASS

17 Electrostatic Discharge

The unit was tested with ± 8.0 kV to ± 16.5 kV air discharge and ± 8.0 to ± 8.8 kV contact discharge with 10 strikes for each condition at the following locations:

- On-board +VOUT and GND
- End of cable +VOUT and GND
- On-board USB PD Source CC Lines
- End of cable USB PD Sink CC Lines

A test failure was defined as an output latch-off that needs operator intervention to recover, or a complete loss of function that is not recoverable.

17.1 VOUT and GND ESD Performance

Discharge points were added on the board and at the end of cable on the USB PD Sink (CYPD4533 EZ-PD BCR) to test VOUT and GND ESD performance. A 1-meter 5 A USB Type C cable with e-marker (Cable Matters) was used to support 65 W load.

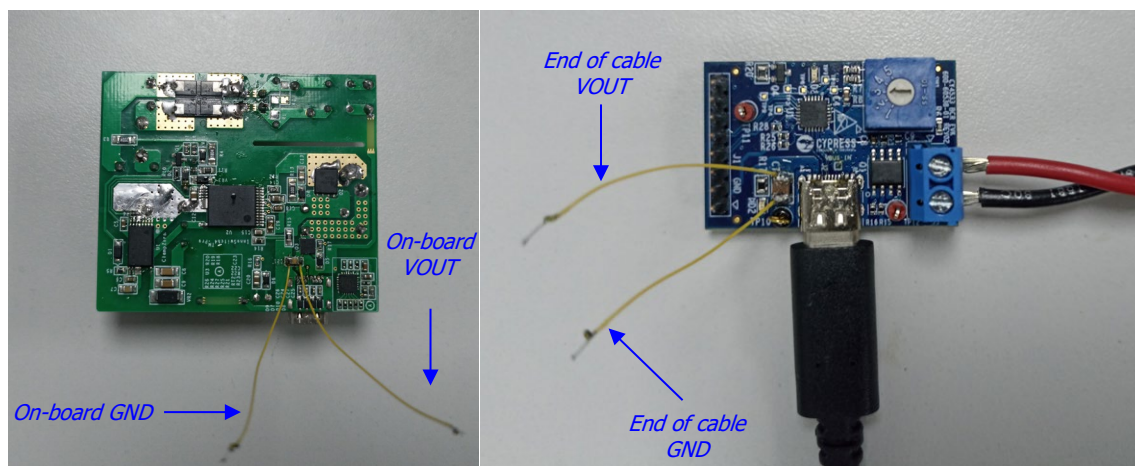


Figure 105 – ESD Discharge Points.

17.1.1 Air Discharge, End of Cable, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (10 Strikes Each)	Test Result 20 V / 3.25 A	Test Result 5 V / 0 A with PD Sink
+8	+VOUT	Pass	Pass
	GND	Pass	Pass
-8	+VOUT	Pass	Pass
	GND	Pass	Pass
+10	+VOUT	Pass	Pass
	GND	Pass	Pass
-10	+VOUT	Pass	Pass
	GND	Pass	Pass
+12	+VOUT	Pass	Pass
	GND	Pass	Pass
-12	+VOUT	Pass	Pass
	GND	Pass	Pass
+14	+VOUT	Pass	Pass
	GND	Pass	Pass
-14	+VOUT	Pass	Pass
	GND	Pass	Pass
+15	+VOUT	Pass	Pass
	GND	Pass	Pass
-15	+VOUT	Pass	Pass
	GND	Pass	Pass
+16.5	+VOUT	Pass	Pass
	GND	Pass	Pass
-16.5	+VOUT	Pass	Pass
	GND	Pass	Pass

17.1.2 Air Discharge, On-board, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (10 Strikes Each)	Test Result 20 V / 3.25 A	Test Result 5 V / 0 A with PD Sink
+8	+VOUT	Pass	Pass
	GND	Pass	Pass
-8	+VOUT	Pass	Pass
	GND	Pass	Pass
+10	+VOUT	Pass	Pass
	GND	Pass	Pass
-10	+VOUT	Pass	Pass
	GND	Pass	Pass
+12	+VOUT	Pass	Pass
	GND	Pass	Pass
-12	+VOUT	Pass	Pass
	GND	Pass	Pass
+14	+VOUT	Pass	Pass
	GND	Pass	Pass
-14	+VOUT	Pass	Pass
	GND	Pass	Pass
+15	+VOUT	Pass	Pass
	GND	Pass	Pass
-15	+VOUT	Pass	Pass
	GND	Pass	Pass
+16.5	+VOUT	Pass	Pass
	GND	Pass	Pass
-16.5	+VOUT	Pass	Pass
	GND	Pass	Pass

17.1.3 Contact Discharge, End of Cable, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (10 Strikes Each)	Test Result 20 V / 3.25 A	Test Result 5 V / 0 A with PD Sink
+8.0	+VOUT	Pass	Pass
	GND	Pass	Pass
-8.0	+VOUT	Pass	Pass
	GND	Pass	Pass
+8.8	+VOUT	Pass	Pass
	GND	Pass	Pass
-8.8	+VOUT	Pass	Pass
	GND	Pass	Pass

17.1.4 Contact Discharge, On the Board, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (10 Strikes Each)	Test Result 20 V / 3.25 A	Test Result 5 V / 0 A with PD Sink
+8.0	+VOUT	Pass	Pass
	GND	Pass	Pass
-8.0	+VOUT	Pass	Pass
	GND	Pass	Pass
+8.8	+VOUT	Pass	Pass
	GND	Pass	Pass
-8.8	+VOUT	Pass	Pass
	GND	Pass	Pass

17.2 CC1 and CC2 ESD Performance

Discharge points were added to the communication lines of the USB PD Sink (TinyPAT) and of the power supply to test CC lines ESD performance. The two CC lines were differentiated by their voltage levels during the normal operation.

- Sink CC Line: Active (~ 1.7 V)
- Sink CC Line: Low (~ 0 V)

Performing ESD on CC lines using a 5 A cable with e-marker can damage the e-marker chip of the cable. A 1-meter 3 A passive USB Type C cable (Google) was used instead to evaluate the unit under test.

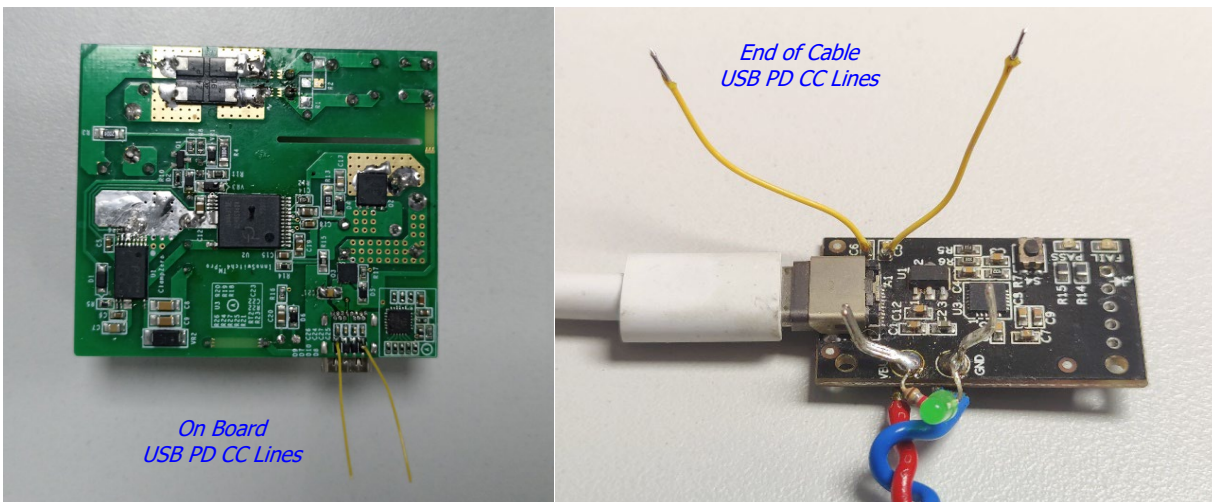


Figure 106 – ESD Discharge Points, USB PD Sink CC Lines.

17.2.1 Air Discharge, On the board, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (10 Strikes Each)	Test Result 20 V / 3.25 A	Test Result 5 V / 0 A with PD Sink
+8	CC Line: Active	Pass	Pass
	CC Line: Low	Pass	Pass
-8	CC Line: Active	Pass	Pass
	CC Line: Low	Pass	Pass
+10	CC Line: Active	Pass	Pass
	CC Line: Low	Pass	Pass
-10	CC Line: Active	Pass	Pass
	CC Line: Low	Pass	Pass
+12	CC Line: Active	Pass	Pass
	CC Line: Low	Pass	Pass
-12	CC Line: Active	Pass	Pass
	CC Line: Low	Pass	Pass
+14	CC Line: Active	Pass	Pass
	CC Line: Low	Pass	Pass
-14	CC Line: Active	Pass	Pass
	CC Line: Low	Pass	Pass
+15	CC Line: Active	Pass	Pass
	CC Line: Low	Pass	Pass
-15	CC Line: Active	Pass	Pass
	CC Line: Low	Pass	Pass
+16.5	CC Line: Active	Pass ¹	Pass ¹
	CC Line: Low	Pass ¹	Pass ¹
-16.5	CC Line: Active	Pass ¹	Pass ¹
	CC Line: Low	Pass ¹	Pass ¹

¹Power supply might initiate Hard Reset due to either:

- PD Controller protection, or
- USB-C power adapter tester Tiny-PAT protection at the load

17.2.2 Air Discharge, End of cable, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (10 Strikes Each)	Test Result 20 V / 3.25 A	Test Result 5 V / 0 A with PD Sink
+8	CC Line: Active	Pass	Pass
	CC Line: Low	Pass	Pass
-8	CC Line: Active	Pass	Pass ¹
	CC Line: Low	Pass	Pass ¹
+10	CC Line: Active	Pass	Pass
	CC Line: Low	Pass	Pass
-10	CC Line: Active	Pass ¹	Pass ¹
	CC Line: Low	Pass ¹	Pass ¹
+12	CC Line: Active	Pass	Pass ¹
	CC Line: Low	Pass ¹	Pass
-12	CC Line: Active	Pass ¹	Pass ¹
	CC Line: Low	Pass ¹	Pass
+14	CC Line: Active	Pass	Pass
	CC Line: Low	Pass	Pass
-14	CC Line: Active	Pass ¹	Pass ¹
	CC Line: Low	Pass	Pass ¹
+16.5	CC Line: Active	Pass ¹	Pass ¹
	CC Line: Low	Pass	Pass ¹
-16.5	CC Line: Active	Pass ¹	Pass ¹
	CC Line: Low	Pass ¹	Pass ¹

¹Power supply might initiate Hard Reset due to either:

- PD Controller protection, or
- USB-C power adapter tester Tiny-PAT protection at the load

17.2.3 Contact Discharge, On the board, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (10 Strikes Each)	Test Result 20 V / 3.25 A	Test Result 5 V / 0 A with PD Sink
+8	CC Line: Active	Pass	Pass
	CC Line: Low	Pass	Pass
-8	CC Line: Active	Pass	Pass
	CC Line: Low	Pass	Pass
+8.8	CC Line: Active	Pass	Pass
	CC Line: Low	Pass	Pass
-8.8	CC Line: Active	Pass	Pass
	CC Line: Low	Pass	Pass

17.2.4 Contact Discharge, End of Cable, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (10 Strikes Each)	Test Result 20 V / 3.25 A	Test Result 5 V / 0 A with PD Sink
+8	CC Line: Active	Pass ¹	Pass ¹
	CC Line: Low	Pass ¹	Pass ¹
-8	CC Line: Active	Pass ¹	Pass ¹
	CC Line: Low	Pass ¹	Pass ¹
+8.8	CC Line: Active	Pass ¹	Pass ¹
	CC Line: Low	Pass ¹	Pass ¹
-8.8	CC Line: Active	Pass ¹	Pass ¹
	CC Line: Low	Pass ¹	Pass ¹

¹Power supply might initiate Hard Reset due to either:

- PD Controller protection, or
- USB-C power adapter tester Tiny-PAT protection at the load

18 Revision History

Date	Author	Revision	Description & Changes	Reviewed
11-Nov-22	RN	1.0	Initial Release.	Apps & Mktg



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Power Integrations Worldwide Sales Support Locations

<p>WORLD HEADQUARTERS 5245 Hellyer Avenue San Jose, CA 95138, USA. Main: +1-408-414-9200 Customer Service: Worldwide: +1-65-635-64480 Americas: +1-408-414-9621 e-mail: usasales@power.com</p>	<p>GERMANY (AC-DC/LED Sales) Einsteinring 24 85609 Dornach/Aschheim Germany Tel: +49-89-5527-39100 e-mail: eurosales@power.com</p>	<p>ITALY Via Milanese 20, 3rd. Fl. 20099 Sesto San Giovanni (MI) Italy Phone: +39-024-550-8701 e-mail: eurosales@power.com</p>	<p>SINGAPORE 51 Newton Road, #19-01/05 Goldhill Plaza Singapore, 308900 Phone: +65-6358-2160 e-mail: singaporesales@power.com</p>
<p>CHINA (SHANGHAI) Rm 2410, Charity Plaza, No. 88, North Caoxi Road, Shanghai, PRC 200030 Phone: +86-21-6354-6323 e-mail: chinasales@power.com</p>	<p>GERMANY (Gate Driver Sales) HellwegForum 1 59469 Ense Germany Tel: +49-2938-64-39990 e-mail: igbt-driver.sales@power.com</p>	<p>JAPAN Yusen Shin-Yokohama 1-chome Bldg. 1-7-9, Shin-Yokohama, Kohoku-ku Yokohama-shi, Kanagawa 222-0033 Japan Phone: +81-45-471-1021 e-mail: japansales@power.com</p>	<p>TAIWAN 5F, No. 318, Nei Hu Rd., Sec. 1 Nei Hu District Taipei 11493, Taiwan R.O.C. Phone: +886-2-2659-4570 e-mail: taiwansales@power.com</p>
<p>CHINA (SHENZHEN) 17/F, Hivac Building, No. 2, Keji Nan 8th Road, Nanshan District, Shenzhen, China, 518057 Phone: +86-755-8672-8689 e-mail: chinasales@power.com</p>	<p>INDIA #1, 14th Main Road Vasanthanagar Bangalore-560052 India Phone: +91-80-4113-8020 e-mail: indiasales@power.com</p>	<p>KOREA RM 602, 6FL Korea City Air Terminal B/D, 159-6 Samsung-Dong, Kangnam-Gu, Seoul, 135-728 Korea Phone: +82-2-2016-6610 e-mail: koreasales@power.com</p>	<p>UK Building 5, Suite 21 The Westbrook Centre Milton Road Cambridge CB4 1YG Phone: +44 (0) 7823-557484 e-mail: eurosales@power.com</p>

